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Drain current enhancement and negligible current collapse in GaN MOSFETs with atomic-layer-deposited HfO_2 as a gate dielectric

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ABSTRACT

Accumulation-type GaN metal–oxide-semiconductor field-effect-transistors (MOSFET's) with atomic-layer-deposited HfO_2 gate dielectrics have been fabricated; a 4 μm gate-length device with a gate dielectric of 14.8 nm in thickness (an equivalent SiO_2 thickness of 3.8 nm) gave a drain current of 230 mA/mm and a broad maximum transconductance of 31 mS/mm. Owing to a low interfacial density of states (D_{it}) at the HfO_2/GaN interface, more than two third of the drain currents come from accumulation, in contrast to those of Schottky-gate GaN devices. The device also showed negligible current collapse in a wide range of bias voltages, again due to the low D_{it}, which effectively passivate the surface states located in the gate-drain access region. Moreover, the device demonstrated a larger forward gate bias of +6 V with a much lower gate leakage current.

1. Introduction

GaN and its derives have been widely studied for applications in high-power devices in high electron mobility transistors (HEMT's) [1–6]. With the surface Fermi level of GaN being unpinned with SiO_2 [7], and high κ dielectrics of HfO_2 [8,9], Al_2O_3 [10,11] Gd_2O_3 [12,13], and MgO [14], GaN metal–oxide-semiconductor field-effect-transistors (MOSFET's) have attracted much interest lately [15–21]. The discovery of $Ga_2O_3(Gd_2O_3)$ as a gate dielectric has led to the first depletion-mode GaN MOSFET [15]. Recently, inversion-channel GaN MOSFET's were also demonstrated, with the electrical characteristics resembling that of the Si based MOSFET's [18–21].

Among the gate dielectrics, HfO_2, due to its high dielectric constant of 18–20, highly insulating electrical property and a large energy-band gap (5.4–5.8 eV), has been applied in Si CMOS and studied in III–V MOS devices [22,23]. In our previous work of GaN MOS capacitors with nanometer-thick atomic-layer-deposited (ALD) HfO_2, low electrical leakage currents and low interfacial density of states (D_{it}) were obtained [8]; these may lead to lower gate leakage currents, a larger gate voltage sweeping range, and a simpler device/circuit structure in GaN MOSFET's, compared with their counterparts of HEMT's with Schottky-gates. Moreover, the current collapse that occurs in unpassivated HEMT devices (caused by the traps existed in the regions between the gate and drain electrodes) could also be minimized/eliminated in GaN MOSFET's. The current collapse significantly reduces RF output power and degrades the device performance.

In this letter, we report a high-performance accumulation-type GaN MOSFET based on ALD-HfO_2 as a gate dielectric. Compared to the previously reported GaN-based MOSFET's and HEMT's, the device demonstrates excellent dc output as well as transfer characteristics, such as a high drain current (I_d) with negligible current collapse, a high transconductance (G_m), low gate leakage currents, and a large gate voltage sweep range.

The growth of HfO_2/GaN was described earlier, with GaN grown by metal organic chemical vapor deposition and HfO_2 by ALD with tetrakis-(ethyl-methyl-amino)-hafnium (TEMAH) and H_2O as the precursors [8]. A post-deposition anneal at 600 °C was carried out under nitrogen ambiance for 10 min to optimize oxide and interface quality. X-ray reflectivity measurements [24] for the annealed sample have revealed that the oxide consists of two layers with an overall thickness of 14.8 nm, bulk HfO_2 (13.2 nm) and an interfacial layer GaON 1.6 nm thick. The interfacial roughness was small of 0.41 nm, critical to make a high-performance device. The determination of oxide film thickness was needed for fabricating the device.

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Ring-gate accumulation-type GaN MOSFET's were fabricated with a two-step process (S/D contact metal and gate metal formation). The S/D contact on the doped GaN was achieved by etching HfO_2 using dilute hydrofluoric acid (HF), removing the interfacial layer GaON layer using dilute hydrochloric acid (HCl), followed by e-beam evaporating metal Ti/Al (30 nm/120 nm) on GaN and rapid thermal annealing (RTA) to 600 °C and dwelling there for 30 s under nitrogen ambience. Finally, Al (120 nm) was e-beam evaporated as the gate electrodes. Both the source-to-gate and the gate-to-drain spacing are 3 μm. The schematic cross-sectional and the planar views of the fabricated ring-gate GaN MOSFET are shown in Fig. 1(a) and (b), respectively.

Fig. 2(a) shows the drain *I*–*V* characteristics of a 4 μm gate-length MOSFET with the gate voltage (V_g) varying from −8 V to +6 V with a step of 2 V. The pinch-off voltage of the fabricated device is −8 V. The maximum $I_d \sim 230$ mA mm at V_g of +6 V and a drain voltage (V_d) of 20 V has been achieved, the highest ever reported for GaN MOSFETs, which is owing to the effective passivation of HfO_2/GaN interface with a low D_{it} and the high dielectric constant of HfO_2. These remarkable interfacial material/electrical properties have led to a more efficient gate modulation and an accumulation of more carriers in the channel layer, thus giving higher accumulated currents at +6 V. Compared to Schottky-gated GaN devices with a barrier built-in voltage <1 V, our device demonstrated a larger positive gate voltage (+6 V) with a low gate leakage current which is resulted from the high conduction-band offset >2 eV of HfO_2/GaN [25] and the low D_{it} between HfO_2 and GaN. A low specific on-resistance (R_{on}) ~4.5 mΩ cm^2 was achieved even though the gate-to-source spacing was large of 3 μm and the doping concentration of channel layer was as low as 2×10^{17} cm^{-3}.

The transfer characteristics ($L_g/W_g = 4$ μm/200 μm), with V_g sweeping from −8 V to +4 V, and for V_d of 15 V, are shown in Fig. 2(b). The device exhibits a broad extrinsic G_m curve, with the peak G_m being ~31 mS/mm with V_d of 15 V. The calculated channel mobility (μ_n) of ~400 cm^2/Vs was derived using the following equation: $\mu_n = G_m\,(L_g/W_g)/N_d T_{ch}$, where N_d and T_{ch} are the doping concentration and the thickness of the channel layer [17]. An I_{on}/I_{off} ratio was extracted to be $\sim 10^2$ with a high off-state drain current (I_{off}) of 10^{-6}A/μm at a V_d of 15 V. The channel leakage currents, resulted from the undoped GaN layer with unintentional donor doping concentration of $\sim 10^{16}$ cm^{-3}, may have caused high I_{off}, which can be improved by inserting a *p*-type GaN layer under the *n*-channel layer as a junction barrier to reduce the additional channel leakage currents.

A D_{it} was calculated to be around $(5–8) \times 10^{11}$ cm^{-2} eV^{-1} near conduction-band minimum of GaN using the conductance method, based on capacitance–voltage (*C*–*V*) characteristics of Al/HfO_2/GaN MOS capacitor, which exhibited clear accumulation, depletion, deep depletion behavior, and small hysteresis of 160 mV (shown in the inset of Fig. 2(b)). The well-behaved *C*–*V* characteristics and a low D_{it} indicate the high-quality interface of HfO_2/GaN.

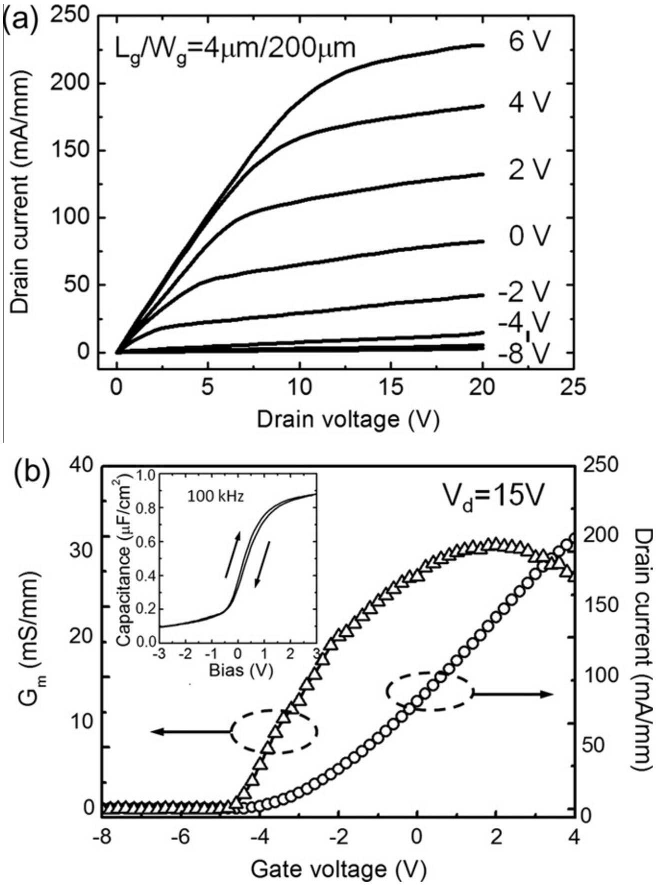

Fig. 2. (a) Drain *I*–*V* characteristic for a 4 μm gate-length GaN MOSFET with a 14.8 nm ALD-HfO_2 as a gate dielectric; and (b) transconductance (G_m) and drain current as a function of gate bias at a drain voltage of 15 V, with the inset showing *C*–*V* hysteresis measured at 100 kHz for the Al/HfO_2/GaN MOS capacitor.

The gate-to-drain, gate leakage current density (J_g) as a function of gate voltage of the device was measured by grounding the drain, and sweeping V_g from −10 V to +8 V. The very low J_g of 10^{-8} A/cm^2

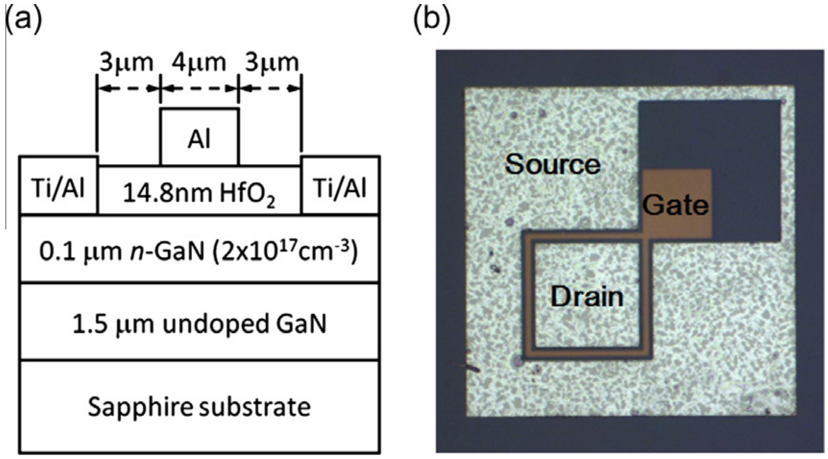

Fig. 1. (a) Schematic device structure of fabricated accumulation-type GaN MOSFET; (b) planar view of ring-gate MOSFET structure.

at V_g varying from −10 V to +2 V was achieved (Fig. 3(a)) and is significantly lower than that of the Schottky-gate GaN devices by at least five orders of magnitude at $V_g > +1$ V. Even at the gate voltage of +6 V, the device also provides the gate leakage current density as low as 10^{-2} A/cm^2. The low gate leakage current reveals the high-quality and robustness of the HfO_2/GaN heterostructure after 600 °C annealing. The oxide breakdown voltage is 6.5 V, corresponding to an electrical breakdown field of 4.4 MV/cm. In addition, the measured I_g–V_d characteristics of the GaN MOSFET's under the off-state gate bias condition ($V_g = -8$ V) is also shown in the inset of Fig. 3(a). The extremely low $I_g \sim 10^{-8}$ mA/mm was observed even at V_d over 30 V. The three-terminal breakdown voltage (BV_{DS}) of the GaN MOSFET is more than 60 V even with the gate-to-drain spacing of 3 µm. The high BV_{DS} value is also an evidence of a high-quality HfO_2/GaN interface that has sustained the high electrical fields.

The pulsed *I–V* measurements with different pulse widths of 80 µs and 300 µs were performed to analyze the current collapse on the device, and are shown in Fig. 3(b) along with that of DC condition. No significant current collapse was observed in both pulse *I–V* curves, as evidenced by the negligible dispersion between DC and pulsed *I–V* curves in the knee region, and no I_d reduction of both pulsed *I–V* curves in the saturation region. This observation strongly indicates the effective surface passivation of GaN using ALD-HfO_2, that has decreased the surface states at the region between the gate and drain electrodes. An increased I_d of pulsed *I–V* curves was observed which is due to the relieving of self-heating effect occurring under high drain bias. In addition, the pulsed *I–V* curve with a shorter pulse width of 80 µs shows a higher I_d in the saturation region which also manifests the existence of self-heating effect in the device.

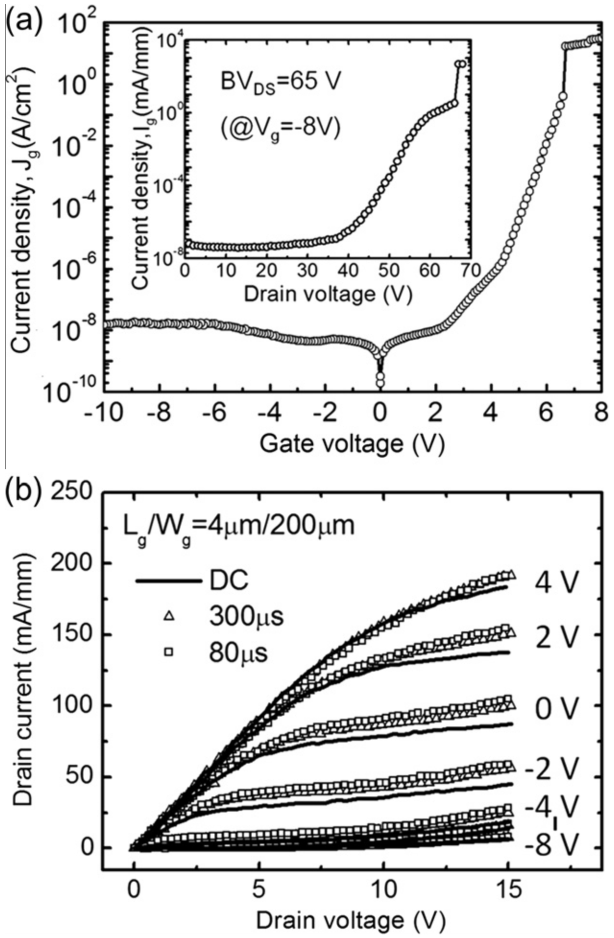

Fig. 3. (a) Gate leakage current density (J_g) vs gate voltage for GaN MOSFET, with the I_g–V_d characteristics under the off-state gate bias condition plotted in the inset; (b) pulsed *I–V* characteristics with pulse widths of 300 µs and 80 µs.

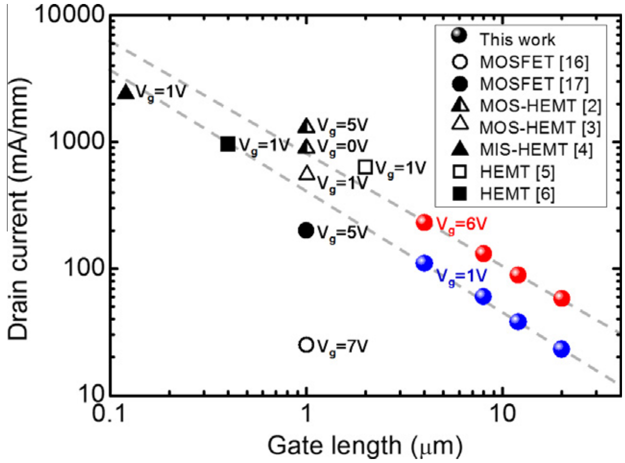

Fig. 4. Summary of maximum drain current vs. gate length of representative work on GaN-based devices.

Maximum drain currents of representative GaN-based MOSFET, MOS-HEMT, and HEMT devices are summarized in Fig. 4 [2–6,16,17]. This work has achieved I_d of 230 mA/mm and G_m of 31 mS/mm, compared favorably to those of previously reported GaN MOSFET's [15–21]. In particular, the drain current achieved in our 4 µm-gate-length device is comparable to that of the 1 µm-gate-length GaN MOSFET using ALD-Al_2O_3 as a gate dielectric [17]. The measured drain currents in our GaN MOSFET's are scaled with gate lengths under $V_g = 6$ V and $V_g = 1$ V with $V_d = 20$ V. For a simple linear extrapolation, we expect to have the maximum drain current of 800 mA/mm under $V_g = 6$ V and 450 mA/mm under $V_g = 1$ V for 1 µm gate-length device, respectively, not considering parasitic resistance and short-channel effect; this is comparable to the results of the state-of-the-art GaN-based HEMT's [2–6] and higher than those of the previous reported accumulation-type GaN MOSFET's [16,17]. Nevertheless, the simply-designed HfO_2/GaN MOSFET's provides extremely low gate leakage currents and negligible current collapse.

In summary, we have demonstrated accumulation-type GaN MOSFET's using ALD-HfO_2 as a gate dielectric with high drain current and negligible current collapse. The large dielectric constant of HfO_2 and high-quality HfO_2/GaN interface have attributed to the high device performance. Notice that the device structure is simple. These results presented in this work have shown that GaN MOSFET's also have excellent potential for high-power RF application.

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