First Demonstration of Monolithic InP-Based HBT Amplifier With PNP Active Load

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***Abstract*—An InP-based integrated HBT amplifier with PNP active load was demonstrated for the first time using complementary HBT technology (CHBT). Selective molecular beam epitaxy (MBE) regrowth was employed and a merged processing technology was developed for the monolithic integration of InP-based NPN and PNP HBTs on the same chip. The availability of PNP devices allowed design of high gain amplifiers with low power supply voltage. The measured amplifier with PNP HBT active load achieved a voltage gain of 100 with a power supply (V_{CC}) of 1.5 V. The corresponding voltage swing was 0.9 V to 0.2 V. The amplifier also demonstrated S_{21} of 7.8 dB with an associated S_{11} and S_{22} of -9.5 dB and -8.1 dB, respectively, at 10 GHz.**

***Index Terms*—Amplifier, complementary, HBT, InP, monolithic.**

I. INTRODUCTION

InP-BASED HBT technology is very attractive for low power, high-speed electronics due to its low turn-on voltage, exceptionally superior high-frequency performance, and excellent current-handling ability [1]–[3]. However, without a complementary device such as PNP HBT, its application could be limited. For example, an important objective in feedback amplifier design is to obtain the required voltage gain in as few stages as possible [4]. With a complementary device (PNP HBT) as its load element, the power supply voltage of InP-based HBT MMIC could be further lowered.

Significant effort has been made in developing GaAs-based HBT complementary technology and prototype circuits including push–pull amplifiers have been demonstrated [5]–[11]. For InP-based HBT technology, such efforts have been minimal. Reports have been made on monolithic integrated complementary InP HBT technology using MBE growth on patterned substrates [12]. However, these refer to the feasibility of device integration and no circuit results have been reported.

Monolithic integration of NPN and PNP InAlAs/InGaAs complementary HBTs has been demonstrated by the authors using regrowth by MBE [13]. The NPN HBT structure consists of a 4300 Å subcollector, a 7000 Å collector, an 800 Å base, a 450 Å graded InAlGaAs transition layer, 1450 Å InAlAs emitter layers, and 750 Å InGaAs emitter cap layer. The PNP HBT structure consists of a 10 000 Å subcollector, a 3000 Å collector, a 500 Å base, a 100 Å InGaAs spacer layer, 2200 Å InAlAs emitter layer, and a 2000 Å InGaAs emitter cap layer. Silicon and beryllium were used as n-type and p-type dopants, respectively. The integrated HBTs showed little degradation over similar discrete devices. The DC gain was 35 for both integrated NPN and PNP HBTs. f_T of 79.6 GHz and $f_{\max}$ of 109 GHz were achieved for NPN devices while f_T of 11.6 GHz and $f_{\max}$ of 22.6 GHz were achieved for PNP devices. Due to the superior electron transport characteristics compared with those of holes, a large mismatch exists between the NPN and PNP device performance. This mismatch could lead to performance degradation in circuit applications such as push–pull amplifiers, where both NPN and PNP HBTs are used as amplifying devices. Performance degradation is, however, expected to be less important when the PNP device is employed as an active load as illustrated in this paper.

With the developed complementary InP-based HBT technology and also by taking advantage of the output resistance of a PNP transistor, large voltage gain can be achieved requiring small power-supply voltage. This paper reports an InP-based HBT amplifier with monolithically integrated PNP active load for the first time. The processing technology, circuit design, fabrication and measurement results are also presented.

II. DEVICE TECHNOLOGY

Selective MBE regrowth was employed for circuit realization. First, a PNP structure was grown over the entire wafer by MBE and then coated with Si_3N_4 dielectric as a mask layer. The wafer was then patterned so that the areas intended for PNP transistors were masked. After lithography, the unmasked Si_3N_4 material and PNP layers was etched and the substrate surface was revealed. The wafer was then introduced in an MBE chamber for regrowth of the semiconductor layers corresponding to the NPN HBT structure.

After regrowth, the wafer was patterned again to expose the area where the polycrystalline NPN material was grown. The polycrystalline NPN material was then etched all the way down to the Si_3N_4 mask. Finally, the Si_3N_4 mask was etched by BHF to expose the PNP material. The wafer was at this stage planarized and ready for device fabrication.

The detailed epitaxial layer structures for InAlAs/InGaAs NPN and PNP HBTs can be found in [13]. The processing steps of the devices were similar to those for discrete HBTs [14], [15]. Ti/Pt/Au and Pt/Ti/Pt/Au were used as contact metals for N and P-layers respectively. An exception to this was that the emitter metals of NPN and PNP devices were deposited together using Pt/Ti/Pt/Au. This simplified the process without significant compromise in emitter resistance for the NPN

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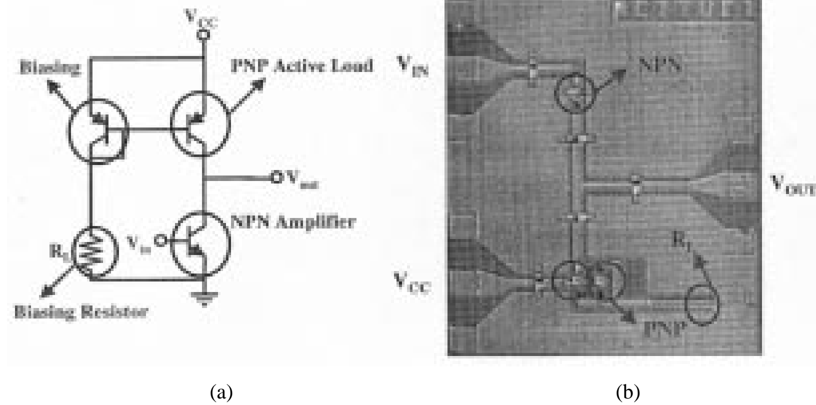
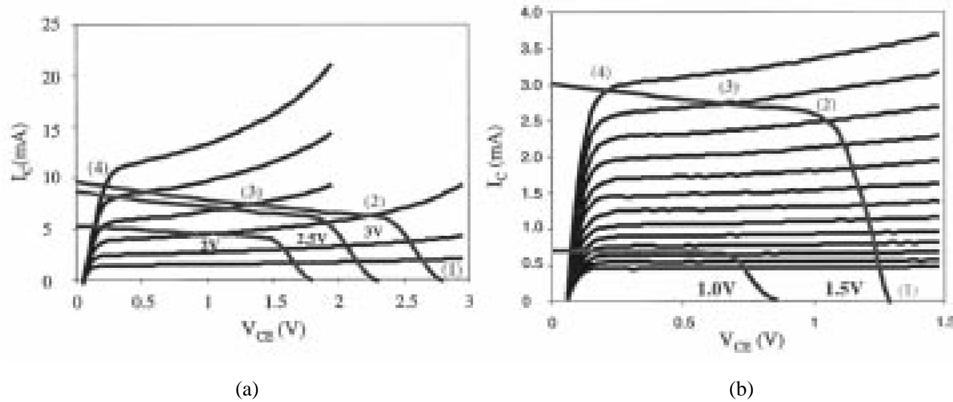


(a) (b)

Fig. 1. (a) Circuit diagram for InP-based HBT common-emitter amplifier with PNP device as active load and (b) circuit photo for InP-based HBT common-emitter amplifier with PNP device as active load.



(a) (b)

Fig. 2. (a) Common emitter NPN HBT characteristics with the superimposed PNP HBT active load line ($V_{\rm CC}$ of 3 V, 2.5 V and 2 V) and (b) common emitter NPN HBT characteristics with the superimposed PNP HBT active load line ($V_{\rm CC}$ of 1.5 V and 1 V).

HBT due to the high doping concentration of the emitter cap layer. The base and collector layers were reached and contact metals were deposited by processing individually the NPN and PNP HBTs. MIM capacitors was included employing a 2000 Å-thick Si_3N_4 as dielectric layer sandwiched between the top and bottom metal plates. Thin film resistors utilized a 700 Å-thick Ni/Cr with a sheet resistance of 20 $\Omega/\Box$.

III. Circuit Design

Active devices can be used in either biasing a circuit as current sources or as load elements for an amplifier stage. Compared to resistors, these active devices are usually more economical in terms of chip area.

By taking advantage of the high output resistance of a PNP transistor, large voltage gain can be achieved requiring just small power-supply voltage. For portable electronic devices, which require low operation power and long battery life, this could consequently be of great interest [4].

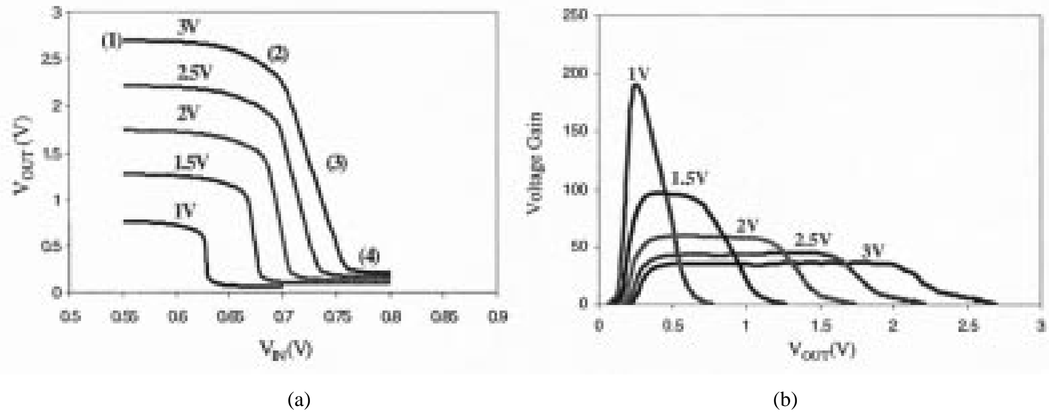
The circuit diagram for a common-emitter amplifier with active load is shown in Fig. 1(a). In this circuit, $5 \times 10\ \mu\text{m}^2$ NPN and PNP InP-based HBTs were used as amplifying device and active load respectively. The fabricated circuit photograph is shown in Fig. 1(b). The chip size for this amplifier is 0.78 mm $\times$ 0.93 mm.

IV. Experimental Performance

Fig. 2(a) and (b) shows the experimental NPN I-V characteristics along with the active load line. As can be seen, the load line corresponds to the PNP HBT I-V characteristics. The I-V curve is merely flipped about the horizontal axis and shifted to the right by the amount of supply voltage $(V_{\rm CC})$ used. Fig. 2(a) shows the case of $V_{\rm CC}$ equal to 3 V, 2.5 V and 2 V, and Fig. 2(b) shows the case of $V_{\rm CC}$ equal to 1.5 V and 1 V.

The operation principle of this amplifier is as follows: The NPN HBT is turned off in region 1 in the absence of an input drive signal. As the base-emitter voltage increased, the output voltage decreased along the PNP active load line. Initially, the PNP transistor is saturated as indicated in the region between point 1 and 2. As the output voltage decreased further and the PNP transistor moves into the forward active region, a small increase in input voltage leads in rapid shift of the NPN transistor from the forward active region (3) into the saturation region (4). The useful operation region for such circuit is in region 3 where both NPN and PNP transistors are in the forward active region and a small increment in input voltage results in large variation in output voltage and therefore large voltage gain.

The measured DC transfer characteristics of the InP-based HBT common emitter amplifier with PNP HBT active load are shown in Fig. 3(a) for $V_{\rm CC}$ of 3 V, 2.5 V, 2 V, 1.5 V, and 1 V, respectively. The corresponding operation regions are also plotted similarly to the results present in Fig. 2(a) and (b).



(a) (b)

Fig. 3. (a) DC transfer characteristics of InP-based HBT common emitter amplifier with PNP HBT active load ($V_{\rm CC} = 3, 2.5, 2$ V, 1.5 V, $1V$) and (b) voltage gain as a function of output voltage for InP-based HBT common emitter amplifier with PNP HBT active load.

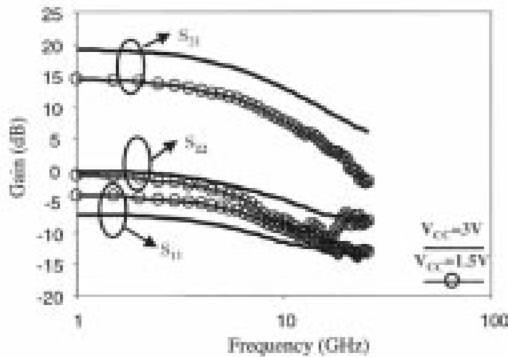


Fig. 4. Microwave gain of InP-based HBT common emitter amplifier with PNP HBT active load at $V_{\rm CC}$ of 3 V and 1.5 V.

The voltage gain as a function of the output voltage is shown in Fig. 3(b). As can be seen, as $V_{\rm CC}$ decreases from 3.0 V to 1.5 V, the voltage gain increases from 40 to 100. The corresponding output swing (linear region) for $V_{\rm CC}$ of 3 V and 1.5 V is from 2.2 V to 0.3 V and from 0.9 V to 0.2 V respectively. The linear region here is defined as the region bounded by the upper and lower output voltages where the gain decreased to one half of the peak voltage gain. The increase of voltage gain as the power supply voltage decreases can be explained by the increase of device Early voltage as the collector-emitter voltage of the HBT devices decreases. This trend can be clearly seen from the DC characteristics of the NPN and PNP HBT shown in Fig. 2(a) and (b) where the collector current increases at a faster pace in the higher than lower collector-emitter voltage region due to device self-heating and soft-breakdown.

Fig. 3(b) also shows that a voltage gain of about 200 can be achieved with a power supply voltage of only 1.0 V. However, the useful output voltage swing (linear region) is limited in the range of 0.45 V to 0.18 V due to the knee voltage of PNP and NPN HBTs. The upper output voltage swing is particularly degraded with the relatively large knee voltage of PNP device. This is due to the inherently large collector resistance of PNP HBTs as a result of the p-type doped material.

The microwave performance of the fabricated InP-based HBT common emitter amplifier with PNP HBT as active load was measured and plotted in Fig. 4 for a power supply voltage $V_{\rm CC}$ of 3.0 V and 1.5 V. As can be seen, the circuit showed S_{21} of 13 dB and S_{11} of -11.5 dB and S_{22} of -5 dB at 10 GHz for $V_{\rm CC}$ of 3.0 V. At $V_{\rm CC}$ of 1.5 V, 7.8 dB S_{21} was measured at 10 GHz with the associated S_{11} and S_{22} of -9.5 dB and -8.1 dB respectively. For these measurements, the input bias voltages were set to maintain the output voltage in the linear region. For example, at $V_{\rm CC}$ of 3.0 V and 1.5 V, the measurements shown in Fig. 4 were performed with the corresponding output voltages of 1.27 V and 0.6 V. These output voltages were approximately the middle point of the respective linear region as shown in Fig. 3(a) (region 3) for $V_{\rm CC}$ of 3 V (2.2 V to 0.3 V voltage swing) and $V_{\rm CC}$ of 1.5 V (0.9 V to 0.2 V voltage swing). The further reduction of $V_{\rm CC}$ to 1 V reduced the microwave gain further as the HBT was biased at lower current level. However, the circuit still showed positive S_{21} of 1.7 dB with the associated S_{11} and S_{22} of -6.2 and -7.1 dB at 10 GHz.

The operation frequency of the investigated amplifier is limited by the characteristics of the PNP HBT. Potential improvement of performance can be expected by further optimization of the HBT layer structure such as introduction of composition and doping gradient in the base to assist the transport of hole carriers by establishing a built-in electrical field. Other structure improvements, including thinner emitter layer, emitter cap layer and collector layer, could also be used for minimization of the emitter and collector resistances. HBT layouts can also be modified, such as, by employing one base contact per emitter finger, to reduce the extrinsic semiconductor region under the base contacts and hence reduce base-collector capacitance $C_{\rm BC}$ [16]. Self-aligned collector contacts can be adopted to reduce collector resistance R_C [17]. As a result, the improved PNP HBT performance combined with the superior InP-based NPN HBT performance than their GaAs-based HBT counterparts makes InP-based complementary HBT technology an ideal substitute for GaAs-based complementary technology.

V. Conclusion

A complementary InP-based HBT technology was developed to monolithically integrate NPN and PNP HBTs on the same chip. This technology was applied to realize a common emitter amplifier with PNP device as active load. Voltage gain of almost

100 was achieved with a power supply voltage ($V_{\rm CC}$) of 1.5 V. The voltage swing was from 2.2 V to 0.3 V and 0.9 V to 0.2 V respectively for $V_{\rm CC}$ of 3 V and 1.5 V. A voltage gain of 200 was also demonstrated for $V_{\rm CC}$ of only 1 V. However, the maximum voltage swing is limited due to the relatively large collector resistance for PNP HBT. Moreover, 13 dB and 7.8 dB gain (S_{21}) were achieved at 10 GHz with $V_{\rm CC}$ of 3 V and 1.5 V. The resulted high gain amplifier with low power supply voltage shows promising features for the application of the developed complementary InP-based HBT (CHBT) technology in low power and high speed electronics.

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