AlGaN/GaN HEMTs With Low Leakage Current and High On/Off Current Ratio

Yu-Syuan Lin, Yi-Wei Lain, and Shawn S. H. Hsu

***Abstract*—In this letter, we propose using an oxide-filled isolation structure followed by N_2/H_2 postgate annealing to reduce the leakage current in AlGaN/GaN HEMTs. An OFF-state drain leakage current that is smaller than 10^{-9} A/mm (minimum 5.1×10^{-10} A/mm) can be achieved, and a gate leakage current in the range of 7.8×10^{-10} to 9.2×10^{-11} A/mm (V_{GS} from -10 to 0 V and $V_{DS} = 10$ V) is obtained. The substantially reduced leakage current results in an excellent ON/OFF current ratio that is up to 1.5×10^8. An improved flicker noise characteristic is also observed in the oxide-filled devices compared with that in the traditional mesa-isolated GaN HEMTs.**

***Index Terms*—Flicker noise, GaN, HEMTs, leakage current.**

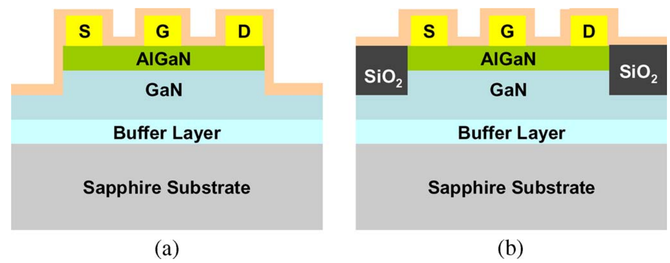

Fig. 1. AlGaN/GaN HEMTs. (a) Mesa isolation structure. (b) Oxide-filled isolation structure.

I. Introduction

High-performance AlGaN/GaN HEMTs have been successfully demonstrated for various applications in recent years [1], [2]. One of the critical issues that still remain for GaN HEMTs is the leakage current which causes additional noise source [3], current collapse effect [4], and reliability problems [5]. Experimental results also indicate that a leakage current results in a lowered breakdown voltage due to the hot-carrier-induced impact ionization [6]. The leakage current was also reported to increase the OFF-state loss and reduce the power supply efficiency [7].

Different approaches were proposed to reduce the gate leakage current [8]–[12]. One straightforward solution was to add an additional gate dielectric layer (MIS-HEMT structure) to block the leakage current path [8]–[10]. A gate leakage current that is as low as 10^{-9} A/mm was reported [8], while the transconductance was relatively low due to the reduced channel control capability [10]. In addition, fluoride or O_2 plasma treatments were employed to reduce the gate leakage current [11], [12], and a leakage current in the range of 10^{-5} to 10^{-8} A/mm was achieved. Different studies were also conducted to investigate the origins of the leakage current [13], [14].

In this letter, we propose a method using the oxide-filled mesa region followed by postgate annealing under a N_2/H_2 mixture ambient to reduce the transistor leakage current. Previous studies reported that the etching process for mesa isolation in GaN-based devices produced deep level traps, causing an increased leakage current [15], [16]. It was found that the defect charges around the gate finger could result in barrier narrowing in the AlGaN cap layer, leading to increased gate leakage current [6]. It was also reported that the OFF-state leakage current can be improved if the gate Schottky contacts are not directly affected by the mesa region [17]. With the proposed oxide-filled structure, the surface states and traps around the mesa edge can effectively be eliminated. Compared with the conventional mesa-isolated structure, the gate finger tips across the trap-rich mesa edge can also be prevented. Moreover, the postgate annealing treatment with forming gas further reduces the traps by hydrogen passivation. The measured results demonstrate a substantially reduced gate and drain leakage current and an extremely high ON/OFF drain current ratio in the proposed oxide-filled GaN HEMTs.

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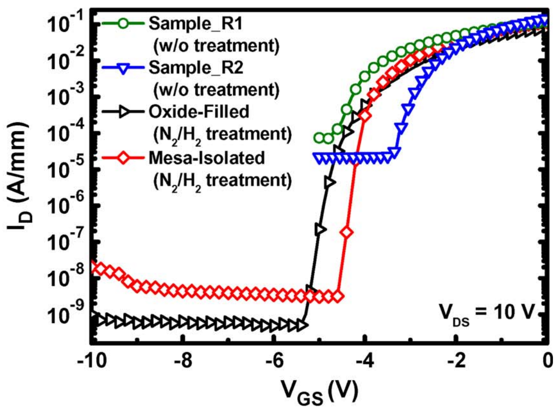
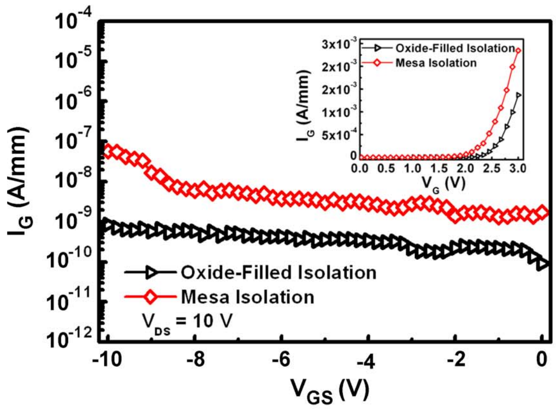
II. Device Design and Fabrication

Fig. 1(a) and (b) shows the cross sections of the AlGaN/GaN HEMTs using the traditional mesa isolation and the proposed oxide-filled isolation structures, respectively. The device structure was grown on a c-plane sapphire substrate by metal–organic chemical vapor deposition, which consisted of a GaN buffer layer, a 3-μm undoped GaN layer, a 3-nm undoped AlGaN layer, a 20-nm n-doped AlGaN barrier layer (25% Al composition), and, finally, a 5-nm undoped AlGaN cap layer. The source/drain ohmic contacts were first formed by Ti/Al/Ti/Au deposition using rapid thermal annealing at 800 °C for 30 s in a N_2 ambient. After making the ohmic contact, a mesa isolation process was done by dry etching using a Cl_2/Ar gas mixture with an etching depth of 300 nm. The etched region around the mesa was then refilled by the e-beam oxide and followed by a lift-off process. Subsequently, a Ni/Au contact (20 nm/300 nm) was deposited to form the Schottky gate. The sample was then subscribed to the postgate annealing



(a)



(b)

Fig. 2. (a) Measured I_D–$V_{\rm GS}$ characteristics. (b) Measured gate leakage current as a function of gate bias.

treatment at 350 °C for 60 s in a N_2/H_2 ambient. Finally, a PECVD Si_3N_4/SiO_2 layer of 0.4 μm/0.8 μm was deposited for surface passivation. Note that the reference design with the conventional mesa isolation had identical process steps except the e-beam oxide refill. Furthermore, the two designs use the same device geometry with the gate length L_g, the gate-to-drain spacing $L_{\rm gd}$, and the gate-to-source spacing $L_{\rm gs}$, all of 2 μm. The overall finger width of the devices is 50 μm.

III. Results and Discussion

Fig. 2(a) shows the I_D–$V_{\rm GS}$ characteristics, where five typical devices are averaged to show a more statistical result. The results from our previous studies with identical process steps and similar material layers except the oxide-filled isolation and postgate annealing are also presented for comparison (sample_R1 and sample_R2). Some performance figures of the devices shown in Fig. 2(a) are as follows. The $I_{D,\max}$ (under $V_G = 0$ V and $V_D = 10$ V) are 115 mA/mm (sample_R1), 144 mA/mm (sample_R2), 80 mA/mm (oxide filled), and 114 mA/mm (mesa isolated). The corresponding $g_{\rm mpk}$ (peak transconductance) are 36, 77, 30, and 42 mS/mm, respectively, and the values of the source resistance R_s are 13.3, 9.2, 16.6, and 13.2 $\Omega \cdot$ mm, respectively. The threshold voltages of the R1, R2, oxide-filled, and mesa-isolated devices are -4.8, -3.3, -5.1, and -4.6 V, respectively.

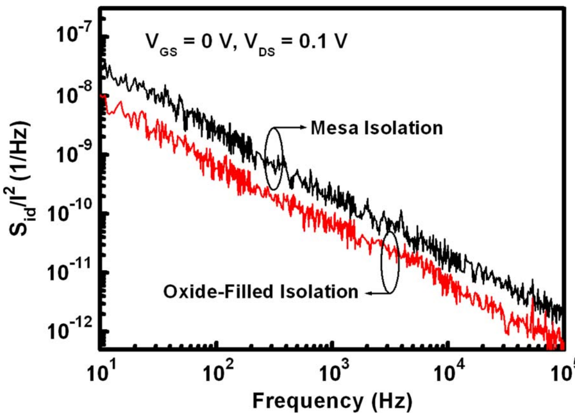


Fig. 3. Measured flicker noise characteristics.

As for the leakage characteristics, the devices with oxide-filled isolation demonstrate an extremely low OFF-state leakage current ($I_D < 1.0 \times 10^{-9}$ A/mm; minimum 5.1×10^{-10} A/mm at $V_{\rm GS} = -5.4$ V) and an excellent ON/OFF current ratio that is up to 1.5×10^8 (a standard deviation of 22%). Even for the conventional mesa-isolated HEMTs, the OFF-state I_D is smaller than 2.1×10^{-8} A/mm (minimum 3.2×10^{-9} A/mm at $V_{\rm GS} = -4.6$ V), and a ratio that is up to 3.5×10^7 can be obtained (a standard deviation of 24%), which is greatly improved compared with that reported for traditional GaN HEMTs without the proposed forming gas treatment (typical OFF-state $I_D \sim 10^{-4}$ to 10^{-6} A/mm; see sample_R1, R2, [18], and [19]). It can be seen that postgate annealing reduces the leakage current by more than three orders of magnitude. With the additional oxide-filled process, the leakage current is further improved by another one to two orders of magnitude. Note that the threshold voltage shifting toward a more negative value is observed in the oxide-filled devices. Similar trends were observed for the devices after surface passivation and explained by the reduced donorlike traps [20]. With the oxide-filled process, the traps at the mesa edge particularly underneath the Schottky gate are reduced, and a similar explanation can be applied.

Fig. 2(b) shows the measured gate leakage under the reverse bias condition, and the forward characteristics are also illustrated in the inset. The gate leakage current levels are in ranges of 7.8×10^{-10} to 9.2×10^{-11} A/mm and 5.8×10^{-8} to 1.7×10^{-9} A/mm ($V_{\rm GS}$ from -10 to 0 V and $V_{\rm DS} = 10$ V) for the oxide-filled and mesa-isolated devices with postgate annealing, respectively. The gate leakage current of the oxide-filled isolation structure also improves significantly compared with that observed in previous studies [18], [19]. It is worth mentioning that the gate leakage level obtained here is comparable and even lower than that in the devices using the MIS-HEMT structure with an additional dielectric layer [8]–[10]. It should also be mentioned that the measured leakage current at the source terminal is very small ($< 10^{-11}$ A/mm), which implies that the drain-to-source leakage through the buffer layer and/or from the oxide-filled region is insignificant. The similar levels of the gate and drain leakages also suggest that the gate leakage current is the main contributor to the observed leakage from the drain terminal. Fig. 3 shows the normalized flicker noise current spectral densities $S_{\rm id}/I_D^2$ of both device structures in the linear region ($V_{\rm GS} = 0$ V and $V_{\rm DS} = 0.1$ V). The result clearly indicates that the oxide-filled design presents a lower noise level compared with the traditional mesa-isolated device. Since flicker noise is related to the defects in the devices, the results also indicate that the oxide-filled isolation design is effective to mitigate the trapping effect in GaN HEMTs.

The fundamental ideas of oxide filled and postgate annealing are somewhat different, and yet, both of them can reduce the leakage current. The oxide-filled process levels the gate finger tips with the mesa to avoid the trap-rich mesa edge. On the other hand, the postgate annealing process can recover the damaged surface area by hydrogen diffusion [21], [22]. Since the etching damage is more severe in the mesa-edge region, it is relatively more difficult to be recovered by hydrogen diffusion. With the oxide-filled process, the mesa edge is filled up, and this problem can be prevented, and thus, an extremely low leaking level can be observed. If the devices are treated only with the oxide-filled process, the mesa-edge traps can be avoided, whereas the traps in the rest of the active area are still a problem. For the devices with oxide-filled isolation followed by postgate annealing, hydrogen diffusion at the mesa edge may not be as effective. However, as explained earlier, it is not that critical anymore. The results suggest that both the oxide-refilled design and the forming gas treatment are important factors to the observed low leakage current and the reduced trapping effect.

IV. Conclusion

In this letter, we have proposed an oxide-filled isolation structure followed by postgate annealing to alleviate the trapping effect and reduce the leakage current in GaN HEMTs. The devices showed the leakage current level to be as low as 10^{-9} A/mm, which was about three orders of magnitude smaller than the typical reported values. An extremely high ON/OFF current ratio that is up to 1.5×10^8 was obtained. The reduced flicker noise level in the oxide-filled GaN HEMTs also indicated alleviated trapping effects, which was consistent with the observed low leakage current.

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