2.07-kV AlGaN/GaN Schottky Barrier Diodes on Silicon With High Baliga's Figure-of-Merit

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***Abstract*— In this letter, we demonstrate high-performance AlGaN/GaN Schottky barrier diodes (SBDs) on Si substrate with a recessed-anode structure for reduced turn-on voltage V_{ON}. The impact of the surface roughness after the recessed-anode formation on device characteristics is investigated. An improved surface condition can reduce the leakage current and enhance the breakdown voltage simultaneously. A low turn-on voltage of only 0.73 V can be obtained with a 50-nm recess depth. In addition, the different lengths of Schottky extension acting like a field plate are investigated. A high reverse breakdown voltage of 2070 V and a low specific ON-resistance of 3.8 m$\Omega \cdot$cm^2 yield an excellent Baliga's figure of merit of 1127 MW/cm^2, which can be attributed to the low surface roughness of only 0.6 nm and also a proper Schottky extension of 2 μm to alleviate the peak electric field intensity in the SBDs.**

***Index Terms*— GaN, Schottky barrier diode (SBD), silicon substrate, Baliga's figure-of-merit.**

I. Introduction

THE SCHOTTKY barrier diode (SBD) is an essential component in many power conversion systems. With the increased demand for a small form factor in various power electronics applications, it is an inevitable trend to increase the operating speed of the devices and circuits. However, this also poses a great challenge of maintaining high power conversion efficiency. Recently, the GaN-based SBDs have attached significantly attention for high power and high speed applications due to the excellent material property such as high carrier density, high electron saturation velocity, and high breakdown voltage (V_{BK}) [1]–[5]. Also, recent progress in technology allows the GaN epi structure to be grown on large silicon substrates, making it realistic to achieve low-cost and high-performance GaN SBDs for power applications [6]. One issue remains for the GaN SBD is the relatively high turn-on voltage V_{ON} owing to the wide bandgap nature of the material, which can increase the conduction loss and seriously degrade the efficiency of circuits and systems.

Various approaches have been proposed to reduce V_{ON} of AlGaN/GaN SBDs, which is $\sim$1$-$1.3 V in typical devices. Table I summarizes recent advances of GaN SBDs on different substrates. The field effect Schottky barrier diode (FESBD) demonstrated a low V_{ON} of 0.63 V using a Schottky-gate-controlled 2DEG technology [1]. A gated ohmic structure was proposed to reduce the turn-on voltage from 1.05 V to 0.37 V without breakdown voltage degradation [2]. A selective Si diffusion approach was proposed to simultaneously improve V_{ON} from 1.3 V to 1 V and V_{BK} from 1250 V to 1500 V [3]. Also, a fully recessed anode structure with a dual field plate featured a high breakdown voltage of 1.9 kV was reported [4]. Among the different approaches, the recess technology is an effective way to reduce V_{ON} while maintaining high reverse blocking capability. By employing the recess process in GaN SBDs, one important issue is the understanding and control of the surface condition of etching. Studies reported that the surface roughness after the recess process is critical to the device characteristics [7]–[10]. A high contact roughness may result in a rapid increase of the channel/buffer leakage current and premature breakdown.

TABLE I
RECENT ADVANCES OF AlGaN/GaN SBDs ON DIFFERENT SUBSTRATES

Ref.	Substrate	V_{ON} (V)	L_{AC} (μm)	V_{BK} (V)	$R_{ON,SP}$ (m$\Omega\cdot$cm^2)	B-FOM (MW/cm^2)
[14]	Sapphire	0.8	20	747	12	47
[13]	Sapphire	--	30	765	81.3	7.2
[12]	SiC	0.43	8	1000	0.45	2222
[11]	Si	0.5	15	800	3	213.3
[4]	Si	0.67	25	1900	5.12	727
[3]	Si	1	15	1500	3.37	666.7
[2]	Si	0.37	18	1440	--	--
[1]	Si	0.63	10	390	1.4	108
This work	Si	0.73	21	2070	3.8	1127

In this letter, we focus on the investigation of surface condition after the recessed-anode formation of GaN-on-Si SBDs. The results show how the surface roughness can affect both forward and reverse characteristics for a fully recessed structure, which has not been discussed in the previous publications. Using a relatively simple structure but optimized surface condition and proper field plate design, the achieved B-FOM of 1127 MW/cm^2 is among the highest compared with the published GaN-on-Si SBDs.

II. Device Structure and Fabrication

The epitaxial layer as shown in Fig. 1 was grown by MOCVD on a low resistivity silicon substrate. The device layout is circular type, which is defined by R (radius of Schottky metal), L_{ext} (extended length over the recess edge),

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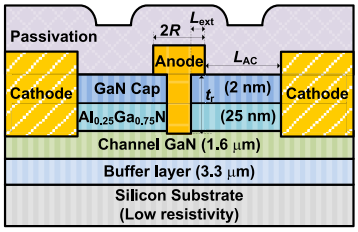


Fig. 1. Cross section of the AlGaN/GaN SBDs on silicon substrate.

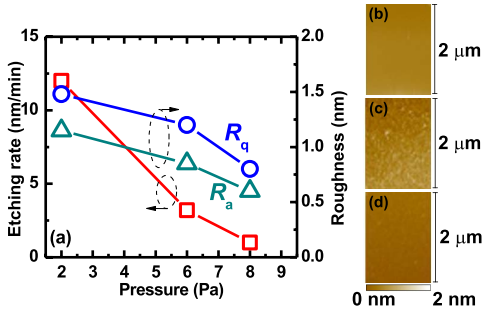
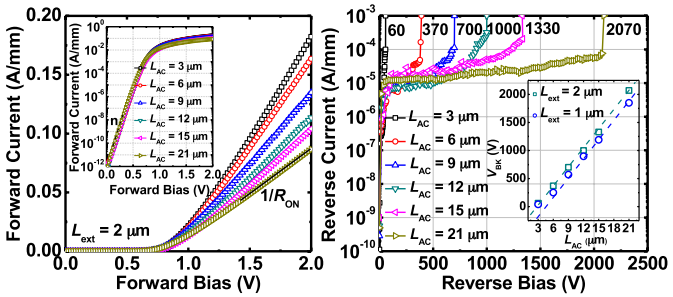


Fig. 2. (a) Measured etching rate and surface roughness of the tested recipes versus different pressures, and the AFM images of (b) the as-grown surface (c) after pressure of 6 Pa etching (d) after pressure of 8 Pa etching.

t_r (etching depth of the recessed anode), and L_{AC} (the distance between anode and cathode). The ohmic contact (Ti/Al/Ni/Au) was first fabricated with a recess depth of 30 nm, followed by rapid thermal annealing at 800 °C for 30 s in N_2 ambient. Note that the recessed ohmic contact of 30-nm allows the TiN contacting the 2DEG channel directly after high temperature annealing, resulting in enhanced carrier tunneling and reduced contact resistance [15]. After the ohmic contact formation, mesa isolation was done by using dry etching with Cl_2/Ar mixture gas. A pattern was developed for the recessed-anode process using various recipes to obtain low surface roughness by the ICP-RIE. Fig. 2(a) presents the etching rate and surface roughness (RMS/average roughness R_q/R_a) vs. pressure, which indicates that the etching rate reduces with increased pressure. At higher pressures, the mean energy of ion bombardment becomes lower due to the increased collisions. As a result, the reduced etching rate leads to improved surface roughness [16]. The finally selected recipe is with a Cl_2 flow of 20 sccm, an ICP power of 30 W, a RF power of 10 W (50 V_{p-p} producing V_{DC} of -1 V), and a pressure of 8 Pa, yielding an etching rate of 1 nm/min. Before recess etching, the R_q/R_a is 0.4 nm/0.25 nm for the as-grown surface, as shown in Fig. 2(b). The R_q/R_a becomes 1.2 nm/0.85 nm and 0.8 nm/0.6 nm after etching with the applied pressures of 6 Pa and 8 Pa, respectively (Fig. 2(c) and 2(d)). The Schottky metal stack of Ni/Au (40 nm/350 nm) was then deposited, followed by a passivation of $SiN_x/SiO_x/SiN_x$ using PECVD at 300 °C. The contact resistance R_c of 0.53 $\Omega\cdot$mm and sheet resistance R_{sh} of 428 $\Omega/\square$ were obtained by the transmission line method after passivation.

III. Results and Discussion

Fig. 3(a) and 3(b) show the measured I–V characteristics of the SBDs ($t_r = 50$ nm) with various anode-to-cathode distances ($L_{AC} = 3 - 21$ μm; $L_{ext} = 2$ μm and $R = 50$ μm)



(a) (b)

Fig. 3. I–V characteristics of the SBDs (a) forward bias and (b) reverse bias.

in forward and reverse characteristics, respectively. Note that the fully recessed anode enables the Schottky metal to contact the 2DEG along with an increased tunneling probability (with a thin barrier in the range of 4 – 10 nm), which results in a reduced V_{ON} without degradation of reverse leakage [17]. Fig. 3(a) shows that the high forward currents of 104 and 86.5 mA/mm for $L_{AC} = 15$ and 21 μm (at a forward bias of 2 V) are achieved, respectively. As shown in the inset of Fig. 3(a), an excellent on/off ratio up to $\sim 10^{11}$ can be obtained. Also, the extracted ideality factor n and V_{ON} (at a forward current of 1 mA/mm) are 1.18±0.01 and 0.73±0.01 V, respectively. The corresponding barrier height $q\phi_B$ is 0.6±0.01 eV. The small variations indicate an excellent Schottky junction uniformity of the devices with different L_{AC}. By using the area of active region including a 2-μm transfer length of ohmic contact and a 2-μm Schottky extension length, the specific ON-resistance $R_{ON,SP}$ can be calculated as 2.2 and 3.8 m$\Omega\cdot$cm^2 for devices with L_{AC} of 15 and 21 μm, respectively. Fig. 3(b) shows the reverse I–V characteristics of devices with various L_{AC}. The Schottky metal extension forms a Γ-shaped electrode and acts similar to a field plate to alleviate the peak electric field intensity. Note that the field plate structure is typically fabricated on top of the passivation layer to take advantage of the e-field redistribution and increased insulator thickness for enhanced breakdown voltage. The length of extension could also be critical to the breakdown voltage [18]. Compared with the GaN SBDs also using the recessed-anode structure [4], [12], we propose a relatively simple structure with the Schottky metal extension directly realized on top of the GaN cap layer (see Fig. 1), which eases the requirement of high quality passivation layer and additional process steps for the field plate structure. Considering the surface-induced trapping effect with the Schottky metal extension, it has been revealed that the impact becomes obvious as L_{ext} exceeds ~4–5 μm [19]. Therefore, the extension of only ~1–2 μm here should not have a significant effect on the device characteristics.

As aforementioned, the surface condition of etching is very important to the recessed structure for optimized device performance. Fig. 3(b) shows that an excellent reverse breakdown voltage up to 2070 V for $L_{AC} = 21$ μm can be achieved, which is an evidence of the high quality surface condition after recess process. The inset of Fig. 3(b) shows the linearly increased breakdown voltage versus L_{AC} with two different L_{ext} of 1 and 2 μm. With an appropriately designed L_{ext},

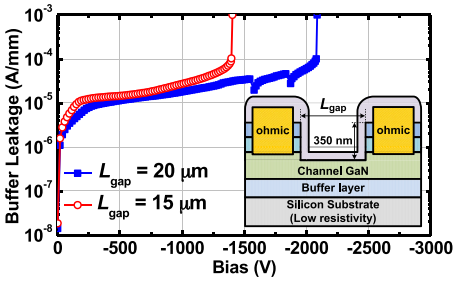


Fig. 4. Measured buffer leakage with the test patterns.

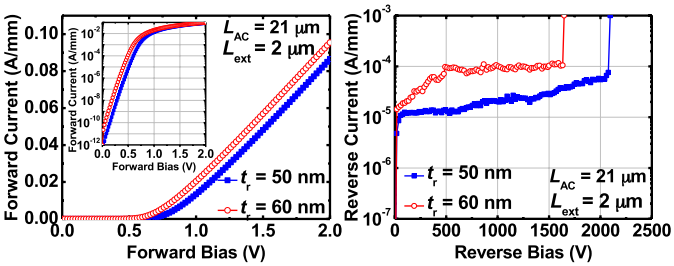


Fig. 5. Comparison of I–V characteristics of the SBDs with 50-nm and 60-nm etching depths (a) Forward bias and (b) reverse bias.

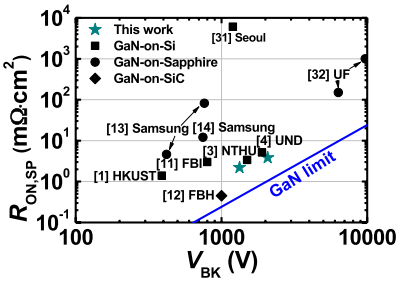


Fig. 6. Benchmark plot of V_{BK} versus $R_{ON,SP}$ for lateral GaN-based SBDs on different substrates.

a complete pinch-off characteristic for the 2DEG channel can prevent degradation of the leakage current and breakdown voltage. A noticeable improvement of V_{BK} of 12.5% for devices with $L_{ext} = 2\ \mu$m ($L_{AC} = 21\ \mu$m) is obtained, compared with that for L_{ext} of 1 μm. The effective critical electric field ($E_{cr,eff}$) can be calculated in a range of 1.1−1.4 MV/cm. It is worth mentioning that V_{BK} still increases proportionally with L_{AC} even up to 21 μm (the maximum value used in this design).

Although a high breakdown voltage is achieved, the leakage current is relatively large in the SBDs. To investigate the origin of leakage current, the test pattern with removed 2DEG channel [20] (inset of Fig. 4) was also fabricated in the same process. The similar leakage levels between the test pattern and the SBD (see Fig. 3(b)) suggest that the buffer leakage is the main contributor to the observed reverse leakage in the SBDs. Without an additional dielectric layer for MIS structure [21] or gated edge termination [22], it should be pointed out that the fabricated devices exhibit a similar leakage level compared with recently reported GaN-on-Si SBDs [2], [11], [21], [22]. It was suggested that the nonalloyed ohmic contact using regrown n^+ GaN can suppress the leakage current [20]. Also, the improved buffer structure by a high-resistivity [23] or an even thicker [24] layer has been reported to effectively reduce the vertical leakage current. Note that the surface roughness related to the defect density and the trap activation energy could exacerbate the trap-assisted tunneling (TAT) process, which is an important leakage mechanism associated with thermally activated reverse current [17], [25]–[27]. As presented in this letter, we obtain a low surface roughness in the etching process, which is expected to alleviate the TAT process and leakage current degradation at high temperatures.

To further prove the impact of the surface roughness on device performance, the devices of two etching depths (50 vs. 60 nm) along with different surface roughnesses (R_q/R_a = 0.8 nm/0.6 nm vs. R_q/R_a = 1.2 nm/0.8 nm) are demonstrated. As shown in Fig. 5(a), the 50-nm SBD exhibits a slightly higher V_{ON} of 0.73 V compared with 60-nm SBD (V_{ON} = 0.6 V). The increased V_{ON} with less surface roughness can be attributed to the increased $q\phi_B$ (from 0.52 to 0.6 eV), resulting from less surface states and alleviated trapping effects. The trend is consistent with previously reported results with improved surface condition [28], [29]. Also, the 60-nm device shows a degraded ideality factor of 1.27, which also agrees with the observed higher surface roughness. This may also explain the devices with a low V_{ON} of 0.43 V but a relatively large n of 1.76 [12]. Fig. 5(b) shows that improved surface roughness exhibits an obvious leakage current suppression together with an improved V_{BK} up to 26% (from 1640 to 2070 V; $L_{AC} = 21\ \mu$m).

Fig. 6 plots the benchmark of V_{BK} versus $R_{ON,SP}$ for various GaN-based power diodes. Owing to the optimized surface condition and proper design of field plate, the proposed devices with a recessed anode demonstrate the highest V_{BK} and best FOM, compared with other SBDs on silicon. Also, our devices show a comparable performance to the SBDs grown on the SiC substrate. Considering the more pronounced lattice and thermal mismatches, it is more challenging to realize high performance GaN SBDs on silicon than SiC [23], [30]. Nevertheless, as compared to the SiC substrate, growing GaN on a large-scale Si substrate has great advantages such as significant cost reduction and the opportunity of integration with existing advanced Si technology. It should be mentioned that the superior FOM obtained in [12] could be mainly attributed to the higher effective critical e-field for the GaN-on-SiC device compared with that of GaN-on-Si substrate.

IV. Conclusion

In this letter, the fully recessed AlGaN/GaN SBDs on silicon substrate with an excellent Baliga's FOM have been demonstrated. The devices with different surface roughnesses indicated that an improved etching surface could effectively suppress the leakage current and enhance the breakdown voltage. Also, the test pattern suggested that the buffer leakage is the main contributor to the observed reverse current in the presented GaN-on-Si SBDs. The recessed anode can effectively lower the V_{ON} to be only 0.73 V while maintaining a high reverse blocking capability. Owing to the low roughness of only 0.6 nm and a properly designed L_{ext} of 2 μm acting as

a field plate, a high reverse breakdown voltage of 2070 V with a low $R_{ON,SP}$ of 3.8 m$\Omega\cdot$cm^2 can been obtained. The achieved B-FOM of 1127 MW/cm^2 is among the highest compared with the published GaN-on-Si Schottky barrier diodes.

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