A De-embedding Method for Extracting S-Parameters of Vertical Interconnect in Advanced Packaging

[1,2]Yin-Cheng Chang, [1]Shawn S. H. Hsu, *Member, IEEE*
[1]Institute of Electronics Engineering
National Tsing Hua University
Hsinchu, Taiwan
ycchang@cic.narl.org.tw

[2]Da-Chiang Chang, [2]Jeng-Hung Lee, [2]Shuw-Guann Lin, and [2]Ying-Zong Juang
[2]Chip Implementation Center
National Applied Research Laboratories
Hsinchu, Taiwan

***Abstract*—An extracting methodology is proposed to characterize the performance of interconnect. This work successfully extracts the interconnect by using transmission matrix (T-matrix) for calculation. This method exhibits its validity without frequency limitation mathematically. It can deal with most kinds of vertical interconnects including bond-wires, micro-bumps and through-silicon-vias (TSVs). Details of equations and measurement procedure are reported in this work. The bump in flip-chip process is taken as an example. The analysis is depicted and the measured results are performed for verification up to 20 GHz.**

Keywords-extraction; de-embedding; interconnect; bump; TSVs.

I. INTRODUCTION

For high density and high operating frequency demand, high performance packaging technologies like System-in-Package (SiP) and 3D-ICs become more and more popular. Accompany with the quality of their interconnects, such as the bond-wires, micro-bumps and TSVs becomes more and more critical, because of the effect they contribute to the system. While lots of the improved technologies were proposed to keep these parasitic low [1]-[2] and various mature characterizations [3]-[6] were presented to extract and model bond-wires, vias, devices, and transmission lines in different applications, there is a relative low amount of literature were published to focus on the de-embedding method of the interconnects.

In [7], four different measurement approaches were used to extract the parasitic inductance of TSV. They applied the Line-Reflect-Reflect-Match (LRRM) calibration to shift the reference planes to the test structures firstly. Then take the advantage of measuring the resonance frequency after adding series or shunt resonators. The constant inductance of TSV can be derived eventually by summarizing various test structures which consisted of resonators. Except for the half wavelength resonator approach, the measured results from the other approaches would be sensitive to the probe placement and the calibration accuracy. And only an inductance value was extracted, such a single lumped model may be insufficient for high frequency prediction. Leung [8] proposed a simple short structure and utilized the half wavelength approach to build up an accurate equivalent-circuit model, which composed of not only the inductance but the resistance, of the through wafer interconnect (TWI) up to 20GHz. A minor concern is the applicable bandwidth of the half wavelength structure which is frequency dependent. And the extracted S-parameter is from the one-port measurement which can not be directly used in the circuit simulation. Ryu [9] proposed an advanced two-port model which composed RLCG components. The extracted parameters are much useful for RF circuit integration. Their unique measurement is to place one probe on the top of via directly and place the other probe on the CPW line which is connected to the bottom side of via. The via can be extracted from a simple de-embedding method like port extension or (Through-Reflect-Line) TRL. This method is simple and straightforward, but will face difficulty if the interconnect under test, like the bumps in the flip-chip process, can not be contacted directly.

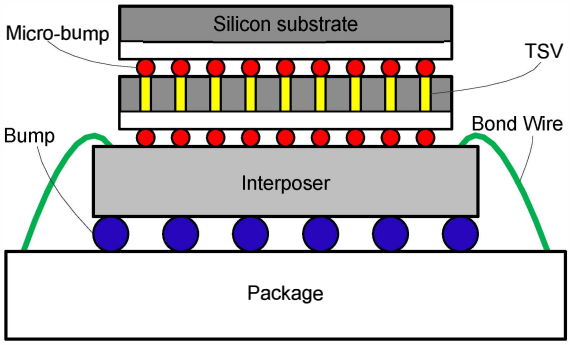


Figure 1. Typical vertical interconnects in advanced packaging technologies.

The most straightforward method to obtain the two port S-parameter of an interconnect is to contact microwave probes at two ends of the interconnect directly. In practice, there are some tasks have to be overcome. Take the TSV for example, the two ends of TSV are not at the same plane, but most developed testing facilities, probe stations, were designed to deal with the issues at the same plane nowadays. Therefore, one interesting idea is to raise the wafer to a vertical position, and then move the horizontal probes to land on two ends of the TSV on two sides. In this solution, the wafer handler might be a task to be solved. And it faces a further difficulty; all the testing results could be meaningless without calibration. A set of double side calibration kits with well-defined standards is the way to realize calibration. But it might become a customized product, the process of implementation and the expense could be the problems before mentioning its accuracy.

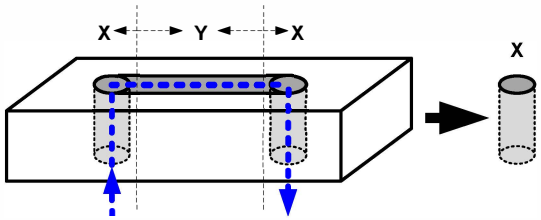


Figure 2. Vertical interconnect with horizontal track in the de-embedding method.

Another idea based on the existing planar calibration is try to land one probe on the top side of TSV and flip another probe to the bottom side of the wafer to make contact. The other idea is to lift both the probe positioners and the wafer to be vertical after a regular planar calibration, and then make contact on the TSV. The latter two solutions could be feasible without needing a new calibration standard under developed. But they remain the risk of suffering from high uncertainty during moving the probe positioners after calibration. For these reasons, the 3D testing was put away in this paper and turned the testing solutions back to the indirect extraction.

In this paper, a de-embedding methodology for extracting two-port S-parameters is proposed. A case of the bump in flip-chip process is utilized as an example. But this method can deal with most kinds of interconnects including bond-wire, micro-bump and TSV with certain purposely designed structures. The following sections depict the method and the experiment results verify the feasibility.

II. METHODOLOGY

A certain structure as shown in Fig. 2 is proposed to assist the idea of extracting the characteristic of interconnect. According to the signal path, signal flows into the left side interconnect from bottom layer, then passes through the track on the top layer. And it eventually goes back to the bottom layer by right side interconnect. Therefore, the structure can be seen as three elements cascaded in a row. In this configuration, the T-matrix was chosen for analysis. Because the T-matrix is more suitable for calculating cascaded elements than other transformations of S-parameters. With the representation of X and Y denote as the vertical interconnect and the horizontal track between interconnects respectively, the equations can be described as below.

$$T1 = Y \tag{1}$$

$$T2 = X \cdot Y \cdot X \tag{2}$$

where T2 represents the structure as shown in Fig. 2. And if the track, T1, can be defined, the unknown X can be derived by solving (1) and (2) as below,

$$T2 \cdot T1 = XYX \cdot Y \tag{3}$$

$$\sqrt{T2T1} = XY \tag{4}$$

$$X = \sqrt{T2T1} \cdot Y^{-1} \tag{5}$$

Eventually, the parameter of interconnect could be extracted. For confirming this method, an assumed equivalent model proposed in [9] of interconnect was applied to represent

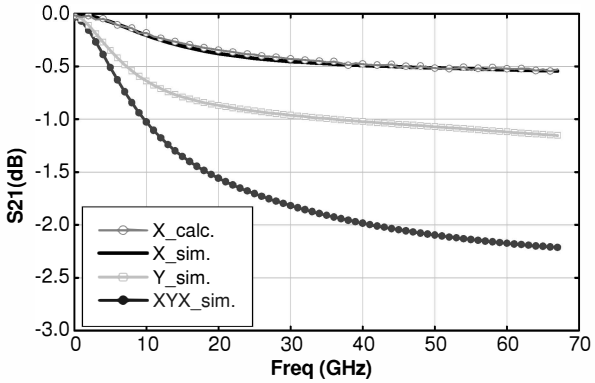
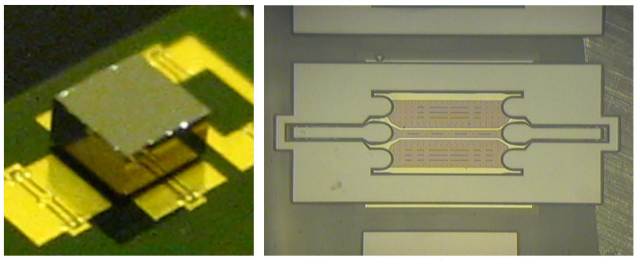


Figure 3. Validity of the methodology from verifying the insertion losses.



(a) (b)

Figure 4. Photos of the flip-chip technology: (a) near view, (b) bottom view (from glass substrate side).

the X. And a transmission line was utilized to describe the track Y. From (5), the results of insertion loss (S21) are calculated and shown in Fig. 3. The solid line without symbol represents the simulated result of the interconnect. And the calculated result shows a well agreement with it. It depicts this method can extract the interconnect from the whole structure successfully. And it is valid without frequency bandwidth limitation mathematically. This methodology can be applied in any technology with vertical interconnects that be able to form the configuration as shown in Fig. 2. The following section depicts the detailed procedures and the design of de-embedding patterns.

III. EXPERIMENTAL PROCEDURE AND RESULTS

A well developed flip-chip technology is adopted to demonstrate the whole experiments in this work. The heterogeneous integration technology connects the standard TSMC 1P6M 0.18 um CMOS process and the glass integrated passive device (GIPD) process by using Sn/Ag bumps as the interconnects. The CMOS chip as the top layer die was flipped and bonded on the bottom glass substrate and formed a face-to-face configuration as shown in Fig. 4. The coplanar waveguide (CPW) structure was chosen and applied in the experiments thoroughly because of the ground reference concern and its popular usage in RF or microwave integration. Besides, the ground-signal-ground structure with well-defined characteristic impedance of 50 ohms makes all transitions under control. Unlike the low frequency solution in board level uses the microstrip-via-microstrip structure; the vertical via suffers from varied transition of the ground reference would cause unexpected effects at high frequency. The full wave em simulation of the patterns in this work was performed by ADS

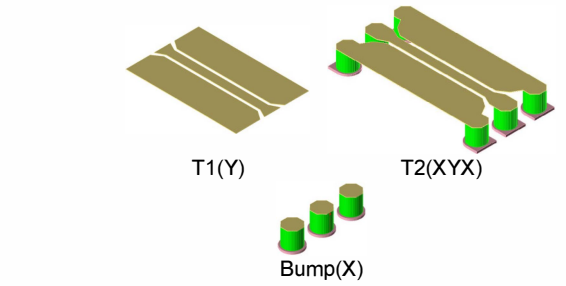


Figure 5. The representation of T1, T2 and bump.

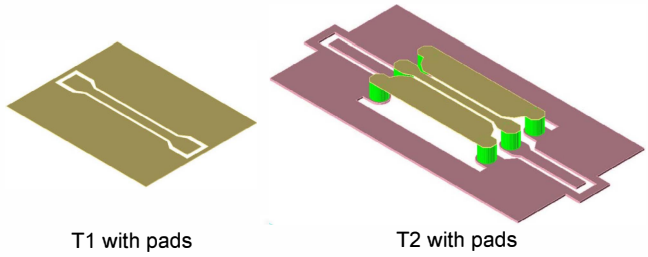


Figure 6. T1 and T2 with probing pads.

MOMENTUM™. And the vector network analyzer used in this work is Agilent PNA N5230A with the measurement capability of 300KHz-20GHz.

Based on the derivation in last section, in order to extract the parameter of the bump, the characteristics of structure T1 and T2 have to be obtained previously as shown in Fig. 5. And all the measurements are on-wafer testing, which means some probing pads extended from T1 and T2 are needed for testing as shown in Fig. 6. The extended pads can be calibrated out by TRL or other fundamental de-embedding methods to shift the measurement reference planes to the desired position. The result as shown in Fig. 7 and 8 indicates the T1 and T2 were extracted out from the probing pad. And the simulated results meet high agreement with the measured results. The slight difference between extracted result and simulated result comes from the em environment and substrate parameters setting.

After T1 and T2 were extracted, transform these two parameters to T-matrix for implementing the equation (5) mentioned in last section. Fig. 9 shows the characteristic of bump are extracted out from a series of de-embedding procedure. The extracted result of the bump is also compared to the em simulation. The measured insertion losses of T2(XYX), T1(Y), and the extracted bump(X) are 1.41dB, 0.88dB, and 0.26dB at 20GHz, respectively. The results show a well consistence and validity of the proposed de-embedding method.

IV. Conclusion

A de-embedding methodology is proposed and proved to have the ability of extracting the interconnect by using T-matrix calculation. The simulation verifies the validity over a wide frequency range without limitation. With some certain purposely designed patterns, this method can be applied in most kinds of interconnects in advanced packaging. The bump in flip-chip process as the example is demonstrated to verify

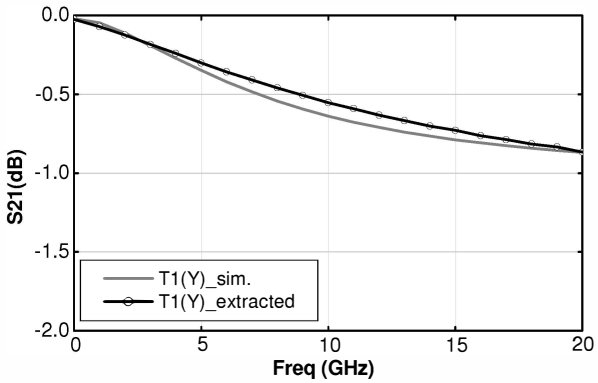


Figure 7. Comparison of the insertion losses between simulation and measurement for T1.

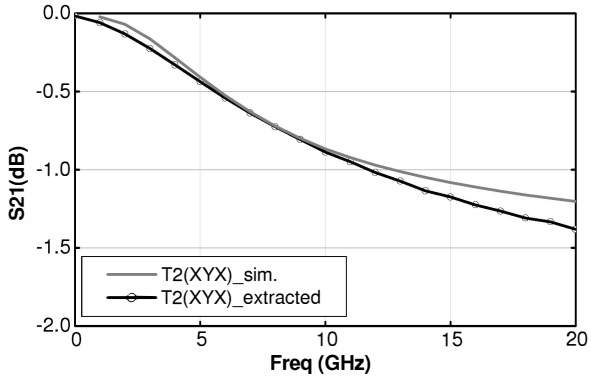


Figure 8. Comparison of the insertion losses between simulation and measurement for T2.

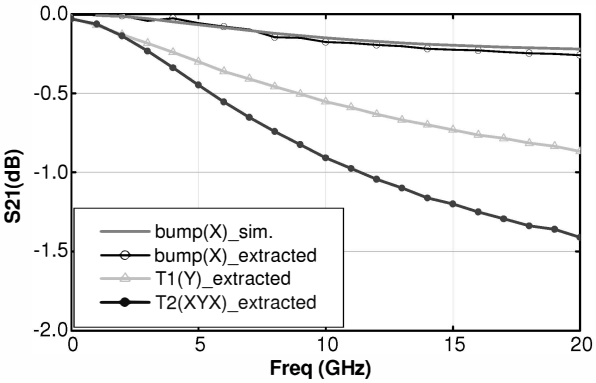


Figure 9. Comparison of the insertion losses in de-embedding procedure.

this procedure. In this work, the experiment investigates the S21 of the bump up to 20GHz with high accuracy.

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