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RF Modeling of Through Silicon Vias (TSVs) in 3D IC

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1. Introduction

As the size of transistor keeps shrinking, advance of CMOS technology becomes more difficult and will eventually reach the physical limitation. To continuously reduce the form factor of the system with multiple chips, one straight forward solution is using stacked dies, called three-dimensional integrated circuits (3D IC). Recently, the technology of Through Silicon Vias (TSVs), developed mainly for realizing 3D IC, attracts much attention. For the design of 3D IC using TSV, the electrical characteristics and the associated SPICE model of TSVs play extremely important roles. The studies of TSV test structures and RF modeling have been reported [1]-[2]. Differing from the conventional planar IC, it is rather difficult to avoid the undesired parasitics in direct on-wafer measurement for the 3D test structure. Therefore, accurate RF modeling of the TSV, involving the test structure design and parameter extraction, is still an issue and need to be studied further.

In this paper, we propose an effective approach for designing the TSV test structures and extracting the equivalent circuit model parameters. The one-port test structures, consuming only a small chip area, are employed to solve the difficulty encountered in the typically used two-port methods. The proposed equivalent model, which composed of *R*, *L*, *C*, and *G*, is based on the physical structure of the TSV and is verified up to 50 GHz. The parameters calculated using the analytical equations confirmed that the proposed approach leads to a well-defined physical-based model.

2. One-Port Test Structures and Parameters Extraction

Fig. 1 shows the cross section of the TSV technology used in this study with a face-to-back structure. As can be seen, the top metal and vias are both made of copper and the TSV is surrounded by a thin layer of SiO_2 liner for isolation. Note the structure is provided from an IC foundry, and the detailed geometrical parameters cannot be disclosed.

For RF modeling of TSV, it is necessary to have well-defined test patterns for parameter extraction. The two-port structure is often used for RF device modeling [3]. However, it is difficult to obtain the intrinsic properties of the TSV using the two-port structure. As can be seen from Fig. 1, since the probing pads for both ports are on the top, the two TSVs need to be connected by an additional bottom metal line. The additional element complicates the de-embedding produce and makes it difficult to extract the intrinsic TSV parameters. In this study, the one-port design, which not only makes the chip area smaller but also simplifies the parameter extraction method, is used for the RF test structures.

Fig. 2 shows the proposed ground-signal-ground (G-S-G) one-port testing structure for the open and short, respectively. Since the process is still on progress, these structures are implemented by EM simulation, and the results are used to emulate the experimental data for the following analysis. After the de-embedding procedure for the RF pads (also by EM modeling), the intrinsic open structure can be simplified as only the shunt elements of the conductance *G* and capacitance *C* by neglecting the parasitic *R* and *L* of the TSVs. On the other hand, the proposed short-circuit structure, which is similar to a daisy chain, can be simplified as only the serial elements of *R* and *L* in the equivalent circuit mode [4]. It is worth mentioning that the proposed one-port daisy chain structure is useful and rather unique for determining the serial parasitic elements *R* and *L* with very small values. The added parasitic resistance and inductance can be measured more precisely by the daisy chain structure. In addition, the one-port structure allows very short distance between the two TSVs and thus negligible bottom metal lines. Therefore, it can resolve the difficulty of parameter extractions and also the required large chip area if using two-port daisy chain.

Fig. 3 shows the equivalent circuit model of the TSV in the G-S-G configuration. The TSV inductance *L* and resistance *R*, and R_1, R_2, and L_r for describing the skin effect can be extracted by the short-circuit test structure. Also, the oxide capacitance C_{ox}, silicon substrate capacitance C_{si} and the corresponding conductance G_{si} can be obtained from the open-circuit test structure [5]. All the extracted parameters are listed in Table I.

3. Parameters Verification Using Analytical Equations

To ensure the extracted parameters are physical-based, the analytical equations are also employed to verify the established equivalent circuit model. For example, the inductance per unit length of the TSVs can be determined by integrating the magnetic field among the three TSVs:

$$\Delta L = 2 \cdot \frac{\Phi}{I} = 2 \cdot \int_r^{d-r} \left[\frac{\mu}{2\pi x} + \frac{\mu}{4\pi(d-x)} - \frac{\mu}{4\pi(d+x)} \right] dx \qquad (1)$$

where μ is the permeability, d is the via pitch, r is the via radius, Φ is the magnetic flux, and I is the current. The capacitances in the model can also be determined analytically. For the liner oxide layer around the TSVs, the associated C_{ox} can be estimated using the equation below:

$$C_{ox} = \varepsilon \cdot \frac{\pi r l}{t_{SiO_2}} \qquad (2)$$

where ε is dielectric constant of silicon dioxide, and t_{SiO2} is the thickness of the silicon dioxide. Since the multiplication of ΔL and ΔC (per unit length) in a transmission line must be constant, the silicon substrate capacitance C_{si} in the model can be obtained from the following equation:

$$\Delta L \cdot \Delta C = \mu\varepsilon_{eff} \tag{3}$$

where the effective dielectric constant ε_{eff} can be calculated based on the TSV structure. Note the ΔC here includes C_{ox} and C_{si} connected in shunt. With L and C_{ox} calculated from (1) and (2), respectively, C_{Si} can be determined from (3). Based on the physical structure, the analytical equations can also be found to determine the parasitic resistance R and G in the model. The calculated parameters are also shown in Table I, which show excellent agreement with those parameters extracted directly from the test patterns.

Fig. 4 compares the S-parameters obtained from the test structure extraction, the analytical equations, and the EM simulation. Note the extract parameters are employed directly without any further optimization. The differences of S_{21} and S_{11} between the EM simulation and the equivalent circuit model are smaller than 0.03 dB and 2 dB, respectively from 1 GHz to 50 GHz. The associated standard errors of S_{21} and S_{11} are 0.05% and 0.95%; and those are 0.18% and 2.32% for the results between the EM simulation and analytical equations.

4. Conclusion

In this study, we proposed a new approach using one-port testing structures to establish the equivalent circuit model of TSVs for 3D IC. Compared with the conventional two-port method, the proposed test structures consumed only a small chip area, and the small serial parasitic elements in the model can be extracted precisely. In addition, the analytical equations were used to verify if the model agrees the physical structure of the TSV. The S-parameters obtained from the EM simulation, the extract model parameters, and the analytical equations showed excellent agreements up to 50 GHz.

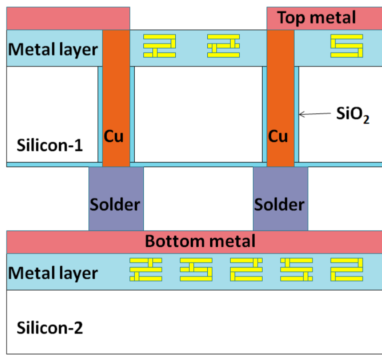
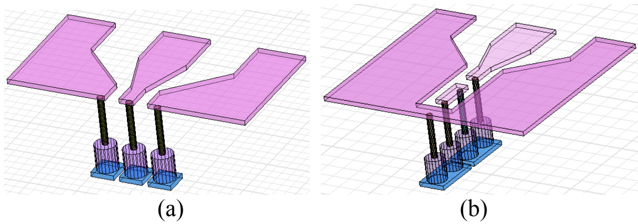


Fig. 1. Cross section of the TSV structure.


(a) (b)
Fig. 2. One-port test structures of (a) open (b) short.

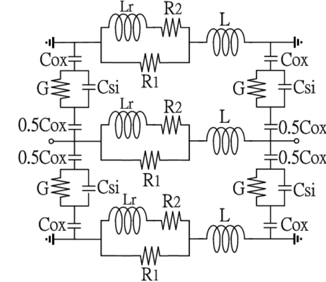


Fig. 3. Equivalent circuit model of G-S-G TSV structure.

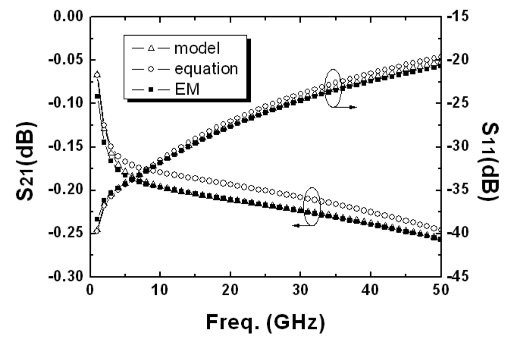


Fig. 4. Comparison of S_{11} and S_{21} obtained by three methods.

Table I Equivalent Circuit Model Parameters of G-S-G TSV Sturcture.

Parameters	R_1	R_2	L_r	L	C_{ox}	C_{si}	G
Test structures	269.79 mΩ	39.75 mΩ	4.24 pH	55.06 pH	80.55 fF	2.60 fF	0.26 mS
Analytical equations	231.92 mΩ	35.01 mΩ	2.10 pH	60.44 pH	81.36 fF	3.01 fF	0.25 mS

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