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Layout Optimization of AlGaN/GaN HEMTs for High-power Applications

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1. Introduction

High performance AlGaN/GaN high electron mobility transistors (HEMTs) have been successfully employed for high power applications owing to the excellent characteristics of GaN such as its wide bandgap, high breakdown field, and high saturation velocity [1]. With a high breakdown voltage (V_{BK}), the transistors are allowed to be biased at very high voltage to achieve high power performance. However, the device reliability can be a critical issue under such harsh conditions. It has been reported that the current collapse and gate-lag effects are closely related to the interface/surface traps existed in GaN-based FETs, which can cause device degradation during operation [2]. Previous studies focused on approaches such as surface passivation and field plates to suppress these effects [3]-[4]. In this work, a square-gate layout is proposed to achieve high breakdown voltage and ensure the device reliability simultaneously. Compared with the conventional multi-finger layout, the proposed design presents significantly smaller current collapse and gate-lag effects. In addition, increase of the breakdown voltage of more than ~ 80 V, and reduction of the off-state leakage current for more than one order of magnitude are also observed. The devices achieve an excellent breakdown voltage up to ~ 500 V without using the field-plate structure.

2. Device Design and Fabrication

The cross section of the modulation-doped AlGaN/GaN heterostructure grown on sapphire substrate is shown in Fig. 1. The measured sheet electron concentration and electron mobility at room temperature were 1.12×10^{13} cm^{-2} and 1340 cm^2/V-s, respectively. Device isolation was achieved by dry etching using Cl_2/Ar gas mixture, and the source/drain ohmic contacts were then formed with Ti/Al/Ti/Au by rapid thermal annealing at 750°C for 30 seconds in a N_2 ambient. The alloy Ni/Au was deposited to form the schottky gate. Finally, a silicon nitride layer was deposited for surface passivation.

Fig. 2 shows the layouts of the traditional multi-finger device, and the proposed square-gate configuration, respectively. For both devices, the gate length is 2 μm and the source to drain spacing L_{gs} is 2μm. A longer gate-to-drain spacing L_{gd} ranging from 8 μm to 16 μm (4 μm/step) was employed as the drift extension region to enhance the breakdown voltage. The overall width of the devices is 600 μm. For The multi-finger design as shown in Fig. 2 (a), breakdown mainly occurs at the gate finger edge of devices, which can be attributed to two reasons. First, the etching process can induce damage especially underlying the gate finger across the edge of the mesa region. The etching damage can also introduce traps resulting in current collapse and gate-lag effects. In addition, a relative higher electric field exists around the sharp tips of the gate finger leading to a lower breakdown voltage. With the proposed layout as shown in Fig. 2 (b), as can be seen, the gate is designed as a closed square shape and thus no overlap between the gate finger loop and the edge of the mesa. As a result, the problems occurred in the multi-finger devices can be avoided. An improved breakdown voltage and reduced current collapse and gate-lag effects can be expected in these devices.

3. Results and Discussion

Fig. 3 (a) shows the measured breakdown voltage of both types of devices for three different L_{gd} values. The square-gate devices show an improvement of ~ 80 V for the average V_{BK} and a much smaller variation from different devices. Fig. 3 (b) compares the off-state gate-source (I_G) and the drain-source (I_D) leakage currents. The square-gate device has both I_G and I_D at least one order of magnitude smaller than those in the multi-finger device. The results demonstrated that the square-gate layout can effectively resolve the problems in the conventional design leading to an improved device breakdown characteristic.

Fig. 4 shows the measurement results of current collapse. Measurements were performed under the sweep of a 60-Hz rectified sine wave using a Tektronix 370 curve tracer. The collapse effect and the knee voltage shift can be clearly observed under different drain bias voltages in traditional multi-finger devices [4]. However, with the proposed square-gate layout, the current collapse is mitigated significantly without changing any process steps. The collapse factor ($\Delta I/I_{max}$) of the square-gate device observed at V_{DS} of 16 V is only 6.2%, which is much smaller than that of the multi-finger device (20.2%). Fig. 5 shows the measured gate-lag characteristics. The applied gate voltage was from –4 V to 0 V using a HP8114 pulse generator. The period and the duty cycle of the pulse were 0.1 s and 50%, respectively. Compared Fig. 5 (a) with Fig. 5(b), the square-gate design demonstrated a much smaller gate lag effect especially under a higher drain bias voltage.

Table I summaries the average characteristics of both types of devices with L_{gd} of 12 μm. As shown in the table, the square-gate devices exhibit a higher breakdown voltage and a smaller current collapse effect. The on-resistance of the square-gate devices is slightly higher due to the longer distance between the middle of the drain to the surrounding source terminal, while the overall figure-of-merit [5] is still clearly improved.

4. Conclusion

In this study, advantages of using the proposed square-gate

AlGaN/GaN HEMTs were demonstrated. With the optimized design, the device can achieve a breakdown voltage exceeding 500 V. Compared with the conventional multi-finger devices, the design successfully improved the breakdown voltage, reduced the off-state leakage, and alleviated current collapse and gate-lag effects. A more reliable high-power operation can be achieved using the square-gate design.

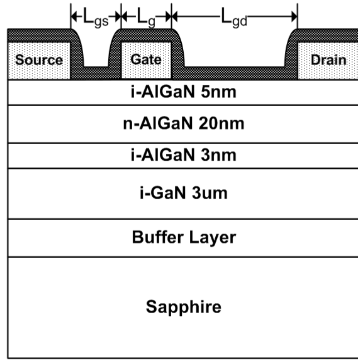
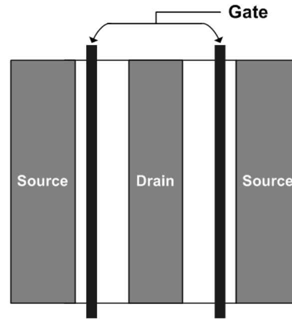
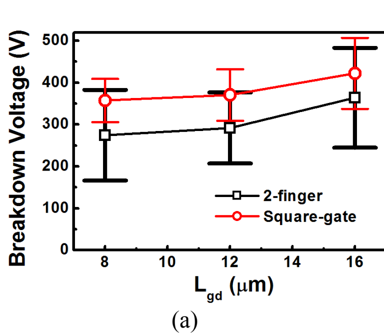


Fig. 1 Layer structure of the AlGaN/GaN HEMTs.

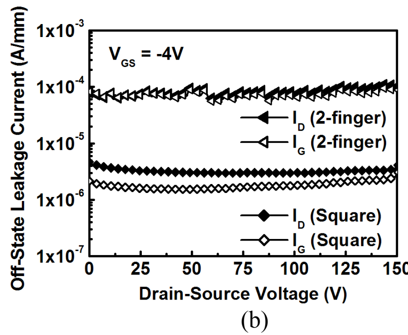


(a) (b)

Fig. 2 (a) Multi-finger layout (b) square-gate layout.

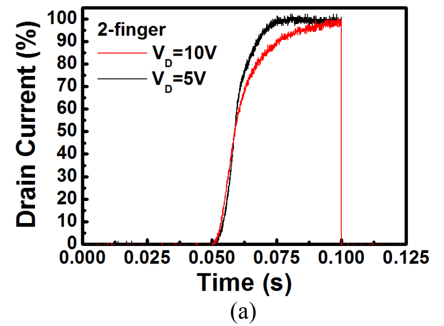


(a)

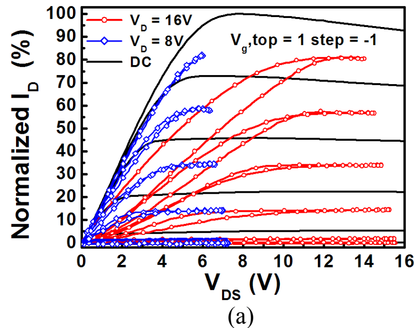


(b)

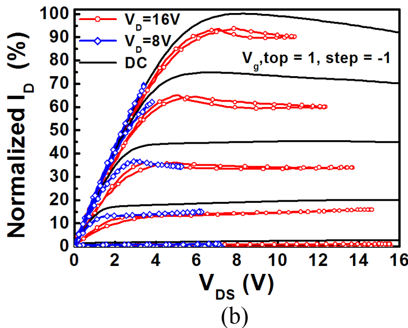
Fig. 3 (a) Breakdown voltage as a function of L_{gd} (b) off-state gate-drain and gate-source leakage currents.



(a)

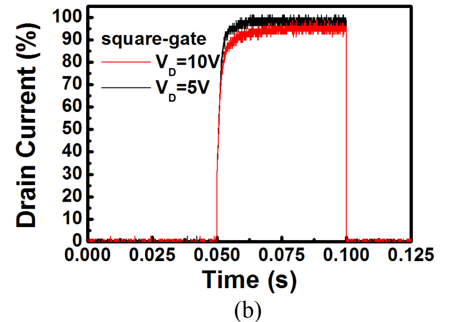


(a)



(b)

Fig. 4 Measured results for current collapse (a) multi-finger and (b) square-gate HEMTs.



(b)

Fig. 5 Gate lag measurement results for (a) multi-finger and (b) square-gate devices.

Table I Comparison between two different layouts

Layout Type	$I_{D,max}$ (mA/mm)	V_{BK} (V)	R_{on} (mΩ-cm^2)	$(\Delta I/I_{max})$	FOM [5]
Multi-finger	250	290	3.5	20.2 %	2.67
Square-gate	220	370	4.2	6.2 %	3.65

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