A 10 Gb/s Wide-Band Current-Mode Logic I/O Interface for High-Speed Interconnect in 0.18μm CMOS Technology

Ching-Te Chiu[1], Jen-Ming Wu, Shuo-Hung Hsu, Min-Sheng Kao, Chih-Hsien Jen, Yarsun Hsu

[1] Department of Electrical Engineering & Institute of Communications engineering, National Tsing Hua University, Hsinchu, 300, Taiwan. E-mail: ctchiu@cs.nthu.edu.tw

Abstract-- A low power, area-efficient 10 Gb/s wide-band current-mode logic (CML) I/O interface for high-speed interconnect is presented in this paper. This interface consists of input equalizer, limiting amplifier, CML buffer and output voltage-peaking circuit. Several wide-band techniques for this work are adopted to broaden the bandwidth and realize the circuit in 10Gb/s operation. The techniques include PMOS active load inductive-peaking, active feedback and Cherry-Hooper topology. These techniques can reduce 80% of the circuit area compared to the circuit area with on-chip inductors. The integration of the input equalizer and output voltage-peaking is also verified in this paper to provide robust I/O interface for high-speed interconnect and compensate transmission signal attenuation in the backplane. This work has been implemented in a 0.18μm CMOS technology. The total power consumption of the I/O interface is only 70mW. The area of input and output interface are 0.02mm^2 and 0.008mm^2. The input interface can operate at 10Gb/s with 40dB input dynamic range and 4mV input sensitivity.

I. INTRODUCTION

The ever-increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs and routers etc., is pushing the off-chip data rate into the gigabits-per-second range. CML I/O interfaces are becoming more and more popular with applications involving transceiver reaching data rates up to 2.5Gb/s or greater [1]. Fig. 1 shows a typical transceiver interface for switch fabric systems. The serial interconnect signals show a lot of high frequency attenuation, skin loss after propagation through long PCB trace on the backplane. At the transmitter, pre-equalizers alter the waveform due to low-pass response of the interconnect [4]. Limiting Amplifiers (LA) are responsible to amplify the input signal to a sufficient voltage for the reliable operation of Clock Data Recovery (CDR). We deploy the current mode logic to implement a CML input interface and a CML output interface. The CML input interface will re-shape and re-amplifier the signal and input to CDR. The CML output interface adopts the voltage peaking technique to enhance the operation bandwidth.

A low power, area-efficient 10Gb/s CML I/O interface for high-speed data transmission is presented in this paper. This architecture of the I/O interface that contains an input equalizer, limiting amplifier, CML output buffer, and a voltage-peaking circuit is described in section II. Each detail circuit block diagram and theoretical analysis will be discussed in section III. The post-simulation results and performance comparison are provided in Section IV. A brief conclusion is given in Section V.

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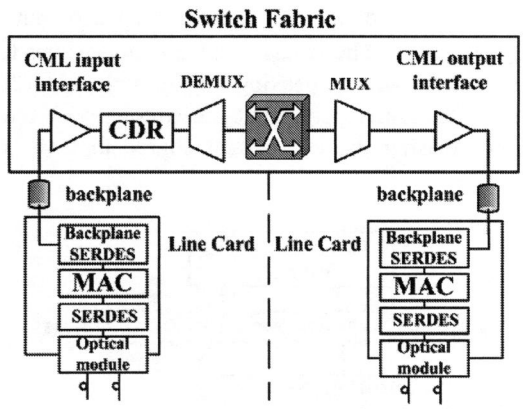


Fig. 1 Block diagram of a typical transceiver interface for switch fabric systems

II. SYSTEM ARCHITECTURE

A. Input Interface With Equalizer

The block diagram of the CML input interface presented in this paper is shown in Fig. 2. This input interface consists of an equalizer, an inductive-peaking active feedback current-mode logic limiting amplifier and a DC offset canceling circuit. The input equalizer is for 50 Ω input impedance matching using Cherry-Hooper topology [2] [6]. The limiting amplifier is fully differential circuit that is composed of a CML input buffer, four gain stage amplifiers and one output buffer. The four gain stage amplifiers are self-biased with a feedback network for DC offset canceling. The tail current of each CML circuit is properly biased by a band-gap reference voltage circuit. All CML buffers and gain-stage amplifiers use PMOS active load and active feedback structure to increase circuit bandwidth for enhancing the operation speed to 10Gb/s. Moreover, the band-gap voltage reference circuit can maintain the operation over a wide temperature range. It can overcome the supply voltage and process variation to provide a stable reference voltage for the tail current. The typical input sensitivity is 4mV and the limiting amplifier output swing is around 250mV for clock data recovery circuit.

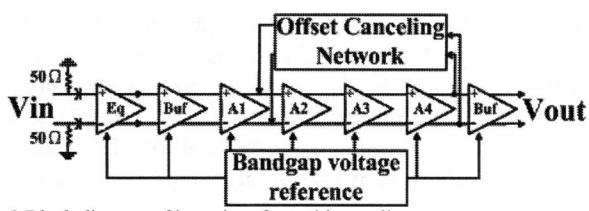


Fig. 2 Block diagram of input interface with equalizer

B. Output Interface With Voltage-Peaking Circuit

The CML output interface is shown in Fig 3. This output interface consists of a level-shift circuit, a voltage-peaking circuit and three-stage CML buffers to be used as a backplane driver. All three-stage CML buffers use PMOS active load and active feedback structure. The tapered CML output buffer increases driving capability stage by stage. The last stage of CML output buffer can provide approximately 8mA driving current in order to drive 50Ω load and let a output swing range up to 250mV. The voltage-peaking circuit owns tunable delay to alter the voltage-peaking tuning range up to 20%. A band-gap voltage reference circuit is used to provide reference voltage for biasing the tail current source in CML output buffer.

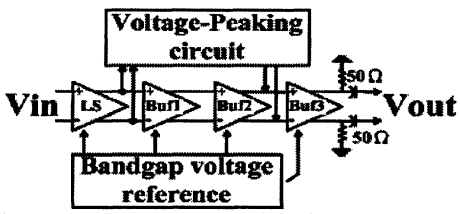


Fig. 3 Block diagram of output interface with voltage-peaking circuit

III. CIRCUIT IMPLEMENTATION

A. Equalizer Circuit

Fig. 4 shows the equalizer circuit that employs the Cherry-Hooper amplifier topology [2]. It is composed of two-stage amplifier circuit with active feedback circuit which includes high bandwidth current buffers M1 and M2. Stage 1 is a trans-conductance amplifier that converts the voltage into current signal. Stage 2 is a trans-impedance circuit that converts the amplified current signal back into voltage. The active feedback amplifier includes current buffers M1 and M2 which increase the gain and the linearity. The proposed equalizer has second-order high-pass transfer characteristics with a tunable zero to compensate for high-frequency loss. The transfer function of the equalizer is approximately given by

$$\frac{V_{OUT}}{V_{IN}} \cong \frac{\left[\left(\frac{1}{R_{NM}}+sC_{NM}\right)+(1+sC_{M1}R_{PM})\frac{1}{G_{M3}}\right](R_1 /\!/ G_{M3}R_{OUT1})R_2G_{M1}G_{M2}]}{(R_1 /\!/ G_{M3}R_{OUT1})R_2G_{M1}G_{M2}+[1+sC_{O1}(R_1 /\!/ G_{M3}R_{OUT1})](1+sC_{O2}R_2)} \quad (1)$$

The R_{NM} and R_{PM} denote the equivalent resistance of the M3 and M4. $R_1 /\!/ G_{M3}R_{OUT1}$ means the total output impedance of stage 1. G_{M1}, G_{M2} and G_{M3} represent the transconductance of the differential pair. C_{NM} is the equivalent NMOS capacitance in the stage 1 and C_{O1}, C_{O2} are the output capacitances of the stage 1 and stage 2. The tunable zero is created by the stage 1 amplifier. A degeneration resistor and a degeneration capacitance are implemented with NMOS transistor to achieve a small size and a wide range of control. The gain and bandwidth are adjusted by controlling the gate voltage (V_1) of the NMOS transistor.

Fig. 5(a) shows that the gain versus frequency characteristics of the equalizer simulated by Hspice. The equalizer gain from DC to 6GHz can be adjusted by the NMOS gate voltage. The gain and the linearity are also enhanced by the feedback current buffer as shown in Fig.5 (b).

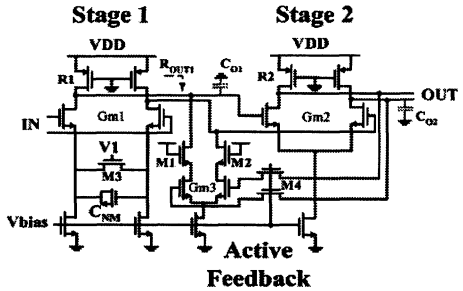
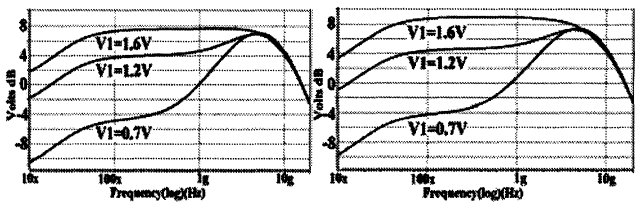


Fig. 4 Block diagram of Equalizer circuit



(a) (b)

Fig. 5 Frequency response of equalizer circuit with NMOS control
(a) Equalizer without current buffers M1 and M2
(b) Equalizer with current buffers M1 and M2

B. Basic Current-mode Logic Circuit

The architecture of a differential current-mode logic buffer circuit in this work is shown in Fig. 6. It includes an active inductor form by PMOS transistors that act as active resistors connected to NMOS transistors load. The input impedance increases with the frequency and acts as the on-chip inductors to employ inductive-peaking and to increase the high-frequency bandwidth. Compared to on-chip inductors, active inductors require much lower chip area and consume less power but have the same frequency response. The gain and the bandwidth of the inductive-peaking CML buffer are adjusted by controlling the size of the PMOS transistor. Fig.7 (a) shows the time domain waveform of the inductive-peaking circuit and Fig.7 (b) represents the bandwidth varied with the size of the PMOS transistor.

To achieve the wide bandwidth operation at 10Gb/s, this CML buffer circuit also incorporates active feedback and negative Miller capacitance to meet high-speed requirement. The differential pair M_5, M_6 and current buffers M_3, M_4 provide active feedback to increase gain and linearity. The transistors M_7 and M_8 introduce a negative Miller capacitance to cancel the Miller capacitance effect of gate-drain and gate-source capacitors of M_1 and M_2. With a gate-source voltage near zero, these devices are realized as accumulation-mode MOS varactors to obtain a larger fraction of the gate oxide capacitance and better tracking. This buffer circuit is used in the entire buffer module for both CML input and output interface.

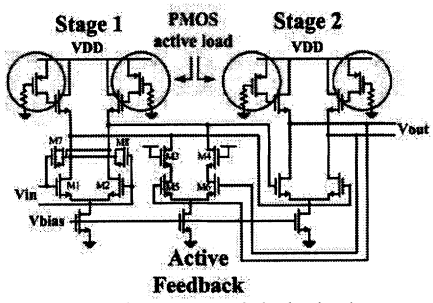


Fig. 6 Block diagram of basic current-mode logic circuit

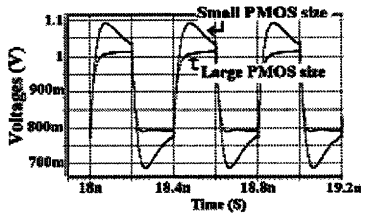


Fig. 7 (a) Time domain waveform of active inductor control

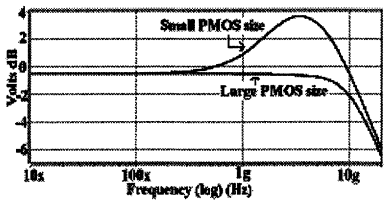


Fig. 7 (b) Frequency response of active inductor control

C. *Gain Stage Amplifier Circuit With Active Feedback*

Fig. 8 shows that a block diagram of four gain stages with a feedback DC offset canceling network. Every amplifier gain stage is composed by CML gain stage circuit that includes pull-up resistors in order to get larger voltage gain. To achieve the required higher bandwidth, current-mode logic gain stage also incorporates active feedback and negative Miller capacitance as shown in Fig. 9. As mentioned earlier, the differential pair M_5, M_6 and current buffers M_3, M_4 provide active feedback to increase gain and linearity. Due to the process variation, the DC offset of the differential amplifier may become large enough to smear the differential output signal. This effect becomes serious especially when the circuit amplifiers a small signal and the DC offset also is amplified at the same time. The DC offset cancellation circuit is necessary because the offset voltages contributed from device and layout mismatches can become a problem after three stages of amplification that make the output signal saturation and duty-cycle distortion. A passive low pass DC offset compensation network is shown in Fig. 8. It is composed of two series resistive branches with off-chip grounding capacitance. Those capacitors are the only external component used in this circuit.

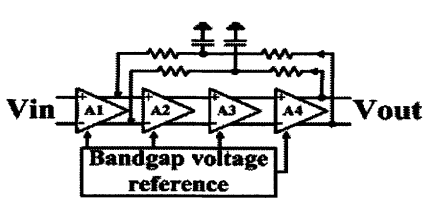


Fig. 8 Block diagram of four gain stages with a total feedback offset canceling network

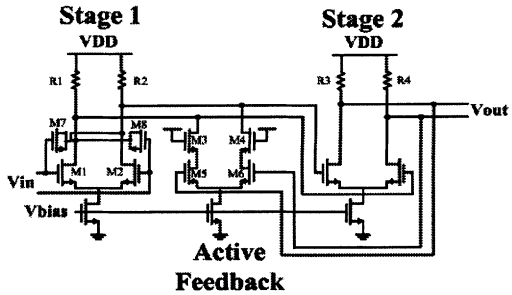


Fig. 9 Block diagram of CML gain stage circuit

D. *Voltage-Peaking Circuit*

The pre-emphasis circuit [4] that is integrated by the CML output interface is to form a voltage-peaking circuit in this paper. The voltage-peaking circuit is shown in Fig 10. It features a CML tunable delay buffer and a differentiator circuit. The CML delay buffer uses basic CML circuit and controls the delay by changing the tail current and inductive-peaking degree to alter voltage-peaking spike width. Fig. 11 shows a simplified differentiator circuit to save the power consumption and layout area. The logical function is similar to that of a digital XOR gate. The current of the current source in the differentiator circuit controls the voltage-peaking spike height. This circuit is used to achieve the 10 Gb/s operation performance in CMOS 0.18μm technology.

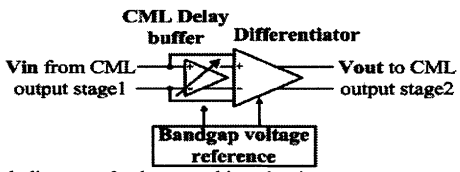


Fig. 10 Block diagram of voltage-peaking circuit

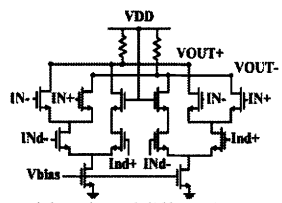


Fig. 11 Block diagram and function of differentiator

E. *Bandgap Voltage Reference Circuit*

The beta multiplier voltage reference (BMVR) [3] is presented in this high-speed I/O interface. Simulated results indicate that the BMVR can be tuned to within 10 mV of a desired value while maintaining a temperature coefficient below 550-ppm/°C and power supply sensitivity under 26 mV/V. BMVR circuit supplies the constant bias voltage for the current source of all the circuit in this I/O interface.

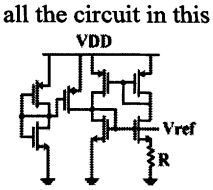


Fig. 12 Block diagram of bandgap voltage reference circuit

IV. EXPERIMENTAL RESULTS

The CML I/O interface has been implemented in 1.8V 0.18μm CMOS technology. The areas of input and output interface are 0.02mm^2 and 0.008mm^2. The total core area of I/O interface is 0.028mm^2, which is almost equal to an on-chip spiral inductor. The layout is shown in Fig. 13.

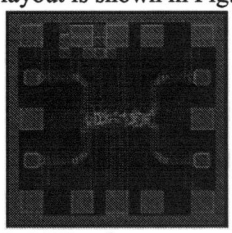
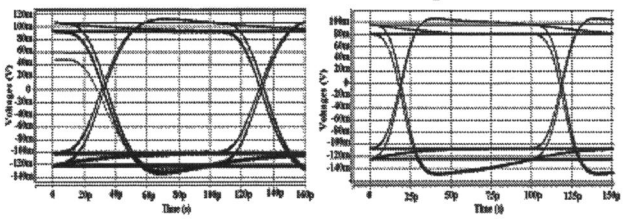


Fig. 13 Layout. core circuit: 0.028mm^2

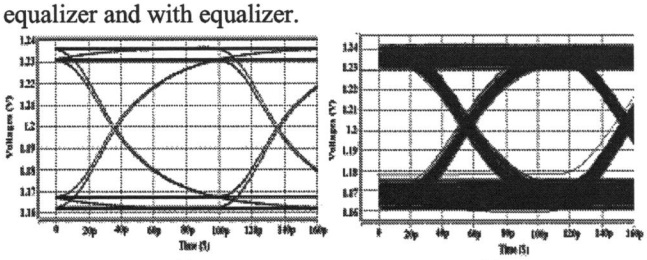
Fig.14 shows the simulated eye diagram. The input signals swing are 4mV$_{PP}$ and 1.8V$_{PP}$ at 10Gb/s, and the output signals measured in 50Ω transmission lines are up to 250mV$_{PP}$.



(a) (b)

Fig. 14 Simulated response of the I/O interface @ 10 Gb/s 2^7-1 PRBS input
(a) Input signal swing: 4mV Output signal swing: 250mV
(b) Input signal swing: 1.8V Output signal swing: 250mV

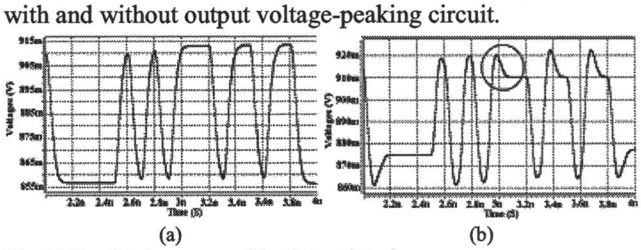
Fig.15 shows the eye diagram of the input interface without equalizer and with equalizer.



(a) (b)

Fig. 15 Simulated response of the Input interface
@ 10 Gb/s 2^7-1 PRBS input
(a) Output signal without equalizer
(b) Output signal with equalizer

Fig.16 shows the voltage waveform of the output interface with and without output voltage-peaking circuit.



(a) (b)

Fig. 16 Simulated response of the Output interface
@ 10 Gb/s 2^7-1 PRBS input
(a) Output signal without output voltage-peaking circuit
(b) Output signal with output voltage-peaking circuit

V. CONCLUSIONS

A low power, area-efficient 10 Gb/s wide-band current-mode logic (CML) I/O interface for high-speed interconnect is presented using a 0.18μm CMOS technology. Several circuits including equalizer, output voltage-peaking circuit, CML gain stage and CML I/O buffer to compensate the signal integrality problem in high-speed data transmission are described. Table I summaries the circuit performance and the comparison with the other recently published results. Clearly, our results have better performances in area and power consumption.

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TABLE I
PERFORMANCE AND COMPARISON WITH THE OTHER RENENTLY PUBLISHED RESULTS.

	This work	[7]	[5]
Process	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply voltage	1.8V	2.4V	1.8V
Power consumption	70mW	120mW	100mW
Operating data rate	10Gb/s	10Gb/s	10Gb/s
Bandwidth (-3dB)	9.5GHz	6.5GHz	9.4GHz
DC gain (differential)	40dB	30dB	50dB
Chip area	0.028mm^2 (Core area)	0.39 mm^2	0.75mm^2