A Ku-band Low-Phase-Noise Transformer Coupled VCO for Satellite Communications

Ping-Yi Wang[1], Min-Chih Chou[1], Yen-Ting Chen[1], Yin-Cheng Chang[1,2], Da-Chiang Chang[2], and Shawn S. H. Hsu[1]

[1]Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan

[2]National Chip Implementation Center, National Applied Research Laboratories, Hsinchu, Taiwan

Abstract — A Ku-band voltage-controlled oscillator (VCO) with a low phase noise is presented in this paper. By increasing the third-harmonic of the fundamental frequency, the transformer-based topology can enforce a pseudo-square voltage waveform in the LC tank to reduce the phase noise. Implemented in a 90-nm standard CMOS technology, the VCO exhibits an average phase noise of -117.2 dc/Hz at 1 MHz offset over a 9.5 – 11.7 GHz tuning range. The oscillator only occupies 0.2 mm^2 while drawing 13.3 mA from the 1.2-V power supply, and the achieved FoM is 185.4 dBc/Hz. The proposed VCO is suitable for applications of satellite communications.

Index Terms —Transformer-coupled, VCO, phase noise, satellite communications.

I. Introduction

The rapid advancements in the digital satellite communication systems demand high performance and low power IC solutions for achieving high frequency wireless link, as shown in Fig. 1 for the Ku-band low noise block. One of the key circuit blocks in the satellite receiver regarding both power dissipation and overall performance is the voltage-controlled oscillators (VCOs). For this reason, the VCO circuits with good phase noise and low power consumption is of extreme importance, but is still a challenging topic nowadays, especially using the CMOS technology.

The class-B VCO is a popular configuration due to the simplicity and robustness, as shown in Fig. 2 (a). However, the phase noise and power efficiency could be degraded significantly with the MOS current source if not designed properly. In addition, the G_M-devices $M_{1\text{-}2}$ enters the deep triode region during a part of the oscillation period. Moreover, the tail capacitor C_T, which creates a low impedance path between the common-mode node and ground, should be large enough to filter out the thermal noise of the current source M_T at around the frequency of even harmonic of the fundamental. A well-known circuit technique of noise filtering was reported in [1], which provides relatively high impedance between the current source and G_M-devices. However, it requires an extra inductor to resonant with the parasitic capacitances, and resulting a large chip size.

Recently, Andreani *et al.* [2] has introduced a class-C harmonic VCO topology, exploiting the advantages of using resistors to bias the transistors in the class-C region, as shown in Fig. 2(b). The dc bias circuit saves nearly 36% of power with the same phase noise performance. However, the constraint of preventing the transistor operating into the deep triode region limits the maximum amplitude of the oscillator

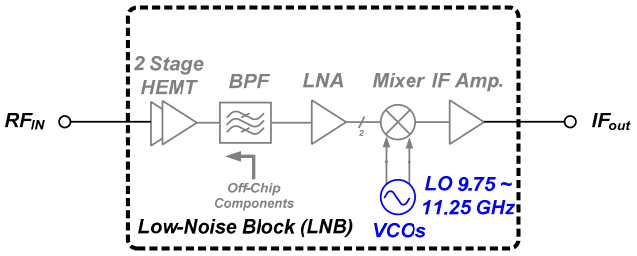

Fig. 1. System block of a Ku-band low-noise block (LNB) for satellite communications.

to be around $V_{DD}/2$. Consequently, the constrained voltage swing limits the lowest achievable phase noise of class-C VCO.

The harmonic tuning oscillator comes up with a pseudo-square voltage waveform in the LC tank by increasing the third-harmonic using an additional peak of tank impedance at that frequency. Based on this idea, Kim *et al.* [3] increases the oscillation zero-crossing slope, resulting in better phase noise performance. However, the two separated inductors cause a large chip size with a reduced tuning range due to the parasitic effects. In this work, we present a transformer coupled technique, which can achieve a small chip area with low phase noise. By using the 90-nm CMOS technology, a Ku-band VCO is implemented and demonstrated for satellite communications.

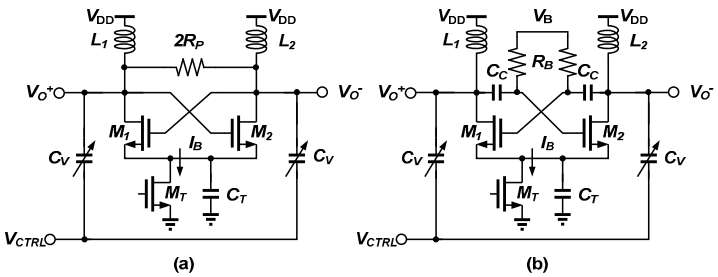

Fig. 2. Two different oscillator topologies. (a) class-B, (b) class-C.

II. Circuit Design

Fig. 3 shows the proposed VCO in class-F operation, where M_1 and M_2 are the transconductance stage for generating the negative impedance, k_m is the coupling coefficient of the transformer, and M_T is the dc bias transistor, respectively. For suppressing the flicker noise from the tail current transistor, the current source capacitor C_T is adopted to filter out the

978-1-5090-1235-0/16/$31.00 ©2016 IEEE

second harmonic leakage from the LC tank. To meet the oscillation criterion of start-up condition, the circuit must satisfy the following equation,

$$G_M \,|\, Z(\omega) \,|\,_{\omega=\omega_0} \geq 1 \qquad (1)$$

Note that a high $|Z(\omega)|$ at ω_0 is desirable since the higher magnitude results in smaller power consumption for maintaining oscillation. The class-F VCO has benefits of higher output swing compared to conventional class-C VCO. The operation principle of the transformer coupled class-F VCO is firstly reported in [4]. By the linear-time variant phase noise model, a square-waveform at the output of the VCO exhibits a lower impulse sensitivity function (ISF) value, which improves the phase noise characteristics. The pseudo-square voltage waveform can be obtained by increasing the impedance amplitude of third harmonic which is coupling from another side of transformer. Fig. 4 presents the EM simulation results of Z_{in} of the transformer-based tank versus frequency with a twin-peak characteristic at f_0 and $3f_0$. The magnitude of Z_{in} is designed at ~ 200 Ω for the 1st peak and 150 Ω for the 3rd harmonic, respectively. In general, increasing the turn ratio n results in sharper transition at zero-crossings and thus enhance oscillation amplitude at the secondary side, which have a direct contribution to phase noise improvement. However, the transformer Q-factors also drops with increased n, and a tradeoff exists.

The line width of both primary and secondary coils is designed as 6 µm. Outer diameter OD of the transformer is 160 µm. The port 1, port 2, port 3, and port 4 are connected to the secondary and primary coils with the capacitance bank C_2 and C_1, respectively. Note port 5 is the dc bias path that provides the dc current to the cross-coupled transistors. The extracted parameters of the transformer are L_1, L_2, n, k, Q_1, and Q_2 of 328 pH, 903 pH, 0.6, 0.66, 20.5 and 12.3, respectively. The fish-bone based pattern grounded shield (PGS) [6] is employed by metal one to isolate the magnetic coupling from the substrate and also improve the Q factor of transformer. The simulated results of the proposed transformer are shown in Fig. 5.

With the considerations of sufficient transconductance and low power operation, the dimension of each cross-coupled device (M_1 and M_2) is 24µm/0.2µm. The tail biasing current generator is implemented with an NMOS transistor of a relatively large dimension of 400 µm/0.5 µm to minimize the 1/f up-conversion to the tank. The MOS varactor is designed by the accumulation-mode MOS (A-MOS) varactors with a gate length of 0.4 µm and a finger number of 48, respectively. The capacitance of the varactor ranges from 150 to 185 fF throughout the entire tuning curve. The coarse tuning capacitor bank is also needed to cover the process variation, which is achieved by 3-bit digital controlled word using binary weighted capacitors array with the capacitances of 30, 60, and 125 fF, respectively. Finally, the tail capacitor C_T is designed as 2 pF to filter out the 2nd order harmonic. The resistor-biased capacitor cell exhibits a better trade-off between tuning range and phase noise. The simulated overall tank Q ranges from 12.0 to 15.2 across the tuning range, including the open drain buffer needed for the measurement.

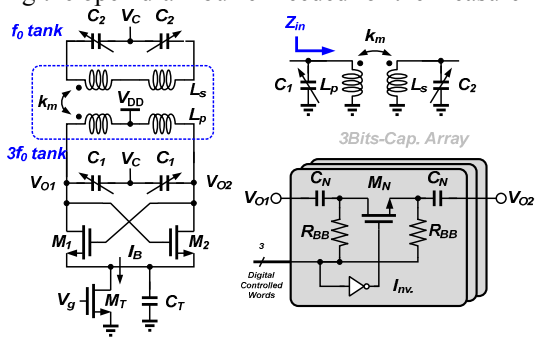

Fig. 3. Schematic of the proposed VCO circuit.

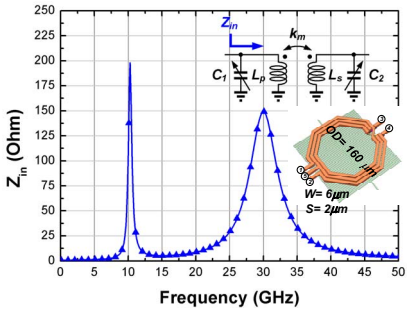

Fig. 4. Input impedance of the transformer-based tank as a function of frequency.

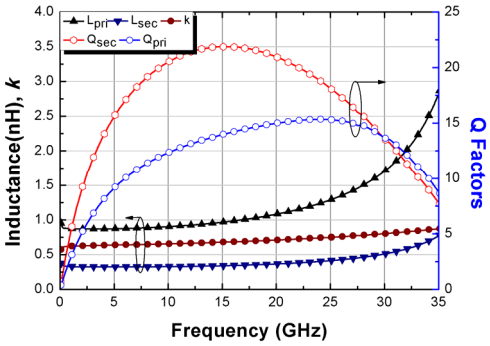

Fig. 5. Simulated results of the proposed transformer.

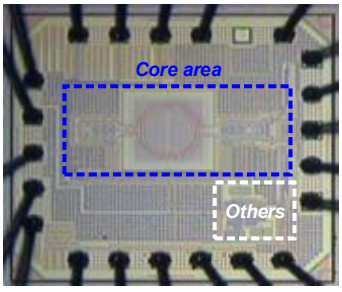

Fig. 6. Micrograph of the proposed transformer coupled VCO.

TABLE I
COMPARISONS OF THE PREVIOUSLY REPORTED VCOS AND THIS WORK

Ref	CMOS Process	Freq. (GHz)	Phase Noise @ 1MHz (dBc/Hz)	Tuning Range (%)	V_{DD} (V)	Power (mW)	FOM (dBc/Hz)	Area (mm^2)
[6]	65 nm	8.2	-120.86	10.5	0.6	10.6-12.3	185.2-188.4	0.38
[7]	65 nm	26	-98.5	15.4	1	26	176.1	0.024
[8]	65 nm	6.25	-111.5~ -117.8	52	0.5	7.4-11	181~185.4	0.67
[9]	90nm	10	-108	2.4	1.2	6.72-9.96	181	N.A.
This work	**90 nm**	**10.6**	**-117.2**	**10.6**	**1.2**	**16**	**185.4**	**0.2**

III. MEASURED RESULTS AND DISCUSSION

Fig. 6 shows the chip micrograph of the proposed VCO with a core area of only 0.2 mm^2. Under a 1.2-V supply voltage, the dc power consumption of the core circuit and buffer are 16 mW and 12 mW, respectively. The output spectrum was measured on wafer by using the Agilent E4407B spectrum analyzer, and the phase noise was measured by using the Agilent E5052B signal source analyzer. Fig. 7 shows the measured frequency range versus the tuning voltage, which is about 2.25 GHz over the entire tuning range. The measured phase noise at 9.45 GHz is -117.2 dBc/Hz at 1 MHz offset as shown in Fig. 8.

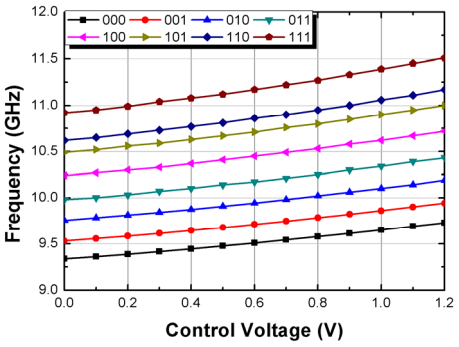

Fig. 7. Measured output frequencies versus tuning voltage.

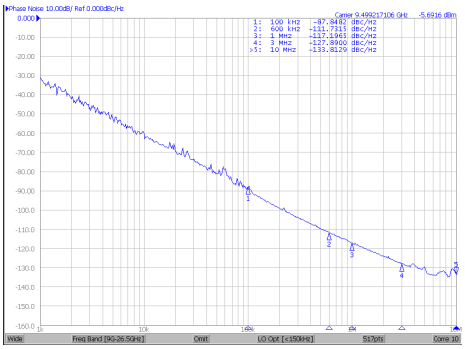

Fig. 8. Measured phase noise at 9.5 GHz.

IV. CONCLUSION

This work successfully demonstrated a Ku-band VCO for satellite communications. With a 1.2-V supply voltage, the proposed VCO achieved phase noise of -117.2 dBc/Hz in a 1MHz offset frequency under 13.3 mA biasing current. The measured results showed that the proposed VCO can achieve a low phase noise with an excellent FOM while maintaining low power consumption and comparable tuning range, compared with previously reported works. The proposed VCO is suitable for the application in high performance frequency synthesizers for satellite communications.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC), Hsinchu, Taiwan for chip implementation and high frequency measurement support by Shawn-Guann Lin and Hsuan-Lun Kuo.

REFERENCES

[1] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no.12, pp. 1921–1930, Dec. 2001

[2] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43,no. 12, pp. 2716–2729, Dec. 2008..

[3] H. Kim, S. Ryu, Y. Chung, J. Choi, and B. Kim, "A low phase-noise CMOS VCO with harmonic tuned LC tank," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 7, pp. 2917–2923, Jul. 2006

[4] M. Babaie and R. B. Staszewski, "Third-harmonic injection technique applied to a 5.87–to7.56 GHz 65 nm class-F oscillator with 192 dBc/Hz FoM," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 348–349

[5] C. Patrick Yue, and S. Simon Wong, "On-chip spiral inductors with patterned ground shield for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May. 1998.

[6] H. Jia, B. Chi, and Z. Wang "An 8.2 GHz triple coupling low-phase-noise class-F QVCO in 65 nm CMOS," *in IEEE ESSCIRC*, pp. 1-4, Sep. 2015

[7] J.-C. Chien, N.-C. Kuo, and Ali. M. Nikenjad "A 26-Ghz low-phase-error in-phase-coupled QVCO using modified bi-directional diode," *in IEEE RFIC*, pp. 1-4, Sep. 2014

[8] M. Elbadry, S. Kalia, and R. Harjani "A 52% tuning range QVCO with a reduced noise coupling scheme and a minimum FOM_T of 196dBc/Hz," *in IEEE CICC*, pp. 1-4, Sep. 2014

[9] J. Borremans, A. Bevilacqua, S. Bronckers, M. Dehan, M. Kuijk, P. Wambacq, and J. Craninckx, "A compact wideband front-end using a single-inductor dual-band VCO in 90 nm digital CMOS," *IEEE J. Solid-State Circuits,* vol. 43, no. 12, pp. 2693–2619, Dec. 2008.