GaN-on-Silicon Devices and Technologies for RF and Microwave Applications

Shawn S. H. Hsu, Chuan-Wei Tsou, Yi-Wei Lian, and Yu-Syuan Lin
Dept. of Electrical Engineering and Institute of Electronics Engineering,
National Tsing Hua University, Hsinchu, Taiwan

***Abstract*— This paper presents our recent studies on GaN-on-Si devices and technologies for RF and microwave applications. The considerations of layer structure and fabrication technology are reviewed including two different GaN-based heterostructures and optimization of ohmic and Schottky contacts. Also, the proposed novel approaches for achieving high speed GaN-on-Si HEMTs are addressed such as the hybrid-drain structure and silicon substrate removal technology. Finally, the small-signal equivalent circuit model is employed to analyze the parasitic effects of silicon substrate for the device at high frequencies.**

***Index Terms*—GaN-on-Si, HEMT, RF, microwave.**

I. INTRODUCTION

THE Gallium Nitride (GaN) technology has attracted tremendous attention recently for RF and microwave applications. With the superior material properties such as the large bandgap (E_g= 3.42 eV), high electron saturation velocity ($v_{sat} \sim 2.7 \times 10^7$ cm/s), large breakdown field ($E_c \sim 3.3$ MV/cm) and high mobility ($\mu_n \sim 2000$ cm^2/V·s) in the 2D electron gas channel, the GaN-based devices are excellent candidates to realize the power amplifiers in the wireless transmitter front-end for achieving high efficiency and high output power. In addition, recent progress of material engineering allows high-quality GaN layers to be grown on large-scale silicon substrates (on an 8-in wafer was reported [1]), making it possible to achieve low-cost and high-performance GaN-on-silicon devices. Table I compares the properties of several commonly used semiconductor materials for RF/MW applications. Note that the Johnson's figure-of-merit (J-FOM) is an index of the high frequency power capability of the material. As can be seen, GaN has an obvious advantage compared with other materials for high frequency and high power applications.

In this paper, the design considerations of GaN-based High Electron Mobility Transistor (HEMT) for high frequency applications are first discussed such as the structure of epitaxial layer, optimization of ohmic contact, and gate recess. Different approaches to improve the frequency response of the GaN-on-Si devices will also be addressed including the proposed hybrid drain design and substrate removal structure. Finally, the small-signal equivalent circuit model is employed to evaluate the substrate parasitic effects in the device to find out the bottleneck of the operating speed of the GaN HEMTs on low-resistivity silicon substrate.

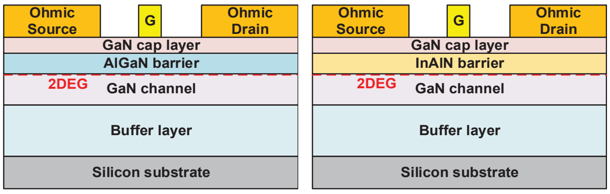
TABLE I
COMPARISON OF DIFFERENT SEMICONDUCTOR MATERIALS

Properties	Si	GaAs	4H-SiC	GaN
Bandgap E_g (eV)	1.12	1.42	3.26	3.42
Dielectric constant ε_r	11.8	12.8	9.7	9
Breakdown field E_c (MV/cm)	0.3	0.4	2.2	3.3
Electron mobility μ_n (cm^2·V^{-1}·s^{-1})	1400	8500	1020	2000
Saturation velocity v_{sat} ×10^7(cm/s)	1	2	2.2	2.7
Intrinsic concentration n_i (cm^{-3}) @ T = 300 K	10^{10}	1.8×10^6	10^{-8}	1.9×10^{-7}
Thermal conductivity k_{th} (W·cm^{-1}·°C^{-1})	1.5	0.5	4.5	1.5
J-FOM	1	3	16	30

II. LAYER STRUCTURE AND FABRICATION TECHNOLOGY

A. *AlGaN/GaN vs. InAlN/GaN Heterojunctions*

Fig. 1(a) shows the typical layer structure for the GaN-on-Si HEMT for high frequency applications. Grown on the high resistivity (HR) silicon substrate with a well-controlled buffer layer (usually an AlN layer), a high quality GaN channel can be formed on the silicon substrate. With the strong piezoelectric and spontaneous polarization effects, the AlGaN/GaN heterostructure exhibits a high carrier density with high mobility in the 2DEG channel. However, the relatively large lattice mismatch between AlGaN and GaN can induce strain, which is critical to the device long term reliability. As shown in Fig. 1(b), a different GaN-based heterostrucure InAlN/GaN has been proposed to solve this problem. The lattice-matched heterostructure of $In_{0.17}Al_{0.83}N$/GaN can produce high spontaneous polarization and achieve an excellent carrier density ($\sim 2.7\times10^{13}$ cm^{-2}). The unstrained barrier also leads to improved device reliability. It should be mentioned that the aspect ratio of $L_G/T_{barrier}$ (gate length/barrier layer thickness) is limited in the conventional AlGaN/GaN structure due to the relative thick barrier layer. With the strong spontaneous effect induced by the InAlN barrier layer, an increased $L_G/T_{barrier}$ value is allowed, which can effectively improve the short channel effect of the device for RF/MW applications. Fig. 2 shows the frequency response of the in-house fabricated InAlN/GaN HEMT. With a foot length of about ~ 0.1-μm as shown in the inset of Fig. 2, the obtained f_{max} exceeds 100 GHz. The achieved J-FOM is 1.3 THz·V [2].



(a) (b)

Fig. 1. Layer structures of (a) AlGaN/GaN HEMT (b) InAlN/GaN HEMT on silicon substrate.

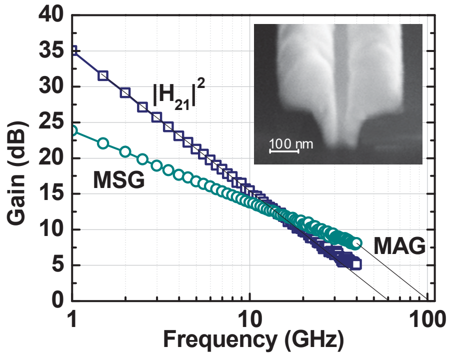


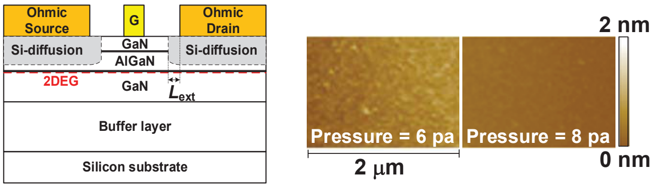
Fig. 2. Frequency response of the in-house fabricated InAlN/GaN HEMT (inset: SEM micrograph of the T-shaped gate).

B. *Fabrication Technology of GaN HEMTs*

It is of critical importance to optimize both the ohmic contact and Schottky contact in the GaN HEMTs for RF/MW applications. A high-quality ohmic contact can reduce the conduction loss, and improve the gain and efficiency of the circuits. Also, the ohmic contact can seriously degrade the breakdown voltage V_{BK} if not properly fabricated. On the other hand, the Schottky gate of HEMT can mainly affect the transconductance of the device and thus the f_T and f_{max}.

Owing to the nature of wide bandgap, optimization of ohmic contact is essential for the GaN-based devices [3]. The layer composition typically used is Ti/Al/Ni/Au to have a low contact resistance. One problem associated with the ohmic contact in GaN HEMT is the metal spikes underneath the contact, which can reach the buffer layer and alter the electric field, resulting in premature breakdown of the device. We proposed using the silicon diffusion structure to solve this problem, as illustrated in Fig. 3(a). With the silicon diffused underneath the ohmic contact, the ohmic spikes can be surrounded. Also, the extended diffusion (L_{ext}) can create a second E-filed peak to reduce the intensity of E-field at around the electrode, which could enhance the breakdown voltage [4].

The gate recess technology allows the Schottky contact to be closer to the 2DEG channel, which can enhance the transconductance g_m and improve both f_T and f_{max} of the devices. The etching process is critical to the recessed Schottky gate. In the developed process, various recipes were attempted to obtain low surface roughness by the ICP-RIE. One sensitive parameter for the etching process is the chamber pressure. The etching rate reduces with increased pressure since the mean energy of ion bombardment becomes lower due to the increased collisions at higher pressures. As a result, the reduced etching rate leads to improved surface roughness. Fig. 3(b) compares the surface morphology for the Schottky recess at two different pressures. Note that a similar technology was applied to the Schottky barrier diodes (SBDs) for power applications, which demonstrated the highest V_{BK} and best FOM for the GaN-on-Si SBDs [5].



(a) (b)

Fig. 3. (a) Silicon diffusion for improved ohmic contacts (b) AFM images of the roughness of recessed sureface with different recepies.

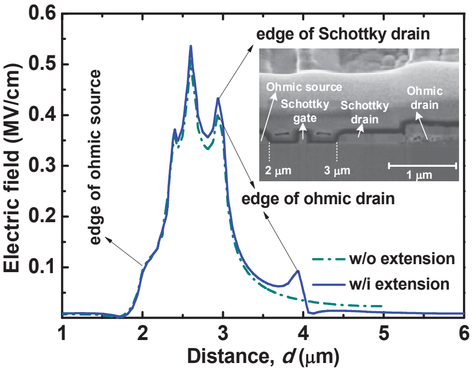


Fig. 4. Electric field distribution of the GaN-on-Si HEMT with and without extended Schottky drain (inset: FIB image of the cross section of the GaN-on-Si HEMT with hybrid drain structure).

III. DESIGN CONSIDERATIONS OF HIGH SPEED GAN-ON-SI HEMTS

A. *Hybrid Schottky Drain Structure*

The most straightforward approach to enhance the high frequency characteristics of FET devices is scaling of the gate length. In addition to that, there are more aspects to be considered to enhance the RF/MW performance for the GaN-on-Si HEMTs. One critical geometrical parameter for improving f_T and f_{max}, which is not often emphasized, is the source-drain distance (L_{SD}). With the shortened L_{SD}, the intrinsic path of carrier transportation is reduced, leading to improved high frequency characteristics of devices. We propose the hybrid Schottky-ohmic drain structure by using the extended Schottky electrode in the drain side to reduce the effective source-drain distance for GaN-on-Si HEMTs. Also, the extended Schottky drain forms a Γ-shape electrode, which can alter the shape of electric field at around the drain side to minimize the leakage and enhance the breakdown voltage [6]. Fig. 4 shows the electric field distribution of the proposed hybrid-drain structure for GaN-on-Si HEMTs compared with the conventional design, where the Schottky drain extension is 1 μm. The peak E-field at the original ohmic contact edge (d= 3 μm) is alleviated successfully. The inset of Fig. 4 presents the cross-section of the GaN-on-Si HEMT with the Schottky drain extension. With the proposed Schottky drain extension, the f_{max} of device can be improved up to ~ 40%. Also, the leakage current can be reduced by 3–4 orders of magnitude with an obviously improved breakdown voltage.

B. GaN-on-Si HEMT with Substrate Removal Structure

One issue of the GaN-on-Si HEMT for RF/MW applications is the parasitic effects introduced by the silicon substrate. The HR substrate is often used to ease this problem. However, compared with the low resistivity (LR) silicon substrate, grown of high strain GaN layer on HR substrate has a more serious bowing problem with increased cost. The bowing problem also limits the GaN-on-Si technology moving towards larger silicon substrates. Inspired by the MEMS technology, we propose the substrate removal structure, as shown in Fig. 5. By removing the substrate, the GaN devices for RF/MW applications can be expected to fabricate on the LR silicon substrate with less parasitic effects. The STAD (Silicon Trench around Drain) structure was proposed [7], which removes the silicon substrate of GaN HEMT from the back side at around the drain to enhance the breakdown voltage of the devices. Although V_{BK} was significantly improved by the STAD structure, the more severe thermal effect was an issue. Compared with the STAD approach, the substrate removal structure that we proposed is from the front side of the transistor, which not only have a simpler process flow, but also with a better control for the thermal effect since the silicon substrate is only partially removed.

C. Small-signal Model Analysis of Substrate Parasitics

Fig. 6(a) shows the small-signal model of GaN-on-Si HEMT including the parasitic elements R_{sub} and C_{sub} introduced by the silicon substrate and buffer capacitance, respectively. Based on the model parameters of our typical process, Fig. 6(b) and 6(c) investigate the impact of different C_{sub} and R_{sub} on power gain of transistor, respectively. It was found that the frequency response is sensitive to the increased C_{sub} if R_{sub} is relatively small, which is corresponding to the LR substrate condition. On the other hand, the frequency response is almost unchanged to the further reduced R_{sub} if C_{sub} is relatively small (corresponding to a think buffer layer). The results indicate the possibility of using LR silicon substrate for GaN-on-Si HEMT in RF/MW applications, as long as a think GaN buffer layer is used.

IV. CONCLUSION

In this paper, the GaN-on-Si technologies and devices for RF and microwave applications were reviewed and discussed including some of our recent progresses. The lattice-matched heterostructure of InAlN/GaN with an increased L_G/T_{barrier} ratio could improve the short channel effect and reliability of devices. Optimization of ohmic and Schottky contacts is of extreme importance to the device high frequency performance, and the proposed silicon diffusion and low-damage gate recess process are beneficial to both f_T and $f_{\max}$ of the devices. The GaN-on-Si HEMT with the hybrid-drain structure was proposed to simultaneously improve DC and RF/MW characteristics, and the partially removed silicon substrate can enhance the breakdown voltage and minimize the substrate parasitics. Also, based on the small-signal model analysis, the GaN-on-Si HEMTs could be realized on the LR substrate for high frequency applications with an increased buffer thickness.

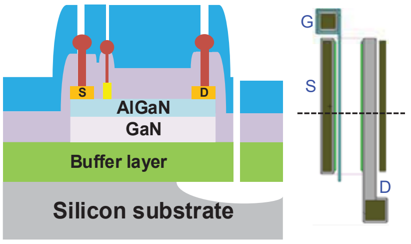
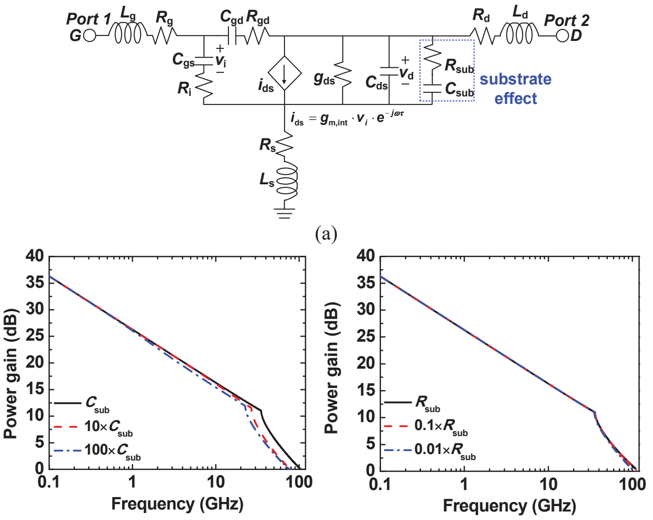


Fig. 5. Conceptual plots of substrate removal for improving the operating speed of transistors.



(a)

(b) (c)

Fig. 6. (a) Small-signal model of GaN-on-Si HEMTs (b) impact of C_{sub} and (c) impact of R_{sub} on device power gain and $f_{\max}$.

ACKNOWLEGEMENT

The authors acknowledge the GlobalWafers Corporation for the support of GaN-on-Si substrates.

REFERENCES

[1] S. Lenci, B. D. Jaeger, L. Carbonell, J. Hu, *et al.*, “Au-free AlGaN/GaN power diode on 8-in Si substrate with gated edge termination,” *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 1035–1037, Aug. 2013.

[2] C.-W. Tsou, C.-Y. Lin, Y.-W. Lian, and S. S. H. Hsu, “101-GHz InAlN/GaN HEMTs on silicon with high Johnson’s figure-of-merit,” *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2675-2678, Aug. 2015.

[3] Y.-W. Lin, Y. Lian, J. Yang, H. Lu, Y. Huang, C. Cheng, and S. S. H. Hsu, “Contact engineering of GaN-on-silicon power devices for breakdown voltage enhancement,” *Semiconductor Science and Technology*, vol. 28, 074018, July 2013.

[4] Y.-W. Lian, Y.-S. Lin, J.-M. Yang, C.-H. Cheng, and S. S. H. Hsu, “AlGaN/GaN Schottky barrier diodes on silicon substrates with selective Si diffusion for low onset voltage and high reverse blocking,” *IEEE Electron Device Letters*, vol. 34, no. 8, pp. 981-983, Aug. 2013.

[5] C.-W. Tsou, K.-P. Wei, Y.-W. Lian, and S. S. H. Hsu “2.07-kV AlGaN/GaN Schottky barrier diodes on silicon with high Baliga’s figure-of-merit,” *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 70–73, Jan. 2016.

[6] Y.-W. Lian, Y.-S. Lin, H.-C. Lu, Y.-C. Huang, and S. S. H. Hsu, “AlGaN/GaN HEMTs on silicon with hybrid Schottky-Ohmic drain for high breakdown voltage and low leakage current,” *IEEE Electron Device Letters*, vol. 33, no. 7, pp. 973-975, July 2012.

[7] P. Srivastava, H. Oprins, M. Van Hove, J. Das, *et al.*, “Si trench around drain (STAD) technology of GaN-DHFETs on Si substrate for boosting power performance,” in *Proc. IEEE IEDM*, Dec. 2011, pp. 19.6.1–19.6.4.