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Chip-Level High-Frequency EMC Strategies and Measurement Techniques

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***Abstract*—This paper presents different electromagnetic compatibility (EMC) strategies for achieving low EM emission and high immunity. The proposed designs and measurement techniques for improving and evaluating the chip level EM interference (EMI) and EM susceptibility (EMS) are included to provide high-frequency EMC solutions. This paper also gives a comprehensive overview for the researchers to continue working on the EMC-related topics and issues at the chip level at high frequencies.**

Keywords—electromagnetic interference (EMI), electromagnetic susceptibility (EMS), IC-electromagnetic compatibility (IC-EMC), measurement, on-chip.

I. Introduction

With the continuous scaling of transistor feature size, the gate count, operating speed, integration level, and packaging complexity keep increasing for modern IC technology. In this era of More than Moore, one related topic that attracts significant attention is the electromagnetic compatibility (EMC) of ICs, in which characterization of EM emission and immunity becomes an important issue. The Intl. Electro-technical Commission (IEC) published a series of standards of IC level test approaches on electromagnetic interference (EMI, 61967 series) [1] and electromagnetic susceptibility (EMS, 62132 series) [2]. The test methods can be divided into radiated or conducted ones as illustrated in Fig. 1.

Currently, the released standards are only available at the IC level with the frequency range below 1 GHz, which cannot cover the frequency range to evaluate EMC for modern chips/ICs operating in the GHz or even up to tens of GHz. Some works for expanding the operation frequency range of the IEC standards were reported [3]-[5]. For instance, by applying the ultra-wide bandwidth components with the well-designed PCB, the applicable bandwidth of the IEC direct power injection (DPI) method [6] can be improved significantly, which allowed investigating the IC-level conducted immunity up to 18 GHz [3]. For the conducted emission measurements, a high precision 1-Ω resistor is the most critical component for the current probe in the IEC 61967-4 standard [7], but the resistor with a wideband characteristic is unavailable. We proposed using the Integrated Passive Device (IPD) resistive network to replace the SMD resistors, and the applicable bandwidth of 1-Ω probe is effectively enhanced from 1 GHz to 2.4 GHz [4]. Also, an IC stripline [8] with a bandwidth of 2.5 GHz was realized to evaluate the injection pulling performance of VCO for the radiated immunity test [5]. In this paper, both the conducted and radiated EMC strategies and measurement techniques at the chip level for high-frequency applications will be reviewed and discussed.

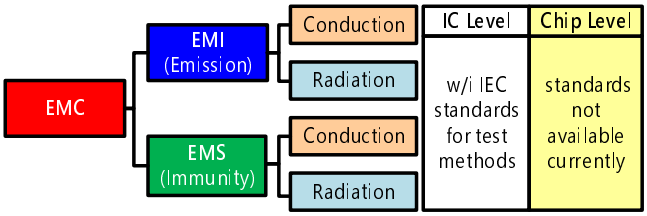
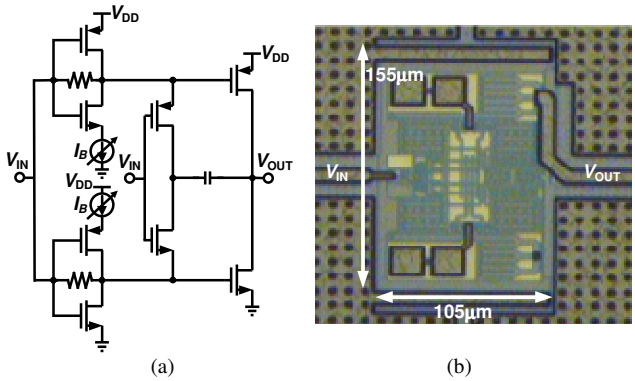
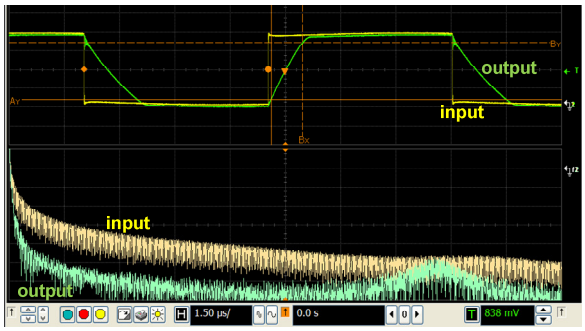


Fig. 1. EMC categories and the status of published EMC standards.



(a) (b)



(c)

Fig. 2. Slew rate controller for low conducted EMI [11]: (a) circuit schematic, (b) chip photo, and (c) input and output waveforms and FFT spectrum of a 100 kHz signal.

II. Design and Testing for Conducted EMI/EMS

A. On-Chip Strategies for Conducted EMI/EMS

Most EMC issues at the system level are mainly considered via careful PCB layout and filtering/shielding element placement. It is essential to consider the EMC solution at the chip and/or package level at high operating frequencies. Based on the EMC strategies at the PCB level, more aggressive techniques have been proposed [9]-[10].

We proposed two on-chip EMC strategies with low design complexity and low cost [11]-[12]. Using an on-chip slew rate controller circuit as the output driver, the noise can be reduced to avoid the EMI issue by increasing the rise and

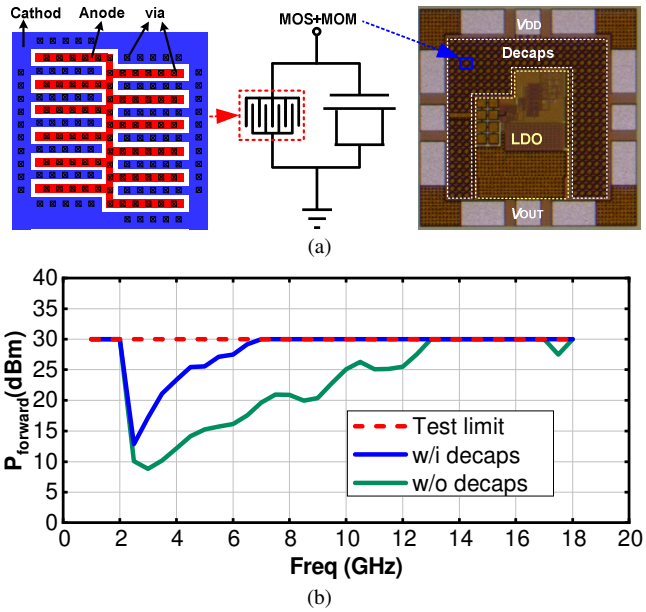


Fig. 3. Decoupling capacitor design for low conducted EMS [11]: (a) MOM+MOS decaps for LDO and (b) LDO with dacaps exhibit lower susceptibility in DPI testing [12].

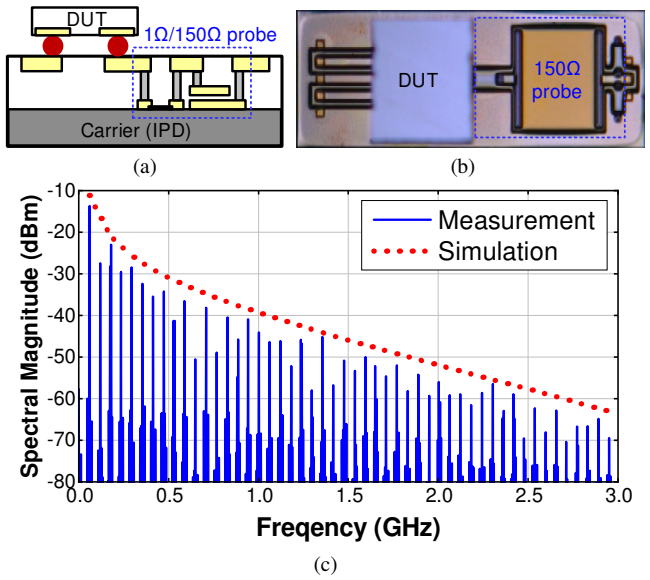


Fig. 4. Chip level conducted EMI measurement [13]: (a) EMI probes realized by the IPD technology with the flip-chip DUT, (b) photo of flipped DUT (VCO) with the 150-Ω probe, and (c) measured spectra of VCO using 150-Ω probe.

fall time of the fast output transition edges as shown in Fig. 2 [11]. A prototype design was realized by 0.18-µm CMOS, and the measured results indicate that the high-frequency contents of the signal can be reduced, and EMI issue can be improved effectively. This circuit can be a part of the I/O block for practical applications.

Another approach that we proposed for improving on-chip EMC is an ultra-high-density decoupling capacitor with stacked MOM and MOS capacitors (Fig. 3(a)), which could provide an extra 17% capacitance compared with the MOS capacitor only. By embedding the decoupling capacitors into a low dropout regulator (LDO) [12] using 0.18-µm CMOS, the EMS can be improved up to 11.6 dB as shown in Fig 3(b).

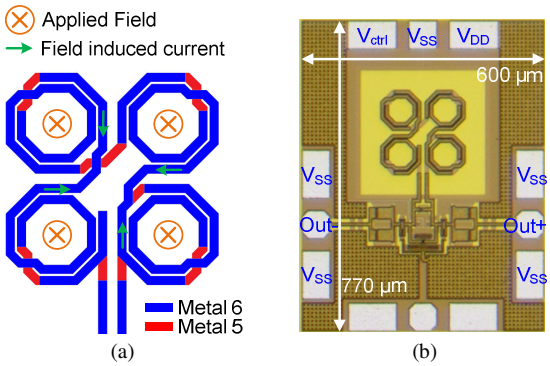


Fig. 5. Inductor design for low radiated EMS and EMI [14]: (a) field-induced currents canceled each other under an applied field in a twisted inductor, and (b) VCO using the twisted inductor with low EMS.

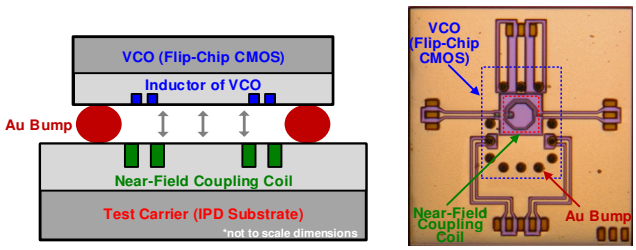


Fig. 6. Chip level radiated EMI and EMS measurement [14]: (a) testing configuration for near field coupling, and (b) top view photo of the test carrier using the IPD substrate.

B. *Measurement Techniques for Conducted EMI/EMS*

The conducted EMS of IC is typically characterized via a method called direct power injection (DPI) [6], which is straightforward to observe the malfunction of the ICs. A similar setup can be applied from the IC level to the chip level by using a typical microwave probe testing system. For example, the proposed design shown in Fig. 3 was evaluated by DPI using this approach.

In contrast, no suitable conducted EMI testing method is available at the chip level. The direct coupling method [7] is widely used for EMI at the IC level. However, the main challenge is that no on-chip probes can be used for the conducted EMI test, especially at high frequencies. We proposed using the IPD technology to realize the high precision 1-Ω/150-Ω probes to capture the signal at the chip level [13], as illustrated in Fig. 4 (a). Fig. 4(b) shows a flip-chip DUT above the carrier IPD substrate with the embedded 150-Ω chip probes. The measurement frequency range can be significantly improved exceeding 20 GHz. Fig. 4(c) shows the measured result of a CMOS ring oscillator by using a chip-level 150-Ω probe. The measured spectrum shows an excellent agreement with the simulated result.

III. Design and Testing for Radiated EMI/EMS

A. *On-Chip Strategies for Radiated EMI/EMS*

In RF design, a rule of thumb to avoid EM emission is to minimize the loop area of a conductor. However, the inductive elements are essential for RF circuits and are often routed as a loop shape. As a result, noise can be easily coupled from the nearby circuits via the inductors. Fig. 5(a) illustrates the proposed twisted inductor for improving EMI/EMS [14]. The metal routing of the inductor can make each lobe generate an

equal magnetic field but exhibits opposite polarity with its adjacent lobe, which can reduce the EM emission. On the other hand, assuming an external undesired field is applied to the inductor, the induced current will cancel each other, which can effectively improve the EMS. A VCO in 0.18-μm CMOS is realized with the twisted inductor as shown in Fig. 5 (b). We also proposed a novel 3D testing setup using the IPD technology to verify the low EMI/EMS property of the VCO as discussed as follows.

B. Measurement Technique for Radiated EMI/EMS

An effective test setup is proposed to demonstrate the chip level EMI/EMS testing. Unlike other reported approaches that place the coupling coil next to the VCO on the same die for EMS testing, the coupling coil is set on top of the VCO directly [14] as illustrated in Fig. 6(a) by flip-chip technology. This proposed test setup can emulate the 3D packaging scenario in the advanced multiple-chip stacking technology. The coupling coil is designed by the IPD technology as shown in Fig. 6(b). The generated magnetic flux from the eXternally injected interference can be directly coupled to the DUT to evaluate the EMS in a stacked die packaging condition. The IPD coil can also be used as a receiver for the EMI test of the DUT. Compared with the conventional 2D testing scenario, the proposed configuration could provide a more uniform magnetic flux with a higher intensity to obtain more precise measurement results, which is more realistic to the actual 3D packaging. The proposed approach is suitable to characterize the EMS/EMI of DUT in the condition of radiated RF interference at the chip level.

IV. Conclusion

This paper presents and discusses various strategies and measurement techniques for the chip-level EMC, which has no IEC standard available currently. We proposed several effective chip-level solutions for the EMC relative problem, which are effective for high-frequency/high-speed IC applications. Also, the proposed novel approaches using the IPD technologies for on-chip probes and testing structures are suitable for evaluating EMC for the future 3D stack die packaging with high operating frequencies at the chip level.

Acknoledgement

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