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A 3.2 GBIT/S CML TRANSMITTER WITH 20:1 MULTIPLEXER IN 0.18 CMOS TECHNOLOGY

C. H. HSIAO, M. S. KAO, C. H. JEN, Y. H. HSU, P. L. YANG, C. T. CHIU, J. M. WU, S. H. HSU, Y. S. HSU
NATIONAL TSING HUA UNIVERSITY , TAIWAN

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ABSTRACT: In this paper, a 3.2Gb/s CML transmitter with 20:1 multiplexer was developed for integrating with 8/10B encoders in high speed network applications. Compared with the common 10:1 multiplexer, this 20:1 transmitter reduces the required operating frequency in routers or switches by half. A double phase source coupled logic based differential circuit is used to achieve the 20:1 serialization with reduced noise effects. A low-power PLL is embedded for generating on chip dual phase clocks. A wide-band low power high speed CML output buffer could provide 250mV output voltage swing up to 10Gb/s. The overall chip size is 650umx950um with power consumption of 104 mW at 3.2Gb/s.

INTRODUCTION

The 2.5~3.2Gbps transmitters is the most popular I/O interface for SONET or high speed Ethernet networking device. Almost all the transmitters adopt the 8/10:1 multiplexing schemes due to the 8/10B encoding. When integrating the transmitter with other high speed routers or switches modules in a single IC, the 8/10:1 multiplexing requires 250M~320MHz clock frequency to maintain the high data throughput rate. Therefore, we proposed a 20:1 transmitter that can reduce the operating frequency requirement in digital core by half.
The 20:1 transmitter contains a 20:1 serializer, a CML output buffer and PLL as shown in Fig. 1. The 20:1 multiplexer converts the parallel data into a serial datum through a set of shift register circuit and the CML output buffer. The 20:1 multiplexer design is presented in section 2. The PLL & CML output buffer are described in section 3 and 4. The simulation and measurement results are shown in section 5 and 6. A brief conclusion is given in section 7.

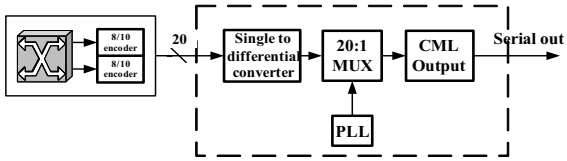

Fig. 1. CML Transmitter with 20:1 MUX

20:1 MULTIPLEXER

The 20:1 multiplexer (MUX) converts the twenty bit input data into a serial datum. For the 20:1 multiplexing, since it is not the power of 2, the general tree type multiplexer can not be used. Therefore, we adopt the shift register approach [1] to store the parallel inputs and send it out serially. In order to achieve the 3.2Gbps data rate, the Source Coupled Logic (SCL)[2] circuits is used in the implementation.

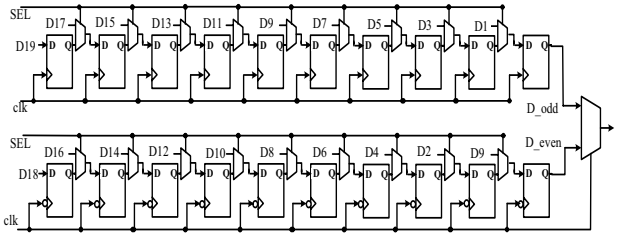

Fig. 2. 20:1 Multiplexer

The block diagram of the 20:1 MUX is shown in Fig. 2. The data stream is divided and sent into two separate 10:1 MUXs, which is composed of nine 2:1 MUXs and ten D flip-flops. The upper 10:1 MUX loads and shifts the odd bit of the parallel data, while the lower one operates the even bits. The twenty bit parallel data are loaded in registers when SEL signal is enabled. Then the even and odd data bits are shifted at the rising and falling edge of the clock. The 2:1 MUX at the right of the 10:1 MUX selects even data bit when clock is high and odd data bit when clock is low. This architecture can be extended to convert any parallel data with even number of bit-width.
The duty cycle of the clock would affect the output of the last 2:1 MUX. In our simulation, we can get 60 picoseconds jitter at the CML output buffer when the 60% duty cycle clock is provided.

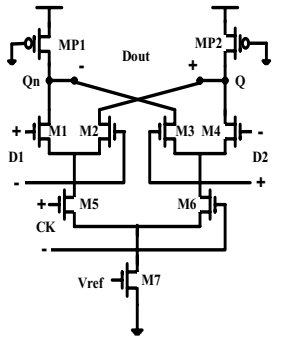

Fig. 3. 2:1 MUX

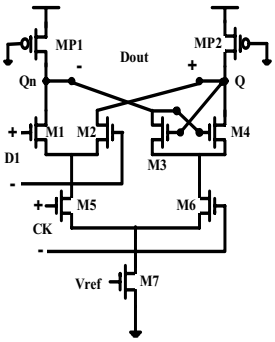

Fig. 4. D-Latch

Fig. 3 is the circuit diagram of a 2:1 MUX [2]. It consists of two symmetric differential pairs M1-M2 and M3-M4 that sample the inputs D1 and D2. The two pairs are controlled by the clock CK through the lower-level pair M5-M6. The MP1and MP2 are the active loads that determine the output swing range.

When the clock CK is positive, the M5 is turned on. Then the input D1 is sampled by the differential pair M1-M2. At the same time, M6 is turned off and the pair M3-M4 is disabled. When the clock CK becomes negative, M1-M2 is disabled and M3-M4 is enabled. So the input signal D2 is transferred to the output.

The operation of the D-Latch [2], as shown in Fig. 4, is similar to the 2:1 MUX. The input D2 in the MUX is connected to the output Q. The M1-M2 is an input sampling pair and the M3-M4 becomes a latching pair. When CK is positive, the sampling pair is enabled. The output nodes Q and Qn track the input D. When CK goes low, the sampling pair turns off and the latching pair turns on. Then the instantaneous states at Q and Qn are stored in the loop around M3 and M4. Two D-latches are cascaded to realize a D flip-flop.

The SCL circuits are based on differential pair design which can reduce the noise and coupling effects. That is reason we adopt the SCL circuits to implement the 2:1 MUX and the D flip-flop.

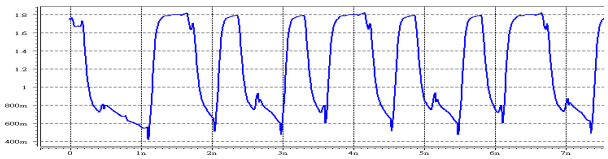

Fig. 5. Output waveform of 20:1 MUX at 3.2Gb/s

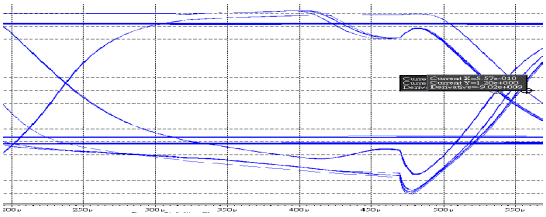

Fig. 6. Eye diagram of 20:1 MUX with 21 ps at 3.2Gb/s

Fig. 5 shows the output waveform of the 20:1 MUX. Its swing range is 0.9v to 1.8v. Fig. 6 shows the eye diagram of the 20:1 MUX. We can see that the 20:1 MUX alone has 21 picoseconds jitter under 50% duty cycle clock. The comparison of our 20:1 MUX and [3] is summaried in Table.1. It shows that our design can achieve higher data rate with more data multiplexing and less peak to peak jitters.

TABLE 1. Summary of 20:1 MUX with comparation

	20:1 MUX	16:1 MUX[3]
technology	0.18um CMOS	0.18um CMOS
Supply voltage	1.8 v	2 v
Data rate	~ 6Gb/s	~ 3.6Gb/s
Power dissipation	43 mW (core)	30 mW (core)
Jitter (with output buffer)	21ps	100 ps

PHASE LOCK LOOP

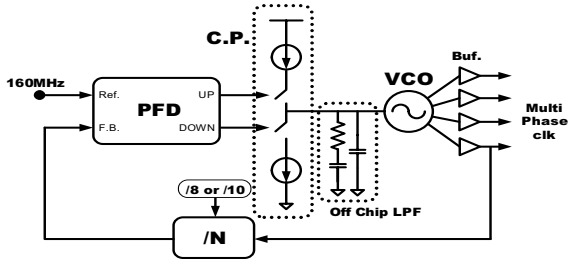

Fig. 7. PLL block diagram.

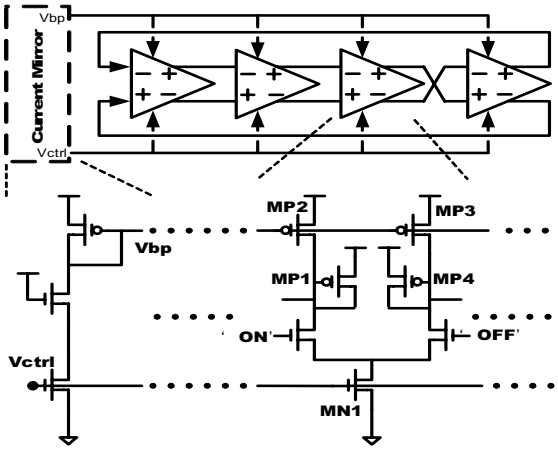

Fig. 8. Current mirror and one VCO delay stage.

Multi-phase phase lock loop (PLL), shown in Fig. 7, contains a ring-type voltage control oscillator (VCO), a phase frequency detector (PFD), a charge pump (C.P.), a divided-by-8/10 two-mode divider, and a 2^{nd} order loop filter. The dual phase clocks from VCO modules are used as differential clocks for the 2-1 MUX and DFFs.

Fig. 8 shows the circuit schematic of the VCO, including a current mirror and a 4-stage ring oscillator generating up to 8 output phases[6]. The current mirror reflects half of the MN1 current to each of MP2 and MP3 in Fig. 8. The output of the branch in differential stage that is 'ON' is discharged by half of the MN1 current until reaching Vdd-Vt where the PMOS diode MP1 clamps the voltage. The opposite 'OFF' branch is pulled to Vdd by the MP3 current which is half of the MN1 current. This provides the fixed swing and common mode operation. It makes this VCO suitable for a wide range of operating frequencies and supply voltage. To obtain 50% duty cycle full-swing output, a differential-to-single-ended converter circuit is designed in every VCO multi-phase output[7].

Fig. 9 shows the PFD in PLL. It is the well-known PFD based on four RS latches[8] and a delay chain which eliminates the dead zone. The charge pump is shown in Fig. 10. Two transistors Mn and Mp are used to eliminate charges stored on parasitic capacitors in node n1 and n2[6]. Furthermore, the PLL design parameters, such as bandwidth and damping factor, change with the division ratio N in feedback path. To compensate loop parameters for changes in N, the Mr1 current branch must be turned on while the frequency divider is in N=10 mode.

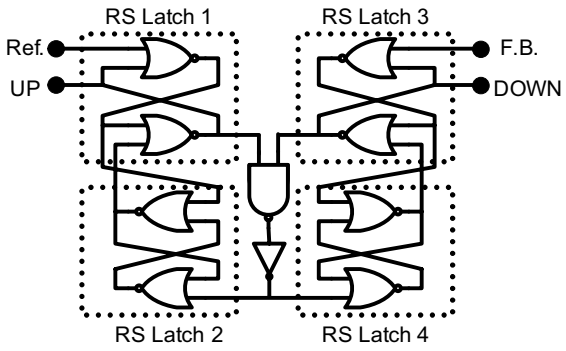

Fig. 9. Phase-frequency detector.

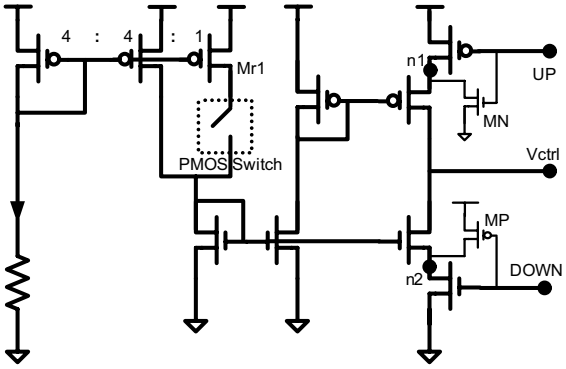

Fig. 10. Charge pump.

The frequency divider circuit provides /8 and /10 modes. We use the off chip loop filter to minimize the area in this test chip.

The simulation result of the PLL frequency range is 5MHz-2.26GHz at Vdd=1.8V. The peak-to-peak jitter of the VCO output is about 32ps at target frequency 1.6GHz, as shown in Fig. 11. The core area of the PLL is about 450*400 um^2. And the power consumption is about 45mw at output frequency 1.6GHz, Vdd=1.8V, and divider ratio N=10.

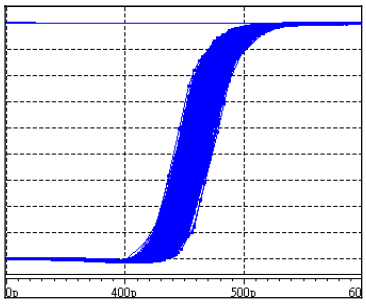

Fig. 11. 4 phase PLL simulation, 32ps at 1.6GHz.

CML OUTPUT BUFFER

The CML output interface is shown in Fig 12. This output interface consists of a level-shift circuit, a voltage-peaking circuit [4] and three-stage CML buffers. It is used as a backplane driver [5]. All three-stage CML buffers use PMOS active load and active feedback structure. The tapered CML output buffer increases driving capability stage by stage. The last stage of CML output buffer can provide approximately 8mA driving current in order to drive 50Ω load and let a output swing range up to 250mV. The voltage-peaking circuit owns tunable delay to alter the voltage-peaking tuning range up to 20%.

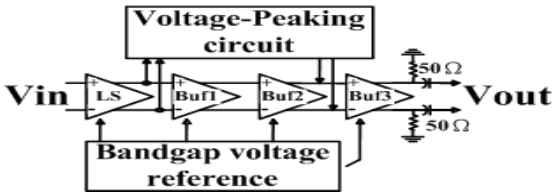

Fig. 12. Block diagram of output interface with voltagepeaking circuit

The architecture of a differential current-mode logic buffer circuit is shown in Fig. 13. It includes an active inductor formed by PMOS transistors that act as active resistors connected to NMOS transistors load. They act as the on-chip inductors to employ inductive-peaking.

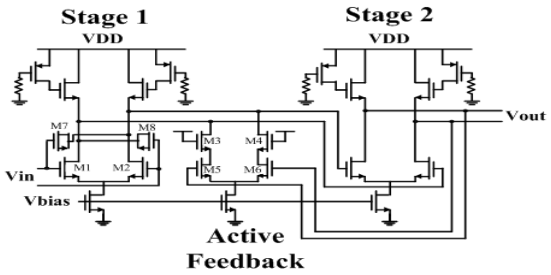

Fig. 13. Block diagram of basic current-mode logic circuit

Fig. 14 shows the CML active load and equivalent schematics. It includes an active inductor formed by PMOS transistors that act as active resistors connected to the NMOS. The PMOS act as a linear resistor R_{DS} when the source-drain voltage V_{SD} is small. The function of this linear resistor R_{DS} is:

$$R_{DS} \propto \frac{V_{SD}}{I_D} \qquad (1)$$

So, the PMOS active load works like an active inductor when the R_{DS} is larger. This could be controlled by tuning the PMOS size and V_{SD} of the PMOS. Moreover, a resistor is added to the gate of PMOS for ESD protection.

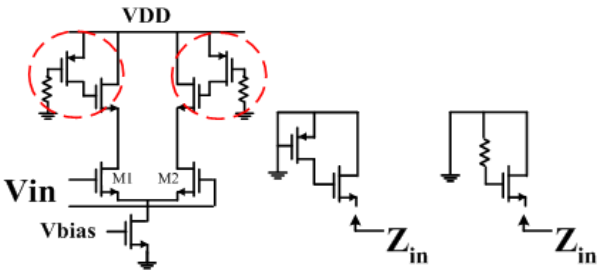

Fig. 14(a,b,c). CML active load and equivalent schematics.

Fig. 14 (b) & (c) are the equivalent schematic of active load in Fig. 14 (a) with the omitting of resistors. The small-signal model and analysis of the active load is shown in Fig. 15 below. Fig. 15 (a) is the small-signal

model; Fig. 15 (b) is the plot of Zin vs. frequency; Fig. 15 (c) is the small signal equivalent model. The impedance Z_{in} can be approximated by:

$$Z_{in} = \frac{1}{Gm}\frac{1+sC_{gs}R_f}{1+\frac{C_{gs}}{Gm}} \qquad (2)$$

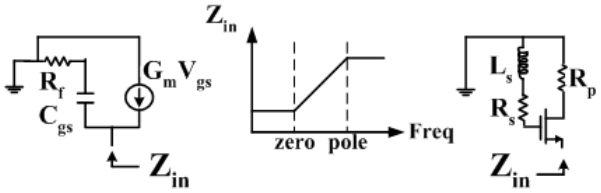

Fig. 15(a,b,c). The small signal model of the active load.

The impedance increases with the frequency and could act as the inductor to employ inductive-peaking and to increase the high-frequency bandwidth.

Compared to on-chip inductors, active inductors require much lower chip area and consume less power but have the same frequency response. Fig. 16 represents the bandwidth varied with the size of the PMOS transistor. Fig. 17 shows the simulated response of the CML Output Buffer. This CML buffer circuit also incorporates active feedback and negative Miller capacitance to meet high-speed requirement.

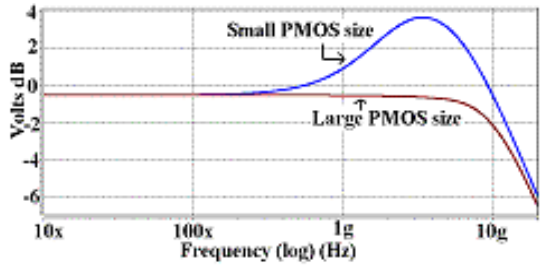

Fig. 16. Frequency response of active inductor control

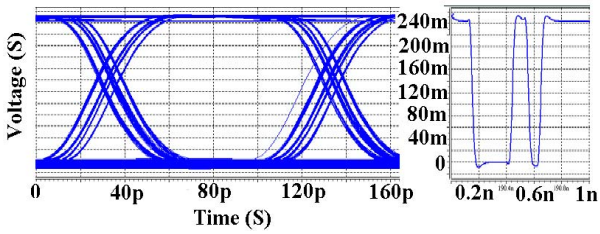

Fig. 17. Simulated response of the CML Output Buffer at 10 Gb/s $2^7 - 1$ PRBS input

SIMULATION RESULTS

We have integrated the 20:1 multiplexer, PLL and CML output buffer. Fig. 18 shows that simulated waveform at the output of CML buffer with 50Ω load resistance. Fig. 19 shows the eye diagram from the 1.6GHz CML output. The peak to peak jitter is 60 ps. The overall chip layout is shown in Fig. 20. The performance of the MUX, PLL and CML output buffer are summarized in Table 2.

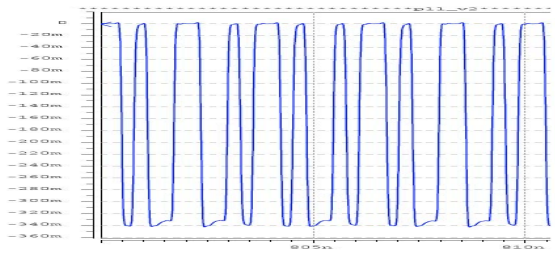

Fig. 18. Waveform of the transmitter output at CML output buffer

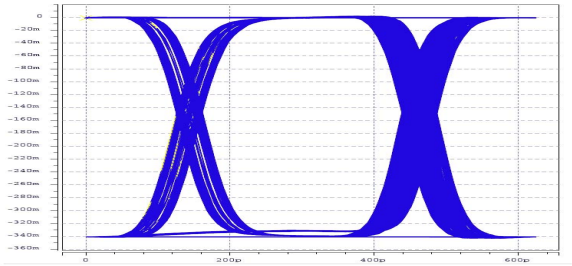

Fig. 19. Eye diagram of the transmitter output

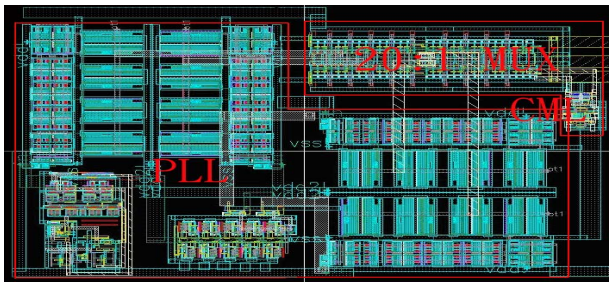

Fig. 20. Overall chip layout

TABLE 2. Summary of MUX, PLL, and CML

	20:1 MUX	PLL	CML
V_{DD}	1.8 V	1.8 V	1.8 V
Operation frequency	~ 6Gb/s	5MHz – 2.26GHz	~10Gb/s
Power	43 mW	45 mW	15mW
Jitter	21ps at 3.2Gb/s	32ps at 1.6GHz	10ps at 3.2Gb/s
Die size	150 * 300 um^2	450 * 400 um^2	100 * 200 um^2

MEASUREMENT RESULTS

Because of the chip area limitation, the PLL and the 20:1 multiplexer with CML output buffer are fabricated in separate chips. Fig. 21 shows the die microphotograph of the 20:1 multiplexer whose output waveform with the CML output buffer at 1.88Gb/s is shown in Fig. 22.

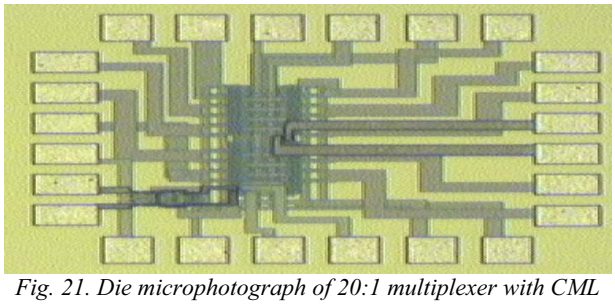

Fig. 21. Die microphotograph of 20:1 multiplexer with CML output buffer.

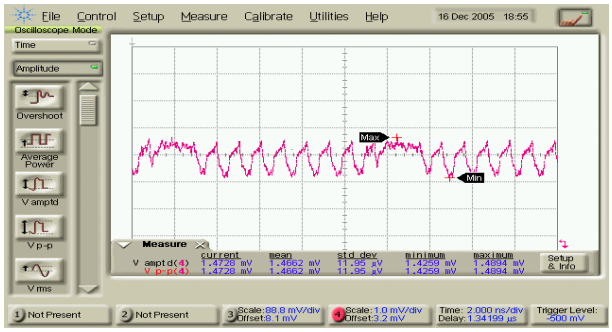

Fig. 22. Measurement of 20:1 multiplexer with CML output buffer at 1.88Gb/s.

Fig. 23 shows the microphotograph of PLL, and Fig. 24 shows the PLL generated clock. The PLL spectrum with peak at 1.606GHz is shown in Fig. 25.

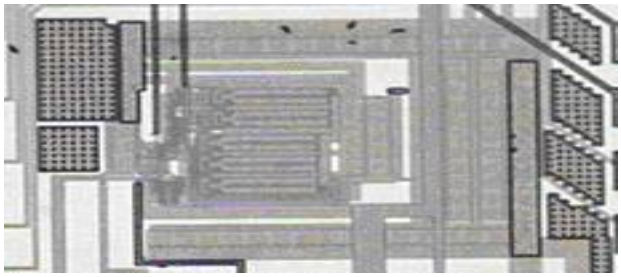

Fig. 23. Die microphotograph of PLL.

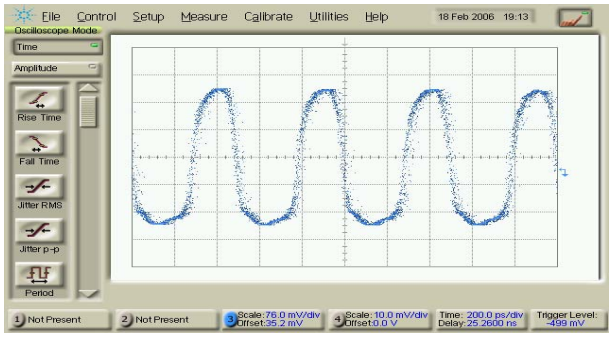

Fig. 24. The PLL generated clock at 1.6GHz.

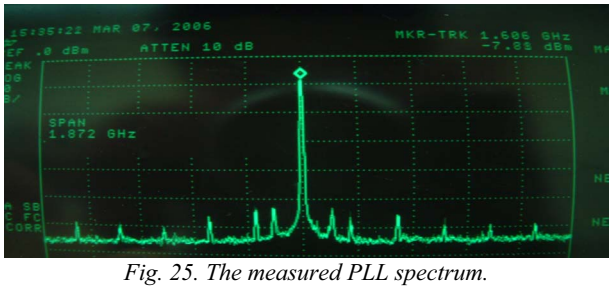

Fig. 25. The measured PLL spectrum.

CONCLUSIONS

A 3.2Gb/s 20:1 CML transmitter has been designed in 0.18um CMOS technology, and has been fabricated in separate chips due to chip area limitation. We proposed a dual phase shift register multiplexer that can be used to implement any even number of N to 1 serialization. The dual phase from the PLL can reduce the clock jitter effect due to the rising and falling sampling in the multiplexer. The total power consumption is 104 mW.

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THE AUTHORS

Prof. Ching-Te Chiu is with Dept. of Computer Science, National Tsing Hua University, Hsinchu, Taiwan. Prof. Jen-Ming Wu, Prof. Shuo-Hung Hsu, Prof. Yarsun Hsu, Chen-Hsiang Hsiao, Min-Sheng Kao, Chih-Hsien Jen, Yu-Hao Hsu and Ping-Lin Yang are with Dept. of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan.

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