A 6.5kV ESD-Protected Low Noise Amplifier in 65-nm CMOS

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***Abstract*—A new ESD topology is proposed for RF low-noise amplifier (LNA). By using the modified silicon-controlled rectifier (MSCR) in conjunction with a P^+/N-well diode clamp, a 5.8-GHz LNA with 6.5-kV ESD protection circuit is demonstrated by a 65-nm CMOS technology. Compared with the reference design, the new topology enhances the ESD level from 3.5 kV to 6.5 kV for human body model (HBM) while the noise figure (NF) is only 0.13 dB higher. Under a supply voltage of 1.2 V and drain current of 6.5 mA, the proposed ESD-protected LNA has a NF of 2.57 dB with an associated power gain of 16.7 dB. The input third-order intercept point (IIP3) is -11 dBm and the input and output return losses are below -15.9 dB and -20 dB, respectively.**

***Index Terms*—CMOS, ESD, RF, SCR, TLP, Low noise amplifier.**

I. Introduction

With the rapid shrinking of the feature size in CMOS technology, the gate oxide thickness reduces accordingly leading to the critical concerns for electrostatic discharge (ESD) protection design in integrated circuits. A good ESD design should provide sufficient immunity to the ESD stress, but not affect the signal under normal operation conditions. For RF applications, the tradeoff between the ESD robustness and circuit performance has to be taken into account. In general, if high RF performance is required, the design of endurable ESD protection for large ESD current stress becomes more challenging [1].

The double-diode scheme typically employed for RF ESD protection has the advantage of simple design and high ESD current capability [2]. However, this configuration does not provide a direct ESD bypass path during the positive ESD zap with V_{SS} grounded (PS mode). This can be an important issue in the design of system-on-chip (SOC) using advanced technology. With the multi-power domain circuitry and thus long power bus routes, the increased parasitic resistances result in a large IR voltage drop and the thin gate oxide is exposed under a high clamped voltage stress. To improve the ESD level, it is highly desirable to have the direct discharge paths to ground to minimize the resistance of the ESD current path [3].

The silicon-controlled-rectifier (SCR) with high current capability has also been widely used as the ESD protection block, which provides a directly discharge path to ground for the PS mode. However, the high switching voltage, low turn-on speed and transient-induced latch-up issues need to be overcome, especially for nano-meter CMOS technologies [3]. Previously published results proposed various approaches to improve these problems. A substrate-triggered SCR can quickly trigger on when the current applied to the substrate of the SCR device [4]; for a gate-grounded nMOS triggered SCR, an nMOS transistor is used as an external trigger device to quickly trigger on SCR [5]. However, the ESD current still needs to propagate through a long path in the PD mode. As a result, the parasitic resistance of the ground buses causes a large IR voltage drop leading to the thin gate oxide exposed under a high clamped voltage stress. It is highly desirable to design an ESD protection block with directly discharge paths to the power (both PS and PD modes) to minimize the resistance of ESD current path [2].

In this study, we proposed a new ESD network topology using the modified SCR in conjunction with a P+/N-well diode clamp and a gate-driven power clamp for RF low noise amplifier (LNA) ESD design. The proposed design provides direct discharge paths to the power. Being the first active block in RF receiver, the ESD protection is of critical importance for the LNA. The measured results demonstrate the proposed ESD-protected LNA can enhance ESD performance up to 6.5 kV for the HBM with only 0.13-dB noise figure and 0.7-dB power gain degradation compared to those of the SCR-only LNA. To the best of our knowledge, the proposed ESD-protected LNA presents the highest ESD level among the published works in 65-nm CMOS technology.

II. Circuit Topology

A. ESD Configuration

Fig. 1 shows the architecture of the proposed ESD network together with the amplifier circuit Fig. 1 also indicates the two ESD bypass current paths for the PS and PD modes. Differing from the conventional SCR topology, the proposed ESD

network topology can provide direct ESD paths to V_{DD} and V_{SS} simultaneously. In other words, the critical PS and PD modes are both enhanced owning to the prevented large IR drop from the power bus resistances. In the PS mode, there are two ESD current paths PS1 and PS2 including a path PS1 through the modified-SCR and an auxiliary path PS2 with P+/N-well diode together with a power clamp. Similarly, there are also two ESD current paths PD1 and PD2 for the PD mode. With the proposed ESD network design, both of the PS and PD modes find the direct paths to the ground and the additional ESD paths further enhance the ESD protection capability.

The complete 65-nm LNA with proposed ESD network is shown in Fig. 2. The P+/N-well diode D_P is employed as a direct ESD path for the PD mode with the dimension of 0.6 μm and 40 μm in length and width, respectively. The modified SCR is employed as a dual-direct ESD path for the PS and NS modes, which the N-well diode (D_N) with the geometry of 8-μm square is used as the direct ESD path for the NS mode. The transistor M_T functions as a trigger source with a total channel width of 64 μm and a channel length of 0.15 μm. The large trigger current resulted from the large M_T can reduce the trigger voltage. Note that the diode chain (D_1, D_2, and D_3) is used to ensure a sufficient holding voltage (V_H) to improve latch-up immunity. There is a trade-off between ESD performance and latch-up immunity for the diode chain. In normal RF operation, the trigger voltage of the diodes must be sufficiently high such that the chain does neither leak nor trigger the SCR. On the other hand, during the ESD event, the increased number of diodes also increases the SCR ESD trigger voltage and thus limits the ESD performance. It should be notice that the gate-driven power clamp can effectively minimize the voltage drop along the ESD current bypass path. In this design, the total capacitance is about 75 fF at the RF input, which shows no obvious impacts on the LNA performance at 5.8 GHz of the RF operation frequency.

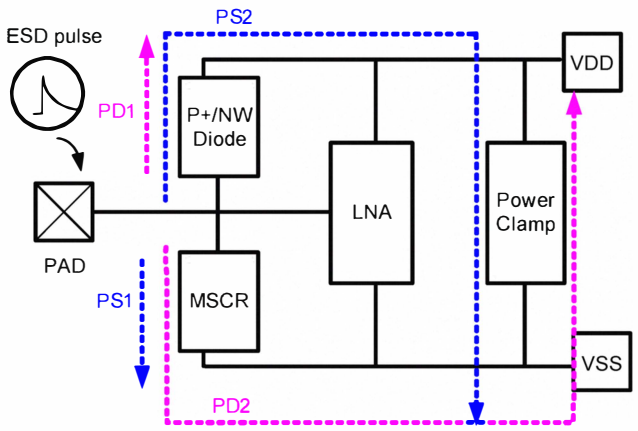

Fig.1. Proposed ESD network consisting of modified-SCR (MSCR) with a diode clamp (P+/N-well), and power clamp

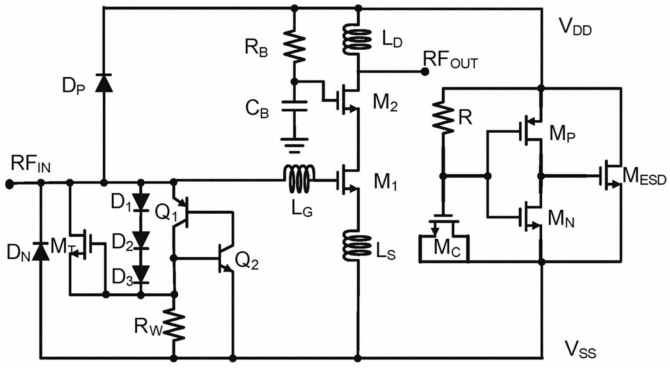

Fig.2. Complete circuit scheme including the proposed ESD-protected LNA in a 65-nm CMOS technology.

B. LNA Configuration

Fig. 2 shows that a cascode configuration is employed for the LNA, in which the inductive degeneration is applied for the common-source stage. The cascode design can not only improve the reverse isolation but also eliminate the Miller effect. The ESD blocks are co-designed with the LNA input matching network including the gate inductor L_g and the source inductor L_s. The L_s and L_g are designed to make the real part of the input impedance matching to 50 ohm at the desired operating frequency. The inductor L_d functions as the inductive peaking and also output matching to 50 ohm. The gate terminal of M_2 is connected through the RC bias circuit R_b and C_b instead of directly tied to V_{DD} to have a more robust ESD performance and AC ground.

III. Results and Discussion

The proposed ESD-protected LNA using modified SCR conjunction with P+/N-well diode and the power clamp are realized in a 65-nm CMOS process. A reference LNA design with SCR-only is also implemented for comparison. The RF characteristics have been measured on-wafer. The ESD performance is also tested on-wafer using *Transmission line pulse* (TLP) test.

A. RF measurements

The LNAs are biased under a 1.2 V supply with an associated drain current of 6.5 mA. The measured S-parameters S_{11} and S_{21} of ESD-protected LNAs are both shown in Fig. 3. With the well-designed ESD circuits, the frequency responses of both cases are almost identical. The power gain can achieve 16.7 dB at 5.8 GHz, which only drops by 0.7 dB compared with the reference ESD-protected LNA. Input insertion loss below –15 dB is also obtained for both cases, which

demonstrates the successfully designed input-matching network. Fig. 4 shows the measured noise figures. Excellent noise figure around 2.57 dB at 5.8 GHz is achieved for the proposed ESD–protected LNA, which is only 0.13-dB higher than the reference design. To evaluate the circuit linearity, the input third-order-intermodulation (IM3) is measured. A two-tone test using 5.8025 GHz and 5.7975 GHz is performed to measure the input third-order intercept point (IIP3). The measured results of –11 dBm also indicate that the proposed ESD circuit does not have impact on the circuit linearity.

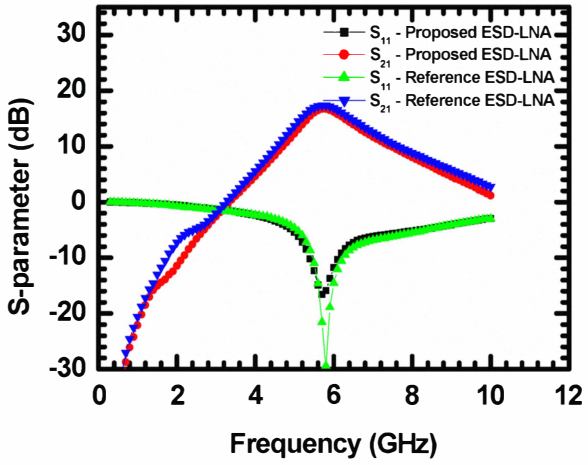

Fig.3. Measured S_{11} and S_{21} of ESD-protected LNA.

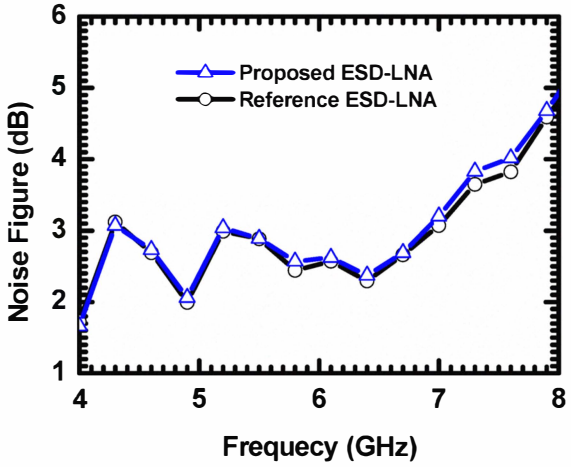

Fig.4. Measured noise figure of ESD-protected LNA.

B. ESD testing results

Fig. 5 shows the *Transmission line pulse* (TLP) test results of the RF_{IN}-V_{SS} path (PS mode). The sudden increase of the leakage current indicates that a second breakdown current of proposed ESD-protected LNA up to 4.3 A can be achieved corresponding to an ESD level of 6.5 kV, while that for the reference ESD-protected LNA is about 2.4 A corresponding to an ESD level of only 3.5 kV. The reference ESD-protected LNA illustrates the pure snapback turn-on behavior, and the triggered voltage (V_T) is about 4.7 V that is lower than the gate oxide breakdown voltage. The figure also indicates that the snapback holding voltage (V_H) is about 1.47 V, which is higher than V_{DD} (1.2V) to avoid latch-up. Particularly, the proposed ESD-protected LNA demonstrates that the P+/N-well diode with power clamp turn-on first in linear-mode, and then the modified-SCR turn-on in the snapback mode also at about 4.7 V, leading to snapback at about 3.72 V with respect to the TLP current of 3A. Table I compares this work with other published RF ESD-protected LNAs. The proposed ESD-protected LNA achieves highest ESD performance with comparable NF by a 65-nm technology with the thinnest gate oxide. The ESD protection only increases the noise figure from 2.44 to 2.57 dB in our design.

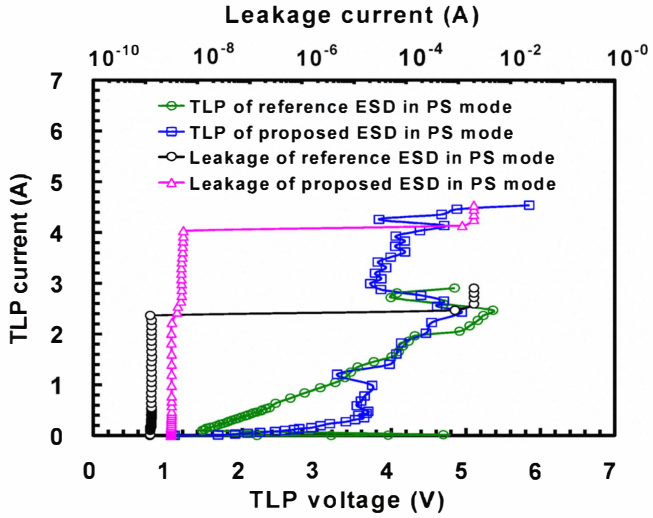

Fig. 5. Measured high current TLP I-V curves.

IV. Conclusion

In this paper, we proposed a new ESD network topology for RF ESD design using the modified SCR in conjunction with a P+/N-well diode clamp and a gate-driven power clamp. The design provides direct ESD discharge paths to both V_{DD} and V_{SS}, which is suitable for multi-power domain design for SOC. The measured results demonstrate the proposed ESD-protected LNA can enhance the ESD performance up to 6.5 kV for the HBM with only 0.13-dB noise figure and 0.7-dB power gain degradation compared with the SCR-only LNA. To the best of our knowledge, the proposed ESD-protected LNA presents the highest ESD level among the published works in 65-nm CMOS technology.

TABLE I

PERFORMANCE COMPARISON OF RF LNA W/WO ESD WITH PRIOR ART

Ref.	Technology (nm)	Freq (GHz)	NF (dB)	P_{DC} (mW)	S_{21} (dB)	S_{11} (dB)	IIP3 (dBm)	HBM (kV)
This work	**65**	**5.8**	**2.57**	**7.8**	**16.7**	**-15.9**	**-11**	**6.5**
			2.44	**7.8**	**17.4**	**-29.4**	**-11**	**3.5**
[6]	65	5.8	1.9	8.4	18	-16	-11	4
			1.85	8.4	18.5	-16.3	-10	--
[7]	90	5.5	2.9	9.72	13.3	-14.4	-3	2
			2.7	9.72	12.3	-10.3	-3	--
[8]	90	2.4	3.2	12.9	21.9	-10.9	-11	4
			2.56	12.9	22.1	-12.6	-10.83	--
[9]	90	5.5	3.4	9	12	-24	0.4	5.5
			3.2	9	12.6	-18	-0.5	2.5
			3	9	13	-18	-0.4	0.5
			3.5	9	16.2	-11.5	-5	1.9
[10]	130	5.5	2.5	6.6	12.4	<-10	-9	5
[11]	150	2.4	2.77	4.65	12.1	-19	2.4	2
		2.46	2.36	4.65	14	-18.5	-2.2	--

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