A Low Noise Amplifier Co-designed with ESD Protection Circuit in 65-nm CMOS

Ming-Hsien Tsai, Shawn S. H. Hsu, and Kevin K.W. Tan
Dept. of Electrical Engineering and Institute of Electronics Engineering,
National Tsing Hua University, Hsinchu, Taiwan

***Abstract*—By means of co-design ESD protection circuit as the low noise amplifier (LNA) input matching network, a 5.8-GHz LNA with excellent ESD and noise performances is demonstrated by a 65-nm CMOS technology. The diode-based ESD design with a power clamp can achieve 4 kV human body model (HBM) performance while the noise figure (NF) is only 0.05 dB higher than that of the LNA without the extra ESD blocks. Under a supply voltage of 1.2 V and drain current of 7 mA, the ESD-LNA has a NF of 1.9 dB with an associated power gain of 18 dB. The input third-order intercept point (IIP3) is -11 dBm and the input and output insertion losses are below -16 dB and -20 dB, respectively.**

***Index Terms*—ESD, Low noise amplifier, CMOS, power-clamp.**

I. Introduction

FOR an radio frequency (RF) receiver, the low noise amplifier (LNA) is often exposed to the risk of electrostatic charge directly. Electrostatic discharge (ESD) protection circuit is therefore of extreme importance for RF LNA design for practical applications. Conventional ESD protection circuit usually consists of large grounded-gate NMOS (GGNMOS) structures with a series resistor to clamp the current, and the ESD circuits are often employed in the IC by "plug-and-play" without considering the impact of the parasitics on circuit performance. This can severely degrade the circuit performance especially for RF LNA design, in which the ESD protection circuit can affect input matching network and degrade both noise figure and gain. The reduced gate oxide thickness and the lowered breakdown voltage as the CMOS technology continuously scaling also make the design of ESD protection circuit for RF applications more challenging [1].

Studies about ESD protection circuits for RF applications have been reported . A tuning inductor was employed to cancel the effect of the capacitive ESD block by a parallel LC resonance [2]-[3]. The ESD protection devices become virtually invisible when normal operation, while the major drawback of these schemes is the additional on-chip inductors consume a large chip area. A distributed ESD protection was also proposed [4], which demonstrated good ESD performance at the expense of using long transmission lines between segments to achieve a suitable inductance.

In this study, we proposed an LNA co-designed with the ESD protection circuits. Differing from previous works with LC resonance to minimize the effect of ESD capacitances, the ESD blocks are utilized as a part of the input matching network directly. To achieve good RF performance and meet the ESD specification simultaneously, the diode-based design with a power clamp is employed. The P+/NW and N+/PW shallow-trench-isolation (STI) diodes are selected for the ESD blocks and co-designed with the LNA input matching network. In addition, the linear gate-driven mode power clamp is employed to provide an efficient detection on ESD events, which is beneficial for the core transistors with a low gate-oxide breakdown. The measured results demonstrate a robust 4 kV HBM ESD performance with only a 0.05 dB noise figure degradation. To the best of our knowledge, an LNA with high ESD performance while maintaining low NF has not been demonstrated yet by a 65-nm RF CMOS technology.

II. Circuit Topology

A. ESD Protection Circuits

Fig. 1 shows the ESD protection scheme employed in this design which consists three components, namely the diodes D_n and D_p, and also the power clamp. The figure also indicates the discharge paths for the four different ESD testing modes, i.e., positive (PD mode) and negative (ND mode) to V_{DD}, and positive (PS mode) and negative (NS mode) to V_{SS}. When a pin-to-pin ESD zapping occurs on the circuit, the diodes function together with the power clamp circuit to provide a low-impedance path to discharge the electrostatic current.

The diodes at the input of LNA play an important role for the ESD discharge paths, which are critical for the input matching network. The diodes with the P+/NW and N+/PW structures surrounded by STI are utilized for D_p and D_n, respectively. Fig. 2 shows the cross section view of the P+/NW STI diode. For an area efficient design, the geometry of diode has a large L/W ratio. Under a fixed chip area, as the total perimeter increases, the overall current handling capability can be enhanced associated with a reduced parasitic resistance. With a double-diode configuration (D_p and D_n), one element is forward biased and the other is reverse biased during an ESD event, which can compensate for the voltage dependence of the diode parasitic capacitance and lessen the impact of the DC voltage swing. Moreover, the power clamp is placed as close as possible to the RF input pins to reduce the interconnect resistance and the associated voltage drop.

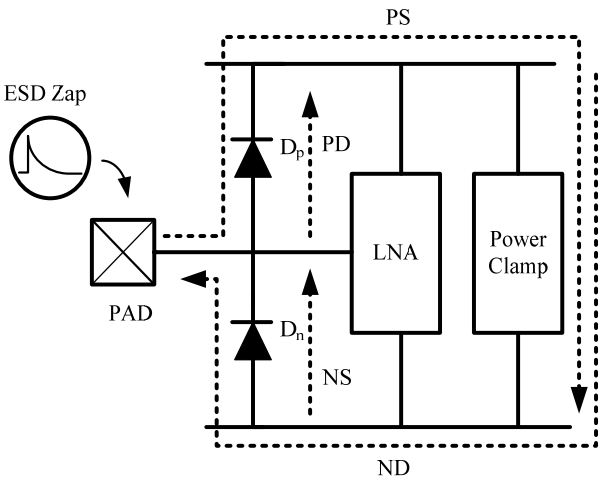

Fig. 1. ESD blocks for RF input including double-diode protection in conjunction with the power clamp circuit.

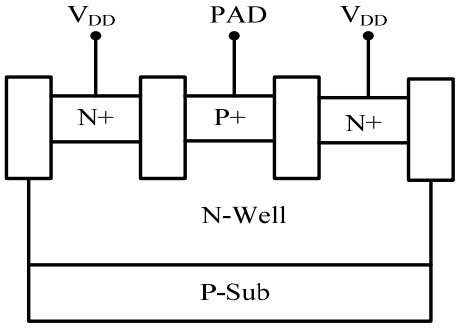

Fig. 2. Cross section of the P+/NW STI diode.

B. LNA Configuration

Fig. 3 shows the complete circuit of the proposed 65-nm LNA with the ESD protection scheme. A cascode configuration is employed for the LNA, in which the inductive degeneration is applied for the common-source stage. The cascode design can not only improve the reverse isolation but also eliminate the Miller effect. The transistors M1 and M2 have the gate widths of 80 μm and 64 μm, respectively. In order to carry a 2.7 A ESD current for 4 kV HBM ESD performance (tested under 1.5 kΩ to simulate human body impedance) while maintaining the RF performance, the STI diodes are co-designed with the LNA input matching network including the gate inductor L_g and the source inductor L_s. Selection of the diode size is a trade-off between the ESD rating and the input capacitive parasitics. After the geometry of the diodes decided, L_s and L_g are co-designed to make the real part of the input impedance matching to 50 ohm at the desired operating frequency. Note that L_s can effectively change the real part of the input impedance. Also, L_g can take care of the additional parasitics introduced by D_p and D_n. The inductor L_d functions as the inductive peaking and also output matching to 50 ohm. The inductances of 0.4, 5, and 2.9 nH are used for L_s, L_g, and L_d, respectively.

The gate terminal of M_2 is connected through the RC bias circuit R_b and C_b instead of directly tied to V_{DD} to have a more robust ESD performance and AC ground. As also shown in the figure, the power clamp is realized by an RC-triggered topology with the multi-finger transistors MN, MP, and MESD of a relatively large size, where MESD is even up to thousands of μm. A strong power clamp can effectively minimize the voltage drop along the ESD current bypass path. During the ESD zap occurs (PS and ND modes), the MESD transistor will turn on to effectively deliver the large ESD current.

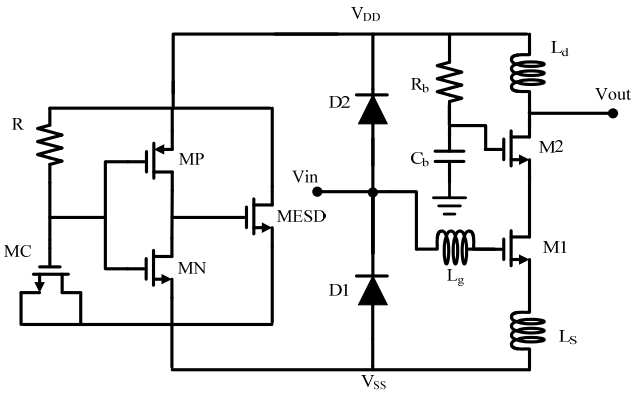

Fig.3. Complete circuit scheme including the ESD protection blocks of the proposed LNA in a 65-nm CMOS technology.

III. Results and Discussion

The LNA with ESD protection circuits using STI diodes and the power clamp are designed and verified in a 65-nm CMOS process. A reference design without the ESD blocks is also implemented for comparison. The RF characteristics such as noise figure and S-parameters have been measured on-wafer using GSG probes from 1 GHz to 10 GHz. The ESD performance is also tested on-wafer using the HBM zap stress.

A. RF measurements

The LNAs are biased under a 1.2 V supply with an associated drain current of 7 mA. The measured S-parameters S_{11} and S_{21} of LNA with and without ESD protection are both shown in Fig. 4. With the well-designed ESD circuits, the frequency responses of both cases are almost identical. The power gain can achieve 18 dB at 5.8 GHz, which only drops by 0.5 dB compared with that without the ESD protection. Input insertion loss below –16 dB is also obtained for both cases, which demonstrates the successfully designed input matching network in the ESD-LNA. Fig. 5 shows the measured noise figures. Excellent noise figure around 1.9 dB at 5.8 GHz is achieved for the ESD–protected LNA, which is only 0.05-dB higher than the reference design. A two-tone test using 5.8025 GHz and 5.7975 GHz is performed to measure the input third-order intercept point (IIP3) as shown in Fig. 6. The measured results of –11 dBm and –10 dBm also indicate that the ESD protection circuit does not have significant impact on the circuit linearity.

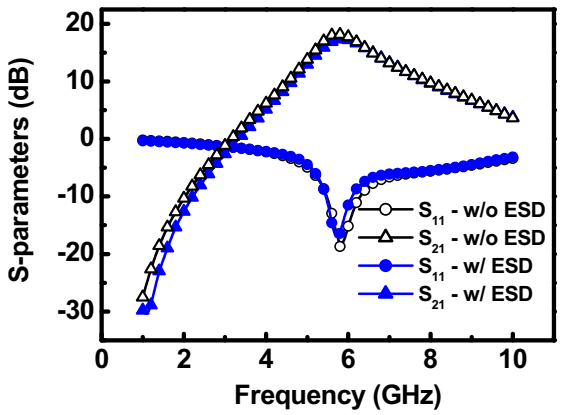

Fig. 4. Measured S_{11} and S_{21} of LNA with/without ESD protection.

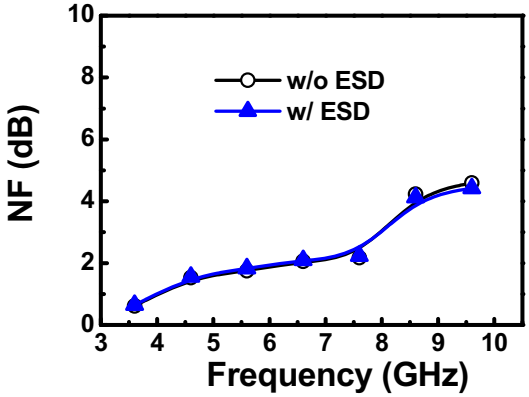

Fig.5. Measured noise figure of LNA with/without ESD protection.

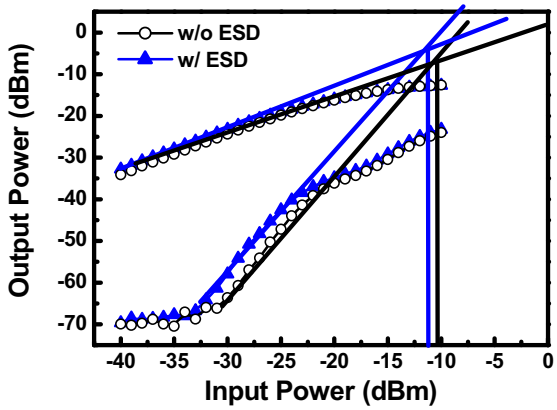

Fig. 6. Measured linearity of LNA with/without ESD protection under a two-tone test.

B. ESD testing results

A commonly used measure for ESD protection is the HBM test, which consists of a charged capacitance of 100 pF, and is discharged through a 1.5 kohm resistor connected to the DUT. As commonly used for the ESD standard, a 2 kV HBM ESD level refers to a current level of 1.34 A. The ESD test combination is summarized in Table I. As can be seen, the worst HBM ESD performance occurs in the ND mode, while it still can pass a 4-kV ESD level, namely failed at 4.5 kV (0.5 kV/step in the test). For the LNA without ESD protection, the circuit failed at only 0.5 kV. Table II compares the published RF LNAs with/without ESD protection circuits. The proposed LNA achieves the lowest NF with comparable or even better ESD performance by a 65-nm technology with the thinnest gate oxide. The ESD protection only increases the noise figure from 1.85 to 1.9 dB in our design.

TABLE I
SUMMARY OF ESD TEST COMBINATION

HBM	ESD Level (kV)
PD mode	4.5
PS mode	4.5
ND mode	4.0
NS mode	4.5

TABLE II
PERFORMANCE COMPARISON OF RF LNA W/WO ESD WITH PRIOR ART

Ref.	Technology (nm)	Freq (GHz)	NF (dB)	P_{DC} (mW)	S_{21} (dB)	S_{11} (dB)	IIP3 (dBm)	HBM (kV)
This work	65	5.8	1.9	8.4	18	-16	-11	4
			1.85	8.4	18.5	-16.3	-10	--
[8]	90	5.5	2.9	9.72	13.3	-14.4	-3	2
			2.7	9.72	12.3	-10.3	-3	--
[9]	90	2.4	3.2	12.9	21.9	-10.9	-11	4
			2.56	12.9	22.1	-12.6	-10.83	--
[10]	90	5.5	3.4	9	12	-24	0.4	5.5
			3.2	9	12.6	-18	-0.5	2.5
			3	9	13	-18	-0.4	0.5
			3.5	9	16.2	-11.5	-5	1.9
[11]	130	5.5	2.5	6.6	12.4	<-10	-9	5
[12]	150	2.4	2.77	4.65	12.1	-19	2.4	2
		2.46	2.36	4.65	14	-18.5	-2.2	--

IV. CONCLUSION

In this study, we proposed a co-designed methodology and demonstrated a 5.8-GHz LNA with excellent ESD and noise performance. The LNA was fabricated in a standard 1P6M 65 nm CMOS process and showed a low noise figure of 1.9 dB and a high power gain of 18 dB with a minimum 4.0 kV ESD performance. With carefully consideration of the ESD blocks

during the RF design, the RF performance of the LNA was virtually unaffected by the ESD protection circuit. The NF only increased by 0.05 dB and the input matching maintained below -16 dB with the additional ESD blocks.

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