A 24-GHz Low-Noise Amplifier Co-Designed With ESD Protection Using Junction Varactors in 65-nm RF CMOS

Ming-Hsien Tsai[1,2], Shawn S. H. Hsu[1], Fu-Lung Hsueh[2], Chewn-Pu Jou[2], Tzu-Jin Yeh[2], Jun-De Jin[2], and Hsieh-Hung Hsieh[2]

[1]Dept. of Electrical Engineering and Institute of Electronics Engineering,
National Tsing Hua University, Hsinchu, Taiwan
[2]Design Technology Division,
Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

***Abstract*—By means of co-designed methodology, a 24-GHz low-noise amplifier, utilizing junction varactors as ESD protection, is first demonstrated by a 65-nm CMOS technology. The ESD protection capability of the junction varactors with multi-finger topology is characterized in details by transmission line pulse (TLP) measurements. Under a 1.2-V supply voltage and a 5.8-mA drain current, the proposed LNA achieves a 1.4-A TLP failure level, corresponding to an over 2-kV human body model (HBM) ESD protection. The LNA presents a lowest noise figure of 2.8 dB at 23.5 GHz and a peak power gain of 14.3 dB at 24 GHz, respectively. The input third-order intercept point (IIP3) is -5 dBm and the input and output return losses are both greater than 10 dB. To the best of our knowledge, this is the first attempt using junction varactors as the ESD device in 65-nm CMOS.**

***Index Terms*— electrostatic discharge (ESD), junction varactor, low-noise amplifier (LNA), radio frequency (RF).**

I. INTRODUCTION

RAPID scaling of the feature size has made CMOS technology the most attractive candidate for system-on-chip (SOC) applications due to high integration level, high operation frequency, and low cost [1]-[4]. Recently, commercial applications use K-band (18 to 26.5 GHz) to realize car radars in CMOS technology [5]-[12]. In such a system, the low noise amplifier (LNA) is often exposed to the risk of electrostatic charge directly. The parasitic effect induced by ESD protection degrades the RF performance of the low-noise amplifier, which becomes more significant as the operation frequency increases. For achieving an overall good system performance with adequate reliability, the electrostatic discharge (ESD) protection is a major concern and should be taken into consideration at the early design stage, especially for the design using advanced CMOS technology with a very thin gate oxide [1]-[4], [13], [14].

Different ESD protection devices designed for RF applications have been reported. The silicide-blocked grounded-gate NMOS (GGNMOS) devices are commonly used in bulk CMOS [15]. However, the large drain to substrate capacitance and parasitic effects limit their high-speed applications. The poly-silicon silicon-controlled rectifier (SCR) devices have the advantage of low-capacitance compared with conventional SCR devices [16]. However, a major drawback is the addition process of the field oxide formation, which increases the cost. The gated diodes have the advantages of lower on-state resistance and fast turn-on time. However, it includes a larger parasitic capacitance per unit width than the shallow-trench-isolation (STI) diode [17]. Differing from the commonly used ESD devices in previous studies, we propose to use the RF junction varactor for ESD protection in this design. The junction varactors are usually utilized as the voltage-dependent tunable capacitors in VCO design or employed for tunable matching network for dynamic load modulation of high power amplifiers [18], [19].

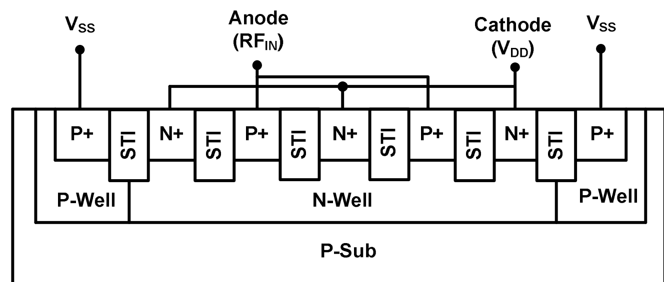

Fig. 1. The cross section view of a junction varactor with multi-finger topology.

In this design, the junction varactors are co-designed with the low-noise amplifier in 65-nm CMOS technology. With accurate scalable RF models, the junction varactors are carefully included as a part of the matching network resulting in an excellent noise figure. Under a supply voltage of 1.2V and an associated drain current of 5.8 mA, the ESD-protected LNA presents a peak power gain of 14.3 dB at 24 GHz and a lowest NF of only 2.8 dB at 23.5 GHz, respectively. The LNA also demonstrates a 1.4-A TLP failure level, corresponding to an over 2-kV HBM ESD protection. To our best knowledge, using RF junction varactors for LNA ESD protection has not been reported in previous publications.

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II. CIRCUIT TOPOLOGY

A. Junction Varactors Design for ESD Protection

Fig. 1 illustrates the cross-section view of the finger-type junction varactor. In contrast to the application for voltage-dependent tunable capacitors or tunable matching network, the junction varactors designed for ESD protection must be able to sustain a large ESD current. The varactors are modified by adding sufficient vias and using large metal widths in both terminals along the ESD paths for small on-resistance and high failure current (It_2), to prevent the electron-migration issue. Under a fixed device area, the multi-finger topology is adopted to sustain a high ESD current with reduced parasitic resistances and easy metal routing.

Transmission line pulse (TLP) measurements are often used to evaluate the ESD protection levels. The ESD pulse of a 10-ns rise time with a 100-ns pulse width, generated by Barth 4002 TLP test system, is used to simulate the HBM ESD behavior. The secondary breakdown point It_2 is determined by a sudden increase of the leakage current. The relation between It_2 and the HBM ESD level (V_{HBM}) can be approximated as V_{HBM} (V) ~ It_2 (A) * R_{HBM} (Ω), where R_{HBM} (= 1.5 kΩ) is to describe the equivalent human body resistance. The ESD current capability of the junction varactors is investigated by varying the device width (W= 1, 2, and 5 μm) and finger number (N=25 and 50), as shown in Fig. 2. A minimum device length of 0.15 μm is selected to increase the total peripheral. As can be seen, for a fixed finger number (N), It_2 increases proportionally to the device width (W) due to the linear reduced on-resistance during ESD zapping; similarly, for a fixed device width (W), It_2 increases proportionally to the finger number (N). These experimental studies indicate that junction varactors can be utilized to achieve desired ESD protection level with proper selected sizes. By the estimated HBM ESD level from the TLP failure current, it is clear that the ESD robustness of the junction varactor increases with the device size, but increased device size also introduces more parasitic capacitances.

B. Design of ESD-Protected LNA using Junction Varactors

Fig. 3 shows the proposed ESD-protected LNA using the junction varactors in conjunction with a power clamp as ESD protection network. The LNA is designed as a cascode configuration with the inductive degeneration applied in the common-source stage. A single-stage topology is designed to prevent some unpredicted parasitic effects from the complicated layout. Besides, metal 1 and metal 2 cross pattern ground shielding is employed for interconnects to alleviate the signal attenuation and substrate coupling effect [20]. The input matching network includes junction varactors (also used as ESD devices) JV_T and JV_B, gate inductor L_G, source inductor L_S, and gate-source capacitor C_{GS}. The extra gate-source capacitor is used for achieving power-constrained simultaneous noise and input matching (PCSNIM) [21]. The drain inductor L_D is used for inductive peaking and also output matching. The power clamp consists of RC (resistor R_C and MOS capacitor M_C)

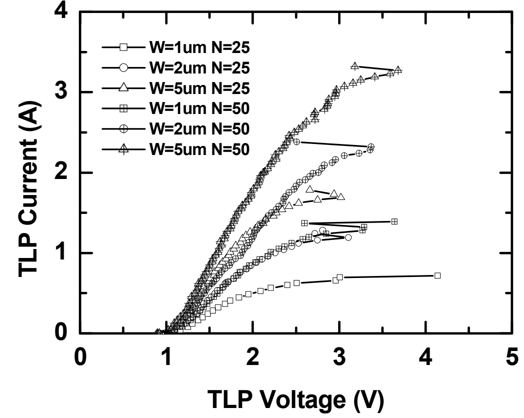

Fig. 2. The measured TLP currents of junction varactors with different sizes.

and inverter (M_P and M_N) to trigger the large NMOS (M_{ESD}), providing a low-impedance path from V_{DD} to ground. The design has the advantage of low turn-on voltage, and is suitable for advanced technology with a thin gate oxide thickness. The transistor M_{ESD} with a multi-finger topology has a large gate width and hence a low on-state resistance during ESD zapping. Since the power clamp is connected between the dc power rails only, the parasitic resistances and capacitances introduced from this block is not that crucial for the RF characteristics.

Using the ESD and matching network co-design approach, the size of M_1 and M_2, and the value of g_m are determined first with the considerations of power dissipation, gain, and noise characteristics. The ESD blocks are then designed based on the estimated protection levels. The shunt parasitic capacitances introduced by the ESD blocks are co-designed with L_G, L_S, and C_{GS} to achieve simultaneous noise and power matching. The ESD design using the junction varactors increases the parasitic capacitance by about 52 fF at the RF input, but is absorbed in the matching network and hence with a small impact on RF performance.

III. RESULTS AND DISCUSSION

The ESD-protected LNA was fabricated in a 65-nm CMOS low-power process. This process features a gate oxide thickness of ~ 2 nm and a minimum channel length of 60 nm for the core devices. The chip of the proposed ESD-protected LNA is with an area size of ~ 0.22 mm^2.

A. RF Measurements

The S-parameters and noise figures measurements were performed on-wafer by the PNA network analyzer and the noise figure analyzer, respectively. Under a supply voltage of 1.2 V and an associated drain current of 5.8 mA, the measured S-parameters (S_{11} and S_{21}) of the ESD-protected LNA are shown in Fig. 4. The LNA presents a peak power gain of 14.3 dB at the center frequency of 24 GHz. The input return loss is greater than 10 dB, demonstrating the successfully designed input-matching network. Fig. 5 shows the measured and

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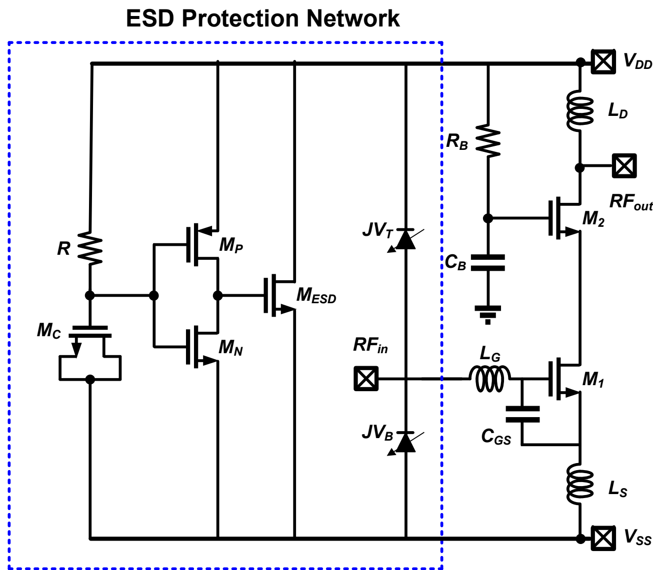

Fig. 3. The schematic of the proposed LNA consisting of the junction varactors and a power clamp for ESD protection.

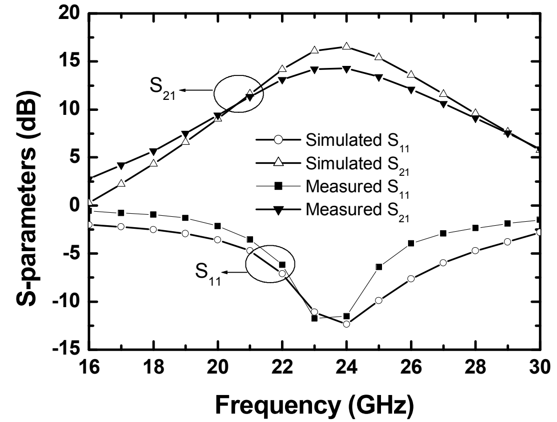

Fig. 4. Measured and simulated S_{11} and S_{21} of the ESD-protected LNA

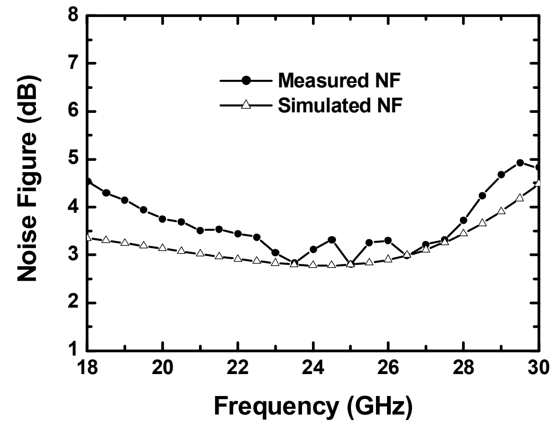

Fig. 5. Measured and simulated NFs of the ESD-protected LNA.

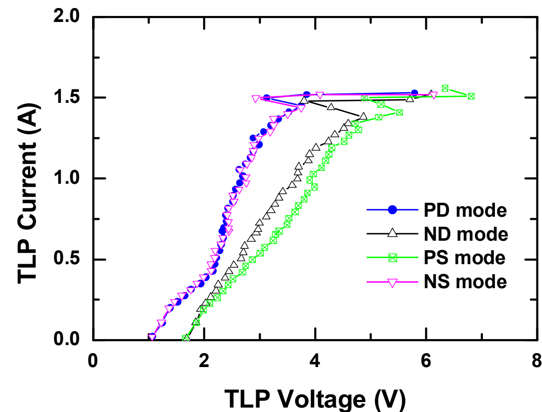

Fig. 6. Measured TLP *I-V* curves including four testing mode.

simulated noise figures. At the frequency of 23.5 GHz, a lowest noise figure of only 2.8 dB is achieved, which agrees well with the simulated result. In addition, the input third-order-intercept point (IIP3) was measured from a two-tone inter-modulation distortion test. The measured IIP3 of the ESD-protected LNA is about –5 dBm at the center frequency of 24 GHz. The result demonstrates that the junction varactors with accurate RF models are suitable for co-design of ESD protection and LNA circuits.

B. ESD Testing Results

The ESD testing was performed on-wafer by DC probes using the Barth 4002 transmission line pulse (TLP) test system. Fig. 6 shows the transmission line pulse (TLP) test results of different testing modes (PD, PS, ND, and NS) for the ESD-protected LNA [3], [4]. In the PD mode, the *I-V* curve presents a linear characteristic, indicating the ESD bypass current enters the RF input pad and flows through JV_T to V_{DD}. Note the *I-V* curve of the NS mode is almost identical to that for the PD mode, indicating the same ESD device size used for both JV_B and JV_T. In the PS mode, the *I-V* curve also illustrates a linear characteristic, suggesting the ESD bypass current travels through JV_T to V_{DD}, and flows to power clamp and then reaches V_{SS}. The *I-V* curve of the ND mode is close to the PS mode representing the same voltage drop of the junction varactor and power clamp. In the four testing modes, a minimum second breakdown current (It_2) up to 1.4 A is achieved, corresponding to an ESD level over 2.0 kV. Note the measured TLP *I-V* characteristic of power clamp is larger than 5.2 A, demonstrating the ESD performance is limited by junction varacters (ESD device at RF input pad). Table I compares this work with other published RF LNAs. The proposed LNA achieves a lowest NF of 2.8 dB under a power consumption of only 7 mW. The LNA also demonstrates an

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED RF LNAS WITH PRIOR ARTS

Reference	Tech. (nm)	Freq. (GHz]	Gain (dB)	NF (dB)	S_{11} (dB)	S_{22} (dB)	Power (mW)	IIP3 (dBm)	ESD (kV)
[5]	180 CMOS	22	10.1	4.3	-12	NA	7.2	-1.0	NA
[6]	180 CMOS	23.7	12.86	5.6	-11	-22	54	2.04	NA
[7]	180 CMOS	22	15.0	6.0	-22	NA	24	NA	NA
[8]	180 CMOS	24	13.1	3.9	-15	-20	14	NA	NA
[9]	180 CMOS	24	12.8	3.3	-7.5	-17	8	NA	NA
[10]	130 CMOS	24	14.0	5.0	-7.0	-15	18	-1.7	2.5
[11]	90 CMOS	24	7.5	3.2	-16	-30	10.6	NA	NA
[12]	350 SiGe	24	12.0	3.1	-5.4	-10.6	41	-1.8	1.5
This work	65 CMOS	24	14.3	2.8	-12	-13	7	-5.0	2.0

ESD level of 2 kV by 65-nm technology with the thinnest gate oxide compared with other published works.

IV. CONCLUSION

In this paper, an ESD-protected 24-GHz LNA was realized in 65-nm CMOS technology using the proposed RF junction varactors as the ESD devices. With the detailed investigation on the ESD protection capability, the modified RF junction varactors were co-designed as a part of the LNA matching network. Under a power consumption of only 7 mW, the LNA achieved an excellent NF of 2.8 dB and a peak power gain of 14.3 dB. Also, the LNA demonstrated a minimum 1.4-A TLP failure level, which is corresponding to an over 2-kV ESD protection.

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