Flicker Noise Characteristics in GaAs MOSFETs

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This study reports the flicker noise characteristics in GaAs-based MOSFETs for the first time. With the improvement in $Ga_2O_3(Gd_2O_3)$ insulators, GaAs MOSFETs reveal the possibility for high-speed and high-power applications, resulting from an electronic mobility that is about five times greater than that in Si, and the advantage of semi-insulating substrate. The DC and RF characteristics of GaAs-based MOSFETs have been demonstrated a current density up to 450mA/mm and a f_T and f_{max} of 17 and 60 GHz, respectively [1]. However, investigations of flicker noise on these devices, which is powerful to examine both the material and device qualities especially the interface/surface imperfections, have not been reported to date. In this work, flicker noise of GaAs MOSFETs is investigated, which provides valuable information on possible noise origins and directions to further improve the material quality and device performance.

Fig.1 shows the device structure o f a depletion-mode (D-mode) n-channel GaAs MOSFET, which consisted of an undoped GaAs buffer and a 900 Å GaAs channel layer with a Si doping concentration of 4×10^{17} cm^{-3}. The layers were epitaxially grown on (100) semi-insulating GaAs substrate using a multi-chamber MBE system. The gate dielectric (a mixture of Ga_2O_3 and Gd_2O_3) was deposited by electron-beam evaporation from a single crystal $Ga_5Gd_3O_{12}$ garnet. The ohmic and gate metals were AuGe/Ni/Au and Ti/Pt/Au, respectively. Fig. 2 presents the DC *I-V* curves for a 2-finger device with a W/L ratio of 200 μm/1 μm. The device demonstrated a well-defined pinch-off characteristics at V_{GS}= -1.5 V. The measured results also indicated a breakdown voltage higher than 10 V, which is substantially higher than typical Si-based MOSFETs and excellent for high-power applications.

Fig. 3 shows the normalized drain noise current spectral density as a function of gate bias under V_{DS} = 2.5 V. Compared to modern CMOS technology, the typical noise spectral density in 0.13-μm NMOS technology is in a range of 10^{-11}~10^{-9} Hz^{-1} (at 10 Hz, under similar bias conditions), which is comparable to the GaAs MOSFETs reported here. Fig. 4 plots the slope γ of the $1/f^{\gamma}$ characteristics as a function of the gate bias. It was found that the extracted values ranged from ~ 0.65 to 1, and also increases with the gate bias. Theoretically, the slope γ should be one based on the assumption of uniformly distributed traps. The observed trend of $\gamma < 1$ reveals that the trap density inside the insulator increases toward interface. Moreover, the gate bias dependence of γ suggests that trap distribution is also non-uniform as a function of energy. As the band bending increases with a higher gate bias, the amount of effective traps raise resulting an increased slope γ [2]-[3].

In summary, the flicker noise characteristics in GaAs MOSFET was investigated for the first time. The device showed a drain noise current density similar to that in modern CMOS technology. Studies on the bias dependence and the slope γ suggest that the main noise origin located close to the $Ga_2O_3(Gd_2O_3)$ insulator and channel interface. This study identified the possible flicker noise origins and locations, which provides a direction to further improve the material quality and device performance of GaAs MOSFETs.

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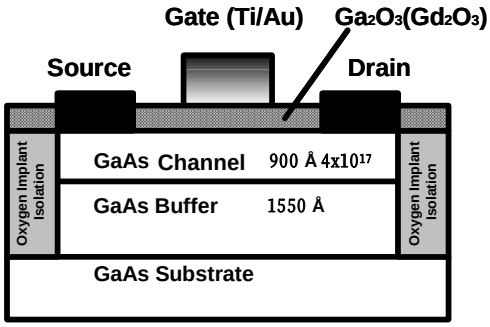

Fig. 1: The cross section of fabricated D-mode n-channel GaAs MOSFET's. The oxide layer thickness is 300 Å.

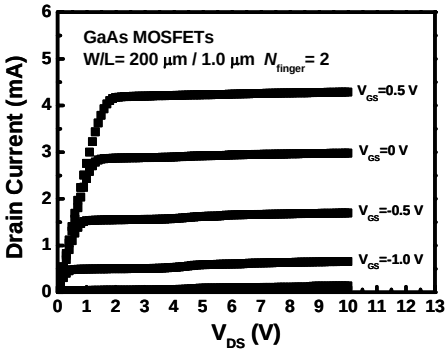

Fig. 2: The DC-IV curves for a two-finger GaAs MOSFET with W/L=200 µm/ 1 µm.

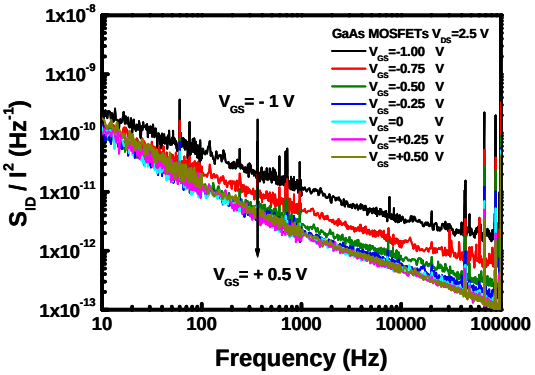

Fig. 3: Drain noise current spectral density for GaAs MOSFETs with V_{DS}=2.5 V and V_{GS} varies from -1 V to 0.5 V.

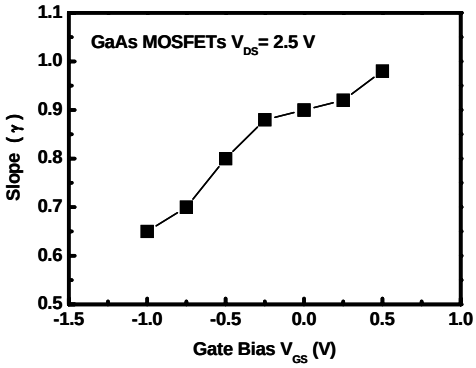

Fig. 4: The slope γ of the $1/f^{\gamma}$ noise characteristics as a function of V_{GS}. The drain was biased at 2.5 V.