ESD Protection Design for Microwave/Millimeter Wave Low-Noise Amplifiers

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***Abstract*—Different ESD design topologies suitable for microwave/millimeter wave low-noise amplifiers (LNAs) are reviewed, and the design tradeoffs and limitations of each topology are also discussed. In addition, a V-band LNA using the proposed Pi-type ESD block is demonstrated in 65-nm CMOS. A series ESD inductor together with two shunt ESD diodes and an bonding (probing) pad form a Pi-type network, acting like an ideal wideband 50-ohm transmission line with a loss of only 0.6 dB at 60 GHz. Under a power consumption of 27 mW, the ESD-protected LNA presents a 4.1-dB *NF* and 18.5-dB power gain at 60 GHz, respectively with a 3-dB bandwidth up to 7.7 GHz. The measured results also demonstrate a 2.5-kV Human-Body-Model (HBM) ESD protection. This LNA shows excellent FoMs compared with recently published results in a similar frequency range.**

***Index Terms*— CMOS, electrostatic discharge (ESD), low-noise amplifier (LNA), human body model (HBM), microwave, and millimeter wave (mm-wave).**

I. Introduction

With increasing demand for wide bandwidth and high data rate, the wireless communication systems operating at microwave/millimeter wave (mm-wave) frequencies have attracted a great attention for various applications [1]-[3]. CMOS transistors demonstrate the capability of high f_T and f_{max} under low power consumption owing to the rapid progress in technology, and have become the most suitable choice for realizing a fully integrated transceiver at such high frequencies. One design challenge for the microwave/mm-wave communication ICs in CMOS technology is the electrostatic discharge (ESD) protection. The small gate oxide thickness (only ~ 1−2 nm) and low gate oxide breakdown voltage (typical ~ 5−7 V) in modern CMOS technology make the device more vulnerable to ESD damage [4]-[5]. Also, the circuit characteristics are very sensitive to the parasitic components introduced by the ESD blocks in this frequency range, especially the low-noise amplifier (LNA) at the receiver front end.

In this paper, we will review and compare two general topologies of ESD protection design for RF circuits including the double-diode and LC-based topologies. The advantages and limitations of each ESD scheme will be discussed. Also, we propose a Pi-type ESD block to achieve a high performance V-band LNA with sufficient ESD robustness. Composed of one series inductor L_{ESD} and two equivalent shunt parasitic capacitors (one from the ESD diodes and the other from the pads), the ESD block is nearly transparent (loss ~ 0.6 dB from 50 to 66.5 GHz with input reflection coefficient < -15 dB) to the LNA core circuit in the frequency range of interest. The ESD-protected LNA demonstrates a 2.5-kV HBM ESD level with a 4.1-dB *NF* and a 18.5-dB power gain at 60 GHz, under power consumption of 27 mW.

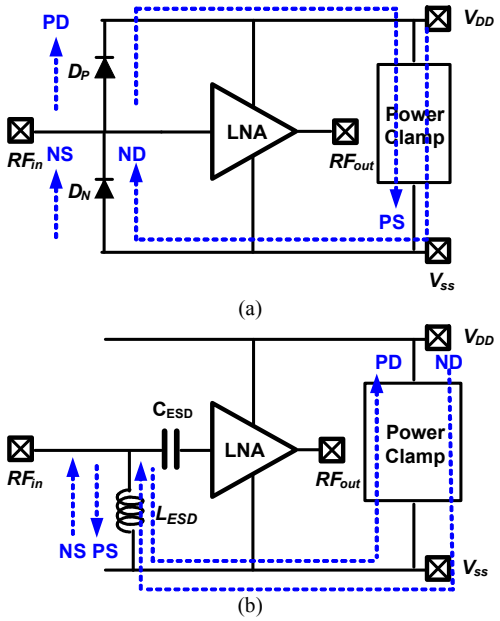

Fig. 1. Two general ESD protection design schemes for RF LNAs (a) double-diode topology (b) LC-based topology.

II. Review of ESD Protection Design for RF LNAs

The parasitic effects introduced by the ESD devices can seriously degrade the input reflection coefficient, noise figure, and gain of the RF LNA if not properly designed. The co-design approach by incorporating the ESD components as a part of the LNA matching network in the early design stage is helpful to achieve a high performance ESD-protected LNA at high frequencies. This concept can be applied to the following two general RF ESD topologies to obtain good LNA characteristics while maintaining a high ESD protection level.

A. Double-Diode ESD Protection Topology

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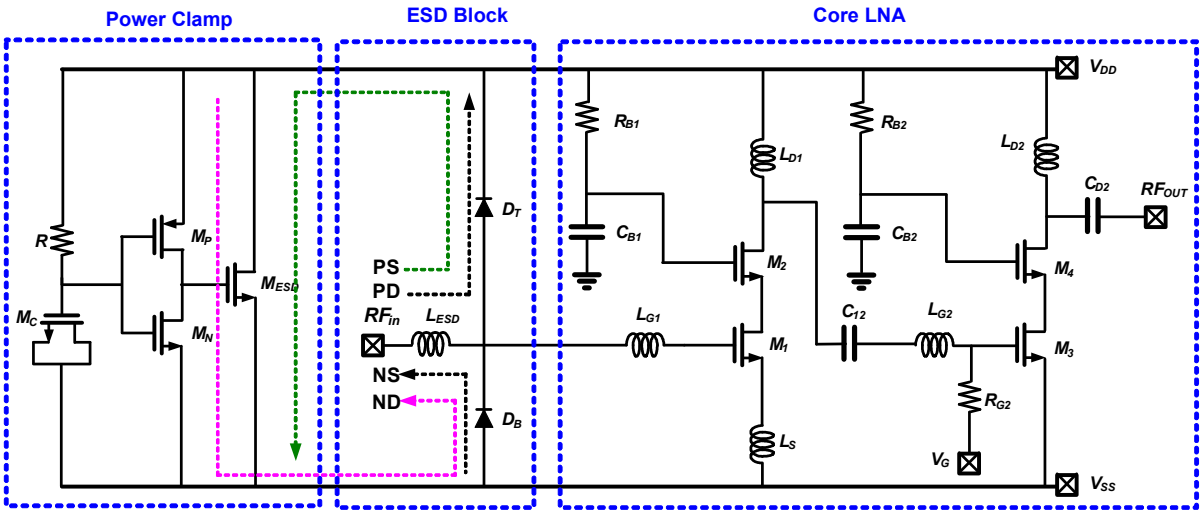

Fig. 2. Schematic of the proposed V-band LNA consists of the Pi-type ESD block, power clamp, and the LNA core circuit.

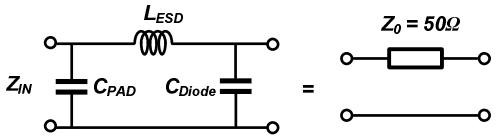

Fig. 3. Equivalent circuit of the Pi-type ESD block, which can be approximated as a 50-Ω transmission line.

Fig. 1(a) shows a widely used ESD protection configuration, constructed by a double-diode topology (D_P: P+/N-well diode; D_N: N-well/P-substrate diode) in conjunction with a power clamp [6]. The paths for the four ESD testing modes (NS, ND, PD, and PS) are also illustrated. Note the power clamp only provides a low-impedance path between V_{DD} and ground, which has no effects on circuit RF characteristics. In this topology, a tradeoff in general exists between the ESD parasitic capacitance and ESD protection level. If a more robust ESD protection is required, a larger parasitic capacitance will be introduced, resulting in more significant RF performance degradation. As mentioned, a better design methodology is to include the ESD diodes as a part of the LNA input matching network. By using the co-design approach, the ESD diodes with increased sizes are allowed, and the LNA performance and ESD robustness can be improved simultaneously.

One critical issue of including the ESD diodes in the LNA matching network is the requirement of accurate RF models of these diodes. We proposed using the scalable RF junction varactors for ESD design [5]. A dual-diode ESD protected LNA in 65 nm CMOS with an *NF* of only 2.8 dB and a Human-Body-Model (HBM) ESD protection of 2.1 kV is demonstrated at 24 GHz (K-band). Also, a third ESD diode, connected between the gate and source of the input common-source transistor, was introduced to provide an additional charge-device-model (CDM) protection. Measured results of a *NF* of 3.2 dB and a *Very Fast Transmission Line Pulse* (VFTLP) current level of 10.7 A can be obtained [5].

B. LC-based ESD Protection Topology

Fig. 1(b) shows the ESD protection scheme using a shunt inductor L_{ESD} and a series capacitor C_{ESD} with a power clamp

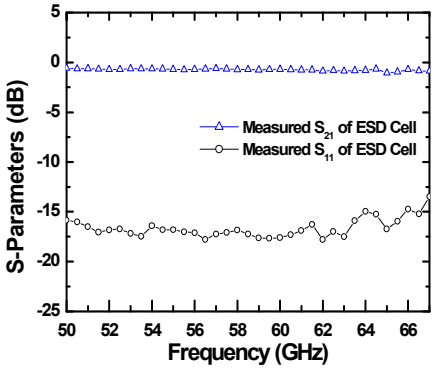

Fig. 4. Measured S_{11} and S_{21} of the proposed transparent Pi-type ESD block.

TABLE I
DEVICE PARAMETERS OF ESD BLOCK (L_{ESD} AND ESD DIODES)

ESD Block	L_{ESD} (pH)	D_T (μm^2)	D_B (μm^2)	Area (μm^2)
Size	110	18×0.6	20×0.6	208×130

[1]. Similar with the double-diode configuration, the best approach of using the LC-based ESD topology is to incorporate the ESD devices as a part of the matching network. The LC high-pass network acts like typical passive elements under normal RF operation. On the other hand, it provides a low-impedance bidirectional path to bypass the discharge current directly to the ground via L_{ESD} during an ESD event, and further blocks the ESD current by C_{ESD} to protect the core RF circuits. In practical design, a relatively large width and a small number of turns should be used for L_{ESD} to increase the current handling capability and reduce the parasitic resistance. Also, C_{ESD} can be implemented by MIM/MOM capacitor with a high breakdown voltage. Compared with double-diode configuration, the LC-based ESD design is more suitable for high frequency applications to reduce the chip size. However, an extremely high ESD protection level can be achieved with properly designed L_{ESD} and C_{ESD}, which is not limited by the increased operating frequencies. We have demonstrated LNAs at both K-band and V-band with HBM ESD levels up to 8 kV using the LC-based ESD topology [1], [2].

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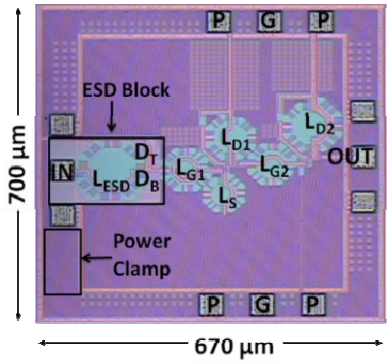

Fig. 5. Chip micrograph of the ESD-protected LNA.

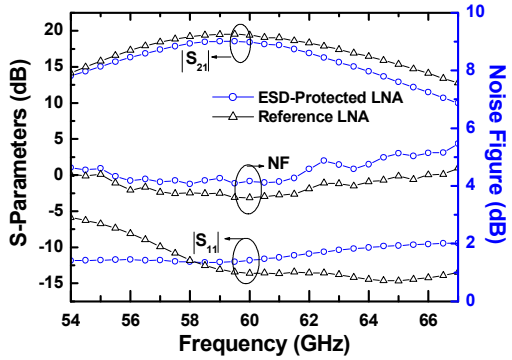

Fig. 6. Measured $|S_{11}|$, $|S_{21}|$, and *NF* of the ESD-protected LNA.

III. V-BAND LNA WITH PI-TYPE ESD PROTECTION

As mentioned previously, the co-design approach is suitable for achieving high performance ESD-protected LNAs in microwave/mm-wave applications. However, such a design methodology requires knowledge in both RF and ESD domains. An ESD block capable of plug-and-play is highly appreciated from RF designers' point of view. A Pi-type ESD block is proposed here for plug-and-play ESD protection. Based on this topology, a V-band LNA in 65 nm CMOS with a 2.5-kV ESD level and *NF* of only 4.1 dB is demonstrated.

A. Design of ESD Protection Network

Fig. 2 shows the detailed circuit schematic of the proposed ESD-protected LNA, where the ESD block is comprised of a series inductor L_{ESD} and two shunt ESD diodes D_T and D_B. Together with the input bonding (probing) pads, the ESD block can be equivalent as a Pi network. If the component values are carefully designed, the Pi network can be approximated as an ideal 50-Ω transmission line, as illustrated in Fig. 3. The design parameters of the ESD block are listed in Table I. With the known dependence of the ESD level on the ESD diode geometry and the associated parasitic capacitance C_{ESD}, the P-type (D_T) and N-type (D_B) shallow-trench-isolation (STI) diodes [6] were determined first to achieve a 2.5-kV HBM ESD level, which is 0.5 kV higher than the typical commercial standard of 2 kV for a safe design margin. By considering both the electro-migration effect and 50-Ω transmission line characteristic, the series L_{ESD} was designed as a half-turn spiral inductor to prevent high resistivity vias in the current discharge path. The thick top metal layer (3.4 µm in thickness) is used and the width of L_{ESD} is 6 µm. The Pi-type ESD block is formed together with the parasitic capacitance of the probing (bonding) pads, making the ESD block close to an ideal 50-Ω transmission line. Fig 4 shows the measured results of the ESD block only, including L_{ESD}, D_T and D_B, and the input pads. The insertion loss (S_{21}) is ~ 0.6 dB and the input reflection coefficient is < -15 dB in a wide frequency range.

B. Design of the V-band LNA

As also shown in Fig. 2, the core LNA employs a two-stage cascode topology, which has the advantages of reduced Miller effect and improved input/output isolation. The inductive source degeneration (L_S) is used in the first stage for simultaneous noise and power matching, together with L_{G1} forming the input-matching network. The inductive loads (L_{D1} and L_{D2}) are used for gain peaking in both stages. The capacitor C_{12} serves as the DC block between the two stages, which also works together with L_{G2} and L_{D1} as the inter-stage matching. The inductor L_{D2} and capacitor C_{D2} are also utilized as the output-matching network to 50-Ω for measurements. The transistor size is determined by investigating the noise and gain characteristics as a function of finger width and bias. A current density of ~ 0.25 mA/µm can be obtained under a gate bias of ~ 0.7 V in 65-nm CMOS technology [1], which is around optimal for low noise design. Based on this guideline and with excellent scalability of MOS transistors, M_1, M_2, M_3, M_4 are all designed to be 36µm in width.

IV. RESULTS AND DISCUSSION

The ESD-protected LNA was fabricated using a 65-nm CMOS process. Fig. 5 shows the chip micrograph, and the chip area is 0.47 mm^2 (including the probing pads). The reference LNA without ESD protection was also fabricated for comparison.

A. RF Measurement Results

The S-parameters and noise measurements were performed by the Agilent network analyzer and noise figure analyzer, respectively. Fig. 6 shows the measured *S*-parameters and *NF*s of the LNAs with/without ESD protection under a 1.5 V supply voltage with an associated current of 18 mA. The LNAs with/without ESD protection achieve power gains of 18.5- and 19.5-dB and noise figures of 4.1- and 3.6-dB at 60 GHz, respectively. The ESD-protected LNA only shows 1-dB power gain and 0.5-dB noise figure degradation, compared with those in the reference LNA. The input and output (not shown) return losses for the LNAs with/without ESD protection are both greater than 10 dB at 60 GHz. Also, the ESD-protected LNA achieves a large 3-dB bandwidth from 55.5 to 63.2 GHz.

TABLE II
ESD PERFORMANCE COMPARISON OF DIFFERENT TESTING MODES

Testing Mode	PS		PD		NS		ND	
	It_2 (A)	HBM (kV)	It_2 (A)	HBM (kV)	It_2 (A)	HBM (kV)	It_2 (A)	HBM (kV)
ESD Level	1.68	~ 2.5	1.68	~ 2.5	1.68	~ 2.5	1.68	~ 2.5

* HBM levels are estimated based on the TLP measurements.

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TABLE III
PERFORMANCE COMPARISON OF THE PROPOSED LNAS WITH PRIOR WORKS

Ref.	This Work		[1]	[7]	[8]	[9]
Tech. (nm)	65		65	65	130	65
Freq. (GHz)	60		60	77	60	60
	With ESD	Without ESD				
NF (dB)	4.1	3.6	5.3	7.8	8.8	6.1
Power (mW)	27	27	18	37	54	35
S_{21} (dB)	18.5	19.5	17.5	10.5	12	22.3
S_{11} (dB)	< -10	< -10	-15	< -10	< -15	< -15
HBM (kV)	2.5	0.2	8	4.05	--	--
TLP (A)	1.68	--	--	--	--	--
Area (mm^2)	0.47	0.37	0.51	0.404	--	0.21
FOM^1	11.9	16.2	10.1	1.4	0.7	7.3
FOM^2	95.2	3.2	80.9	5.6	--	--

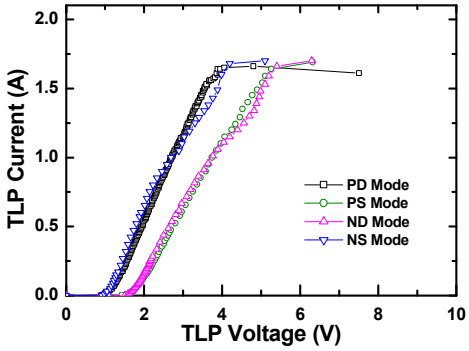

Fig. 7. Measured TLP *I-V* curves of the ESD-protected LNA.

B. *ESD Testing Results*

The ESD testing was performed on-wafer using a Barth 4002 TLP test system and an ESD tester HANWA HED-W5100D, respectively. Fig. 7 shows the test results of the four ESD testing modes. The measured TLP currents of all the four testing modes present a second breakdown current It_2 of 1.68 A, corresponding to a 2.5-kV HBM ESD level. Note that the PS (ND) mode shows a similar on-resistance to the PD (NS) mode, but with an offset voltage of ~ 1.3 V due to the power clamp with an additional voltage drop. Table II summarizes the ESD testing results of different testing modes. The ESD-protected LNA was also tested by the ESD tester together with the RF performance measurements before and after ESD zapping. The measured results show almost identical RF performance before and after 2.5-kV ESD zaps.

Table III compares this work with previously published 60-GHz LNAs. The proposed LNA achieves a lowest *NF* of 4.1 dB under low power consumption. Also, the proposed LNA demonstrates an ESD protection level of 2.5 kV, which is 0.5 kV higher than the standard of typical commercial products. The FOM^1 and FOM^2 (modified from [10]) shown in the table are as follows:

$$FOM^1 = \frac{Gain[abs] \times f_C[GHz]}{(NF-1)[abs] \times P_{DC}[mW]} \quad (1)$$

$$FOM^2 = \frac{Gain[abs] \times f_C[GHz] \times ESD[kV]}{(NF-1)[abs] \times P_{DC}[mW]} \quad (2)$$

V. CONCLUSION

In this paper, different design topologies and concepts of ESD protection for microwave/mm-wave circuits were reviewed, and the design tradeoffs and limitations were discussed. A V-band LNA with the proposed plug-and-play Pi-type ESD block in 65-nm CMOS was also presented. The well-designed ESD block functioned like an ideal 50-Ω transmission line in a wide frequency range. Under a power consumption of 27 mW, the ESD-protected LNA achieved an 18.5-dB power gain and a 4.1-dB noise figure with a 3-dB bandwidth up to 7.7 GHz. An HBM ESD level up to 2.5 kV was also demonstrated.

REFERENCES

[1] M. -H. Tsai, S. Hsu, and *et al*., "Design of 60-GHz low-noise amplifier with low NF and robust ESD protection in 65-nm CMOS," *IEEE Trans. Microwave Theory and Tech.*, vol. 61, no. 1, pp. 553-561, Jan. 2013.

[2] M. -H. Tsai, S. Hsu, and *et al*., "A 17.5-26 GHz low-noise amplifier with 8-kV ESD protection in 65-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 9, pp. 483-485, Sep. 2012.

[3] B. Razavi, "A 60GHz direct-conversion CMOS receiver," *ISSCC Dig. Tech. Papers*, 2005,pp. 400-606.

[4] M. -H. Tsai and S. Hsu, "A 24 GHz low noise amplifier using RF junction varactors for noise optimization and CDM ESD protection in 90-nm CMOS,"*IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 374-376, Jul. 2011.

[5] M. -H. Tsai, S. Hsu, and *et al*., "ESD-protected K-band low-noise amplifiers using RF junction varactors in 65-nm CMOS,"*IEEE Trans. Microwave Theory and Tech.*, vol. 59, no. 12, pp. 3455-3462, Dec. 2011.

[6] M. -H. Tsai, S. Hsu, and *et al*., "A wideband low noise amplifier with 4 kV HBM ESD protection in 65 nm RF CMOS," *IEEE Microw. Wireless Compon. Lett.,* vol. 19, no. 11, pp. 734-736, Nov. 2009.

[7] R. Berenguer, G. Liu, and Y. Xu, "A low power 77 GHz low noise amplifier with an area efficient RF-ESD protection in 65 nm CMOS," *IEEE Microw. Wireless Compon. Lett*., vol. 20, no. 12, pp. 678-680, Dec. 2010.

[8] C. Weyers, P. Mayr, and *et al*., "A 22.3dB voltage gain 6.1dB NF 60GHz LNA in 65nm CMOS with differential output," *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 192-606.

[9] A. Natarajan, S. Nicolson, and *et al*., "A 60GHz variable-gain LNA in 65nm CMOS," in Proc. *IEEE Asian Solid-State Circuit Conference*, Nov. 2008, pp. 117-120.

[10] D. Linten, S. Thijs, and *et al*., "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90 nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1434-1442, July 2005.

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