Dynamic On-Resistance Degradation in E-mode GaN HEMTs Under Over-Voltage Hard Switching Stress: Insight of Physical Space and Energy Levels

Haoran Wang [*], Po-Yen Huang [+], Wei-Ting Hsu [*], Shawn S. H. Hsu [*+], Roy K.-Y. Wong [*+]
[*] Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan, R.O.C.
[+] College of Semiconductor Research, National Tsing Hua University, Hsinchu, Taiwan, R.O.C.
Email: h.r.wang@gapp.nthu.edu.tw ; kywong@ee.nthu.edu.tw

***Abstract*— This study investigates the degradation of dynamic on-resistance (R_{on}) in P-GaN gate enhancement-mode high-electron-mobility transistors (HEMTs) under hard-switching (HSW) stress. Devices were stressed under over-voltage conditions to accelerate degradation. After HSW stress, the dynamic R_{on} increased significantly under a drain-to-source bias (V_{ds}) ranging from 0 V to 500 V, indicating stress-induced defect formation and charge trapping. To analyze the physical distribution of charge trapping, output capacitance (C_{oss})-V_{DS} measurements, combined with TCAD simulations, provide evidence of impact ionization followed by electron and hole accumulation in different field plate (FP) regions. To examine the energy levels of stress-induced traps, current deep-level transient spectroscopy (I-DLTS) revealed a reduction in trap activation energy (E_a) of post-HTOL stressed sample, indicating that hot-carrier modified the defects energy and migrate them closer to the conduction and valence bands. These findings provide critical insight into the physical locations and energy levels of degradation trapping sites after HSW stress, aiding device optimization and long-term switching reliability assessment.**

Keywords—*GaN HEMTs, Power switch, Dynamic R_{on}*

I. INTRODUCTION

Over the past two decades, advancements in design, epitaxial growth, processing, packaging, reliability, and gate driving have facilitated the successful commercialization of gallium nitride (GaN) power high-electron-mobility transistors (HEMTs) [1, 2]. These devices are increasingly being adopted in consumer products, offering high power density and excellent conversion efficiency for power converter applications. However, industrial and automotive applications demand even more stringent requirements in terms of quality and device lifetime [3].

In long-term switching stress reliability, GaN HEMTs can exhibit both static and dynamic on-resistance (R_{on}) degradation due to trap generation and filling, resulting in increased power losses and reduced device lifetime. Compared to soft switching, the switching locus in hard switching (HSW) involves high current and high voltage transitions, which can trigger hot carrier effects, causing trap generation, dynamic R_{on} degradation, and reduced device lifetime. Despite these HSW reliability challenges, most power converters utilize HSW due to its simple circuit topology and cost-effectiveness. To ensure the switching reliability of GaN HEMTs, the JEDEC JC-70.1 committee, which is dedicated to GaN power HEMTs, has established guidelines for evaluating stability (dynamic R_{on}) and reliability (switching acceleration lifetime) [4]. Based on these guidelines, several advanced accelerated switching stress methods for studying dynamic R_{on} degradation in GaN HEMTs have been proposed and implemented, aiming to develop an accelerated degradation model and lifetime prediction, which is crucial [5-8]. However, further insights into the physical locations and energy levels of degradation trapping sites after HSW stress are needed for further optimization.

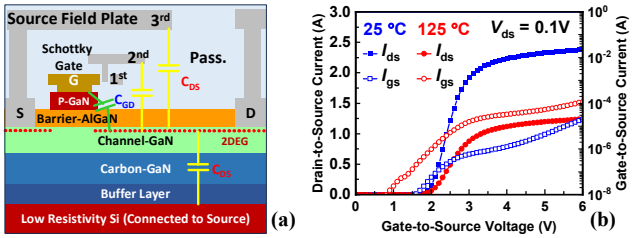

Fig. 1. P-GaN Schottky gate HEMT (a) schematic and (b) transfer and gate leakage characteristics under varying ambient temperatures.

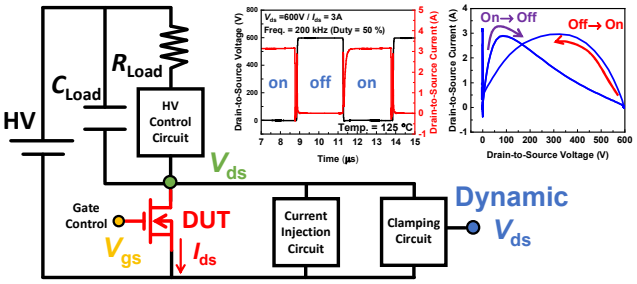

Fig. 2. Schematics of the circuit topology for dynamic HTOL and switching waveform of V_{ds} and I_{ds}. (Insert) Transient waveform and switching locus for HSW stress. During the turn-on transition under HSW, for each V_{ds} stress, I_{ds} reaches its peak at around half of maximum of V_{ds}.

This paper investigates the dynamic R_{on} degradation mechanism in p-type GaN (P-GaN) gate enhancement mode (E-mode) HEMTs. The devices were subjected to voltage-accelerated HSW stress conditions to accelerate the effects of HSW stress on their parameters. To assess the mechanism of dynamic R_{on} stability, DC and CV measurements were conducted. We provide evidence of hot-carrier effects during the high-temperature operating life (HTOL) acceleration test and propose a possible mechanism that identifies the physical location of impact ionization (I.I.) for hot carrier generation. Additionally, we employed current deep-level transient spectroscopy (I-DLTS) to investigate the energy level of traps generated after the over-voltage HSW stress. Furthermore, the trap analysis methodology incorporates deep neural network (DNN) analysis, significantly reducing computation time without compromising the accuracy of activation energy (E_a) extraction. These findings are essential for optimizing device design and evaluating the impact of switching behavior on trap formation and long-term reliability.

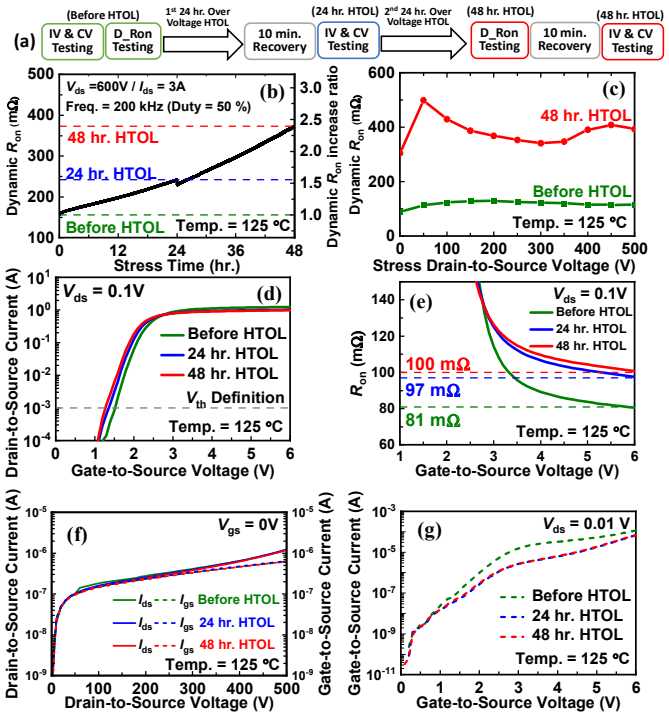

Fig. 3. (a) Over-voltage HTOL stress and test sequences. (b) Dynamic R_{on} as a function of stress time, (c) dynamic R_{on} as a function of V_{ds}, (d) DC transfer curve, (e) R_{on} as a function of V_{gs}, (f) off-state leakage current as a function of V_{ds}, and (g) on-state gate leakage current at an ambient temperature of 125 °C, measured before and after 24 hours and 48 hours of HTOL stress.

II. Static and Dynamic Performance of P-GaN HEMT After Over-Voltage Hard Switching Stress

To investigate the dynamic R_{on} degradation mechanism, a commercial 650 V rating P-GaN Schottky gate E-mode HEMT with source field plates was evaluated [9]. Fig. 1 illustrates the schematic and transfer characteristic of this device. The device was subjected to a high-temperature voltage-accelerated hard switching stress condition, which was performed using the circuit topology proposed in [6] to stress the device and analyze trapping-induced instability. A schematic of the circuit is shown in Fig. 2, which simulates the switching operation without an inductive load. The hot carrier injection during switching transient is supplied by precisely controlling the timing of charging the load capacitor (C_{load}) to generate the HSW waveform and switching locus as illustrated in Fig. 2. This design minimizes the total power consumption, enabling efficient long-term high temperature operating lifetime (HTOL) testing. The sample has conducted at the over-voltage stress V_{ds} of 600 V and drain-to-source current (I_{ds}) of 3 A by a 200 kHz switching pulse with 50 % duty cycle for 48 hours at an ambient temperature of 125 °C, exceeding the typical application voltage of $V_{ds} \leq 520$ V (80 % of the rating), to accelerate the effects of hard-switching stress on their parameters. The dynamic R_{on} is monitored at center of on-pulse (1.25 µs for 200 kHz, 50 % duty operation).

Fig. 3 (a) illustrates HTOL and test sequences. The degradation of dynamic R_{on} under the overall stress time during the accelerated hard-switching stress as shown in Fig. 3 (b). The dynamic R_{on} continues to degrade with increasing stress time, with a slight recovery during the break time between the first and the second 24 hours of stress. The dynamic R_{on} shows a ~2.4 times increasing of the sample increases continuously over the whole time, as shown in

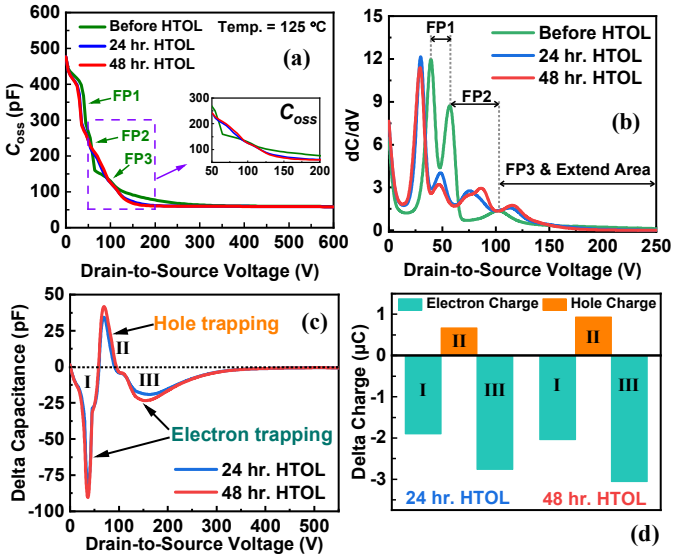

Fig. 4. (a) C_{oss} as a function of V_{ds}, (b) derivation of C_{oss} with V_{ds}, (c) delta capacitance, and (d) delta charge, measured before and after 24 and 48 hours of over-voltage HTOL stress at an ambient temperature of 125 °C.

Fig. 3 (c). After 48 hours of stress, the HSW dynamic R_{on} has significantly degraded by 2.8 to 4.4 times under V_{ds} bias from 0 V to 500 V, which is much higher than the degradation of static R_{on} (~1.25 times). To evaluate the mechanism of HTOL stressed dynamic R_{on}, dynamic and static IV and CV measurements were performed. As depicted in Fig. 3 (d)-(e), the DC transfer current shows a small negative V_{th} shift of about 0.2 V (defined as I_{ds} = 10 mA) and the static R_{on} degrades by ~1.25 times after 24 hours of stress, and show a slight degeneration in the second 24 hours. Meanwhile, the off-state drain and gate leakage currents remain stable, with no leakage path formation and a slight reduction due to electron trapping, as shown in Fig. 3 (f)-(g). The significant difference in degradation between static and dynamic R_{on} suggests the formation of damage and trapping centers under over-voltage HTOL stress. As, the dynamic and static characteristics require different types of equipment, and the gap time for the static measurement between two steps HTOL stress was about few minutes, allowing partial recovery of the trapped electrons.

III. Mechanism Study of Device Degradation After Over-Voltage Hard Switching Stress

A. Trap Physical Space Analysis by Output Capacitance

To evaluate the HSW stress induced electron and hole trapping at different source field plate (FP) regions, the output capacitance (C_{oss}) characteristic of fresh and post-HTOL were studied to identify the hot-carrier trapping physical location. As shown in Fig. 4 (a), in the fresh sample C_{oss} versus V_{ds} plot, the 1st step, 2nd step, 3rd step and the subsequent 'long-tail' represent the monitoring regions under the FP1, FP2, and FP3 with the extended non-overlap drift region, respectively. Which can be clearly identified by the differential CV curve, as the green line in Fig. 4 (b). After the HTOL stress, the C_{oss} profile shifts and the derivation of C_{oss} with V_{ds} shows the boundary of the 2nd step and 3rd step becomes blurry as depicted in Fig. 4 (b), indicating the large amount of charge have been trapped near the locations of FP2 and FP3, resulting in an unstable charge distribution. Noted that positive shifts in the C_{oss} profile indicate hole trapping, trapped charge (ΔQ_{oss}) induced by HTOL stress can

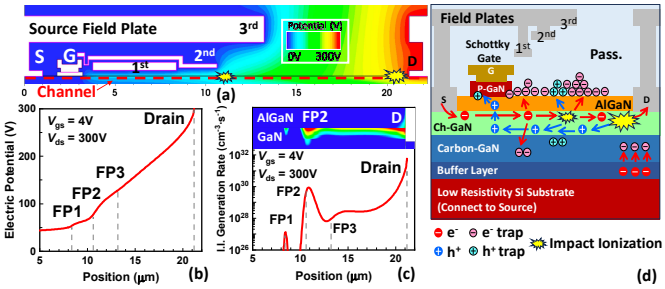

Fig. 5. TCAD simulation under HSW stress (V_{gs} = 4 V, V_{ds} = 300 V). (a) Impact ionization primarily occurs in the channel layer near the drain terminal and at the right edge of FP2. (b) Electric potential and (c) impact ionization generation rate in the 2DEG channel. (d) Proposed mechanism for HSW stress inducing dynamic R_{on} degradation.

be estimated by $\Delta C_{oss} \cdot \Delta V_{ds}$ as illustrated in Fig. 4 (c)-(d). Negative shifts in C_{oss} profile after HTOL stresses are observed at the FP1, part of the FP2 and FP3, and the extended area beyond, marked as region I and III, indicating electron trapping in the relative regions. Conversely, positive shifts occur in region II exhibiting positive shifts in the C_{oss} profile, demonstrating that hole trapping happens at the boundary of FP2 and FP3.

As shown in the TCAD simulation results for the device operating under HSW conditions, the simulated electric potential profile reveals a steep slope (high electric field) at the drain corner and the right edge of FP2 (Fig. 5(a)-(b)), leading to high impact ionization generation beneath these regions (Fig. 5(c)). Fig. 5(d) illustrates the proposed mechanism for the shifting of the C_{oss} profile and R_{on} degradation. The impact-ionized electrons and holes are further accelerated, becoming hot carriers as they transport toward the drain and source, respectively. Some of the hot carriers spill over the barrier layer and become trapped by surface states at the passivation/III-nitride interface and within the bulk, as well as generate new trap sites [10-11]. In the schematic, the high impact ionization rate and strong electric field at regions II and III induce hot hole and electron trapping. The accumulation of massive electron traps significantly depletes the 2DEG, increasing resistance and degrading device performance.

Nevertheless, although C_{oss} data shows a strong correlation to the static R_{on} degradation, significant dynamic R_{on} degradation after stress is not clearly evident in the C_{oss} profile, as the newly generated traps induced by HSW stress may have different capture and response times and thus cannot be fully reflected in the CV test. In additional, the gap time for the static measurement between two steps HTOL stress allows partial recovery of the trapped electrons, the physical location of trapping extracted from C_{oss} still can be reasonably correlated to the dynamic R_{on}.

B. Trap Energy Level Analysis by Current Transient

The generation of hot carriers after HSW stress has been shown to cause damage and create trapping centers, leading to charge trapping phenomena. To investigate the energetic characteristics of these traps, a current deep-level transient spectroscopy (I-DLTS) methodology was utilized to explore how the charge trapping within the passivation layer, barrier layer and buffer epi-stacks. A fresh sample and a post-HTOL sample were subjected to I-DLTS analysis. Initially, a high V_{ds} stress process was applied under the high V_{ds} semi-on condition (V_{ds}= 400 V, V_{gs}= 0.5V), with the power limited by equipment's compliance. This process aims to accelerate

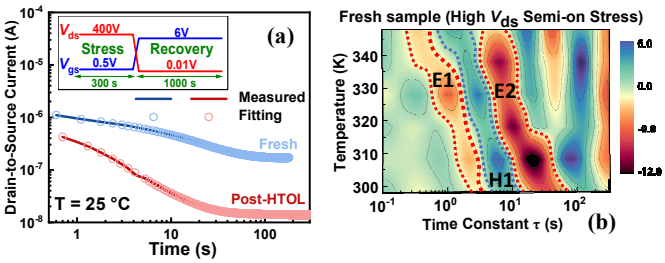

Fig. 6. (a) Measurement and DNN fitting current transient curves at 25 °C, and (insert) stress and recovery biasing conditions. (b) Amplitude contour mapping of τ and the relavent amplitude under various temperatures.

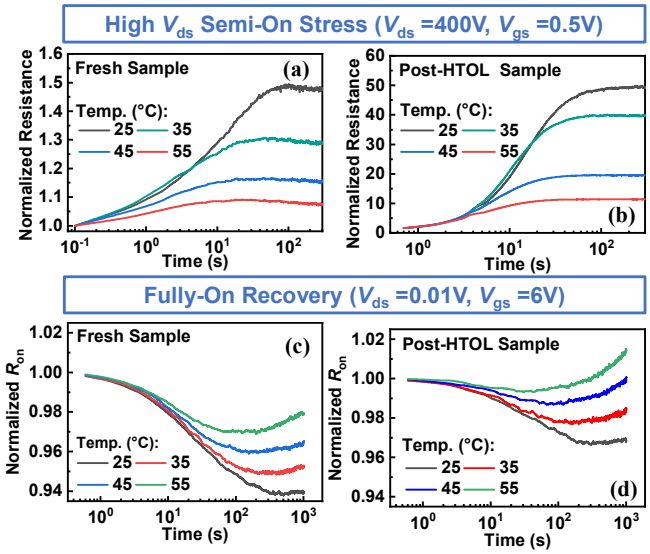

Fig. 7. Normalized resistance and R_{on} transient curves of fresh sample and post-HTOL sample during (a)(b) high V_{ds} semi-on stress process and (c)(d) fully-on recovery process.

electrons and holes and to fill up the traps without causing additional damage. As shown in Fig. 6 (a), the I_{ds} of post-HTOL sample exhibits greater degradation, even though the accelerated current is lower. The measured and DNN-fitted transient curves exhibit high accuracy. By employing an initial value of 1000 time constants (τ) and the corresponding amplitude during contract regression, the process automatically discerns the optimal fitting quantity along with its respective value, as shown in Fig. 6 (b), where the red and blue areas represent negative and positive amplitudes, implying τ for electron and hole traps, respectively [12].

Fig. 7 shows the normalized resistance and R_{on} transient curves during the high V_{ds} stress and recovery processes for both samples. During the high V_{ds} stress, both samples show increasing resistance. The post-HTOL sample exhibited a higher increase ratio, suggesting the occurrence of a substantial amount of electron trapping (Fig. 7 (b)). On the other hand, in the fresh sample, hole trapping (indicated by a 2DEG increase and a decrease in R_{on}) was observed after the saturation of electron trapping (when peak R_{on} is reached), due to relatively smaller number of electron traps in the fresh sample, as shown in Fig. 7(a). Based on the results of part II, two possible hole trapping mechanisms are proposed: (1) hole trapping at the boundary of FP2 / FP3, and (2) electron band-to-band tunneling from the carbon-doped GaN (C-GaN) valence band to 2DEG through dislocations. This causes hole accumulation and trapping at the C-GaN and Superlattice (SL) interface, increasing the 2DEG density (resulting in a decrease in R_{on}) [13-14]. The recovery was carried out under a fully-on condition with a minimal cond-

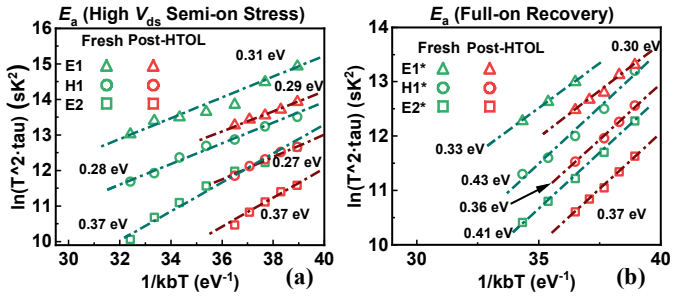

Fig. 8. E_a of the fresh sample and post-HTOL sample during (a) high V_{ds} semi-on stress process, and (b) fully-on recovery process.

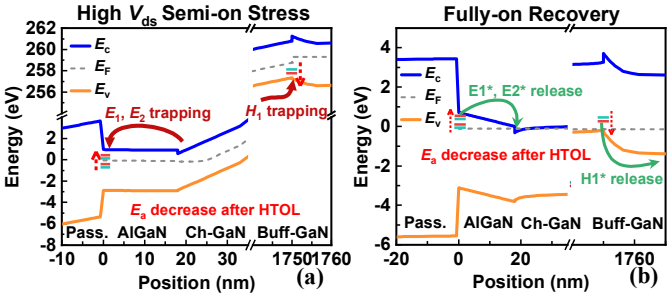

Fig. 9. Proposed band diagrams near the drain terminal during high impact ionization at (a) high V_{ds} semi-on stress, and (b) fully-on recovery process.

uction current to avoid the self-heating affecting R_{on} (V_{ds}=0.01 V, V_{gs}=6 V). During recovery, as seen in Fig. 7 (c)-(d), the R_{on} of both samples decreases initially and then rises, indicating that relatively fast electron de-trapping leads to a gradual decrease in R_{on}, while the slow de-trapping of holes causes an increase in R_{on}. During the hole de-trapping period, the post-HTOL sample exhibits rapid and extensive hole de-trapping, which compensates for electron de-trapping and results in greater R_{on} degradation at the same recovery time. Fig. 8 shows the Arrhenius plot of time constant spectrum extracted from both fresh and post-HTOL samples. These trap states, identified as E_1 (E_1^*), H_1(H_1^*), and E_2 (E_2^*), correspond to different electron and hole trap centers, respectively. Both samples exhibit similar E_a during stress and recovery. However, all τ values in the post-HTOL sample are shorter than those in the fresh sample, suggesting a reduction in E_a. This indicates that, from an energy perspective, the trap levels shift closer to the conduction or valence bands after the hot-carrier impact during HSW stress. The proposed mechanism involves hot carriers breaking weak bonds near defects, at passivation/AlGaN interfaces and bulk, within the epitaxial layers, thereby altering their energy levels [15-16]. Furthermore, despite the comparable E_a values for electrons and holes, the stress and recovery times of holes were longer due to their higher effective mass and lower mobility.

The proposed band diagram of device near the drain terminal (in high impact ionization generation rate region) under HSW stress shows significant electron trapping caused by the large transfer of hot electrons from the channel, which are trapped at the passivation/AlGaN interface. Moreover, holes trapped at the C-GaN and SL interface or at the boundary of FP2 / FP3 (not shown in this diagram) as shown in Fig. 9 (a). During recovery, trapped electrons are released to the 2DEG channel, while trapped holes either de-trap into the GaN buffer or recombine with electrons from the unintentional doped n-type GaN epitaxial layers (not shown in this diagram) as shown in Fig. 9 (b).

IV. Conclusion

The degradation of dynamic R_{on} in p-GaN gate HEMTs under over-voltage HSW stress is attributed to stress-induced defect formation and charge trapping. The physical distribution of charge trapping and the energy levels of stress-induced traps were analyzed through C_{oss}-V_{ds} and I-DLTS, providing critical insights into damage generation, trapping mechanisms, and trap E_a modification under HSW stress. Based on these findings, several optimization strategies are proposed to mitigate damage, including suppressing impact ionization through RESURF engineering, enhancing the robustness of the passivation and AlGaN barrier interfaces and bulk, and increasing the AlGaN barrier thickness to extend the mean free path of hot carriers.

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