SESSION -A13

OPTICAL COMMUNICATION & SYSTEM

CMOS Broadband Amplifiers for Optical Communications

Shawn S. H. Hsu* and Jun-De Jin

High Speed Devices and Integrated Circuits Group, Department of Electrical Engineering
National Tsing Hua University, Hsinchu, Taiwan
Tel: 886-3-5731278; Fax: 886-3-5752120; E-mail: shhsu@ee.nthu.edu.tw

Abstract-**This paper presents CMOS broadband amplifier design techniques for front-end blocks in optical communication systems. Using the proposed π-type inductor peaking (PIP) technique, the Gain-Bandwidth Product (GBP) of the circuit can be significantly enhanced. Three broadband amplifiers for OC-192 and OC-768 including two transimpedance amplifiers (TIA) and one laser driver (LD) are demonstrated by the PIP technique using standard 0.18-μm CMOS technology.**

Index Terms- **Transimpedance amplifier (TIA), laser driver (LD), CMOS, optical, microwave.**

I. INTRODUCTION

The broadband amplifier is one of the key circuit blocks for optical communication systems. The increased demand for large data capacity pushes the operation speed of the amplifiers from 10 Gb/s (OC-192) up to 40 Gb/s (OC-768). Previously reported results were mostly realized using compound semiconductor (III–V or SiGe) technologies to take advantage of the superior transistor characteristics [1-3]. Recently, CMOS technology with continuously scaled feature sizes attracts much attention of circuit designers for broadband amplifier applications owing to the significantly improved frequency response characteristics [4-6]. With the advantages of low cost, low power consumption, and high integration level, CMOS technology is an excellent candidate for broadband amplifier applications up to tens of GHz operation speed.

Different design techniques were reported for achieving a wide bandwidth such as distributed amplifiers (DA), feedback amplifiers, and tuned amplifiers with inductive peaking. The DA configuration usually consumes a large DC power P_{DC} and chip area, and the feedback topology has a tradeoff between the gain and bandwidth. The inductor peaking design is an effective approach to enhance the gain-bandwidth product (GBP). The fundamental idea is that the inductor introduces a zero to cancel the original RC pole to extend the circuit bandwidth. In this paper, the proposed π-type inductor peaking (PIP) techniques are discussed, which introduces two zeros and two pairs of complex conjugate poles to enhance the gain-bandwidth product. The most important blocks in optical communication front-ends including the transimpedance amplifier (TIA) for the receiver and the laser driver (LD) for the transmitter are studied. Based on this design technique, we realize a 40 Gb/s TIA [7] and a 10 Gb/s TIA [8] both with 0.18-μm CMOS technology. In addition, a 10 Gb/s LD is also demonstrated using 0.18-μm CMOS technology.

II. CMOS BROADBAND AMPLIFIERS

Figure 1 shows a small-signal model of MOSFET for the transimpedance gain consideration, where C_{pd} is the parasitic capacitance of the photo diode and i_{pd} represents the input photo current; C_L is the load capacitance. Based on this simplified model, the bandwidth of block I is $1/[R_g(C_{pd}+C_{gs})]$, and that for block II is $1/[R_d(C_d+C_L)]$. The corresponding GBP is $1/(C_{pd}+C_{gs})$ and $1/(C_d+C_L)$ respectively. It is clear that the capacitive components play a critical role regarding the performance limitation. With the proposed PIP technique, these parasitic capacitances can be effectively resonated out to significantly improve the GBP.

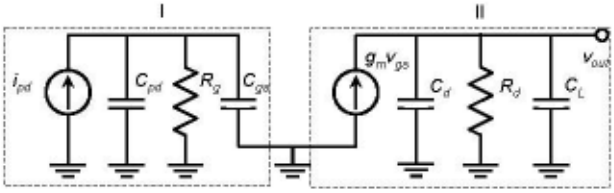

Fig. 1. CMOS small-signal model with a current source input.

A. Pi-type Inductor Peaking

The proposed π-type inductor peaking (PIP) techniques includes three peaking inductors (L_{S1}, L_{d1}, and L_{d2}) as shown in Fig. 2. Assuming a cascaded common-source (CS) topology, the C_g represents the gate capacitance of the next stage. The transimpedance transfer function $-v_{out}/g_m v_{gs}$ can be derived as [7]:

$$Z_{PIP}(s) = R_{d1}R_{d2}\frac{1+s\left(\frac{L_{d1}}{R_{d1}}+\frac{L_{d2}}{R_{d2}}\right)+s^2\frac{L_{d1}}{R_{d1}}\frac{L_{d2}}{R_{d2}}}{D_0+sD_1+s^2D_2+s^3D_3+s^4D_4+s^5D_5} \quad (1)$$

where

$$D_0 = R_{d1}+R_{d2}$$
$$D_1 = L_{d1}+L_{d2}+L_{s1}+R_{d1}R_{d2}(C_d+C_g)$$
$$D_2 = (C_d+C_g)(R_{d1}L_{d2}+R_{d2}L_{d1})+R_{d1}L_{s1}C_d+R_{d2}L_{s1}C_g$$
$$D_3 = L_{d1}C_d(L_{d2}+L_{s1})+L_{d2}C_g(L_{d1}+L_{s1})+R_{d1}R_{d2}L_{s1}C_dC_g$$
$$D_4 = L_{s1}C_dC_g(R_{d1}L_{d2}+R_{d2}L_{d1})$$
$$D_5 = L_{d1}L_{d2}L_{s1}C_dC_g$$

It can be seen that the numerator includes two zeros (R_{d1}/L_{d1}) and (R_{d2}/L_{d2}) and the denominator contains two pairs of complex conjugate poles. By solving the transfer function with properly designed damping factors (< 0.707), these zeros and poles can enhance the bandwidth effectively. Under the constrain of a gain flatness within 2.2 dB, the bandwidth enhancement ratio (BWER) of PIP design can be up to 3.31. The gradually improved bandwidth can be observed by adding the three inductors step by step as illustrated in Fig. 3.

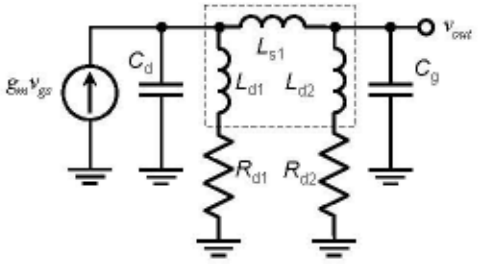

Fig. 2. The equivalent circuit model of one gain stage with the π-type inductor peaking (PIP) technique.

B. Cascade configuration

Increasing the stage number for amplifier design is an effective approach for achieving high GBP.

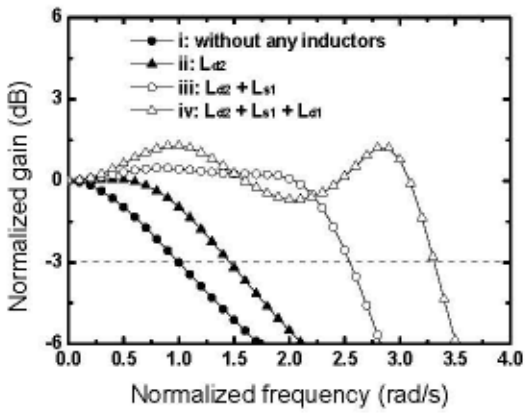

Fig. 3. Simulation results of the gradually improved bandwidth by adding the three PIP inductors step by step.

For the earlier mentioned DA design, owning to the artificial transmission line topology, the gain of each stage sums up for the overall gain. A large GBP can also be obtained, whereas the GBP/P_{DC} could be relatively small. The cascade design approach as shown in Fig. 4 is more effective. The transfer function H_{tot} of a cascade amplifier with n stages can be expressed as follows, where the gain of each stage is A_p, and the bandwidth of each stage is ω_p:

$$H_{tot}(s) = \frac{A_p^n}{\left(1+\frac{s}{\omega_p}\right)^n} \quad (2)$$

The overall gain of the cascade configuration is the multiplication of each stage, and thus its efficiency is better than DA design. Based on (2), the optimum stage number n_{opt} for bandwidth can be derived by differentiating with respect to n. The obtained n_{opt} is $2\times \ln A_{tot}$ (A_{tot} is the desired overall gain). It is worth mentioning that the total power consumption is also critical when determining n_{opt} in practical design. In this paper, the two transimpedance amplifiers are both based on the scheme as shown in Fig. 4, the cascaded common-source topology, where R_M is the matching resistor, and R_D is the load at the drain node, and L_P is the PIP inductors. The design of the laser driver is also based on the cascaded

topology with the PIP technique. However, since the LD needs a large output swing and high driving current, more details need to be considered in the design. The following section discuss about the design of the LD.

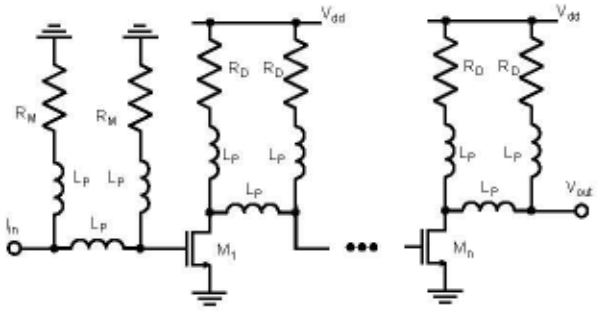

Fig. 4. The cascade configuration with PIP technique for high GBP broadband amplifiers.

C. Design of Laser Driver

Figure 5 shows the circuit schematic of the proposed 10 Gb/s laser driver using the PIP design technique. Differing from the TIA, a large driving current capability is necessary and thus the design features a tree-type parallel configuration. The PIP design is used at both input and output stages for inductive peaking and also impedance matching. The block *Amp I* consists of a common-source stage with the PIP inductor connected at the drain node, which is similar with one stage of the cascade design in Fig. 4.

The cascode configuration consists of a common-source stage followed by a common-gate stage is employed for *Amp II*. The cascode design can distribute the voltage across each transistor to prevent the transistor breakdown under the high output voltage swing. In addition, the Miller effect is alleviated and the input/output isolation is enhanced. Note that a separate V_{DD} for the output stage is used for generating a large output swing up to 3.0 V. The resistors and transistors in the amplifier are also designed with many units connected in parallel to sustain the high current level.

III. MEASURED RESULTS

Using the PIP technique, three broadband amplifiers for the front-end of optical communication system are realized in standard CMOS 0.18-μm technology. With a four stage design (see Fig. 4, n= 4), a 40 Gb/s (OC-768) TIA is achieved. The transimpedance gain is 51 dBΩ, the 3-dB bandwidth is 30.5 GHz, and the power consumption is 60.1 mW under a 1.8 V supply voltage. This amplifier has a gain–bandwidth product per DC power figure of merit (GBP/P_{DC}) of 180.1 GHzΩ/mW [7].

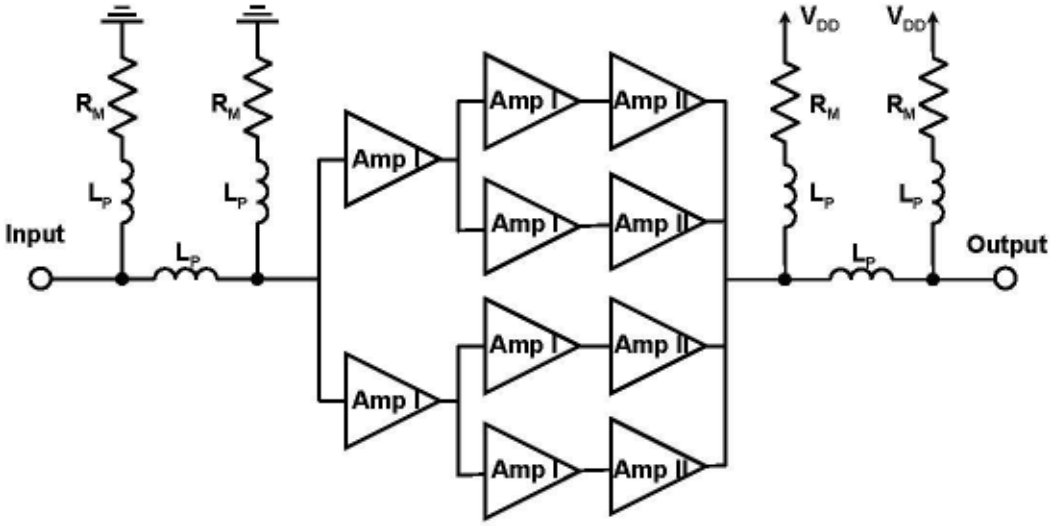

Fig. 5. Circuit configuration of the 10 Gb/s laser driver with PIP technique in 0.18-μm CMOS technology.

With the similar design concept, a TIA for 10 Gb/s applications (OC-192) is also realized by n= 6. A transimpedance gain up to 75 dBΩ is achieved with a 3-dB bandwidth of 7.2 GHz. The figure of merit GBP/P_{DC} is up to 441.1 GHzΩ/mW in this design. The TIA with PIP shows an overall improvement of 7.4× in bandwidth compared to that without any bandwidth enhancement technique in this design [8].

We also employ the PIP design technique for a 10 Gb/s laser driver design. Figure 6 is the chip micrograph. The chip area is 1.3×0.97 mm^2. Under a supply voltage of 1.8 V, the DC power consumption is 800 mW. The measured eye diagram at 10 Gb/s is shown in Fig. 7. The output voltage is measured under a 20 dB attenuation, and thus the actual output swing is 3 V_{p-p} with a corresponding current of 60 mA, which agrees well with the designed value.

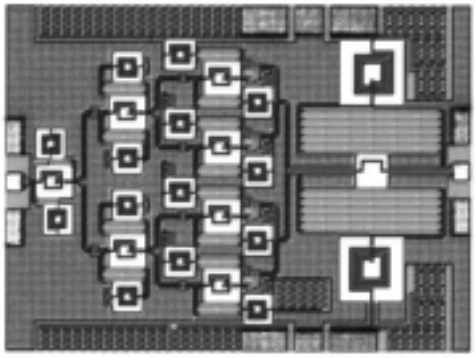

Fig. 6. Chip micrograph of the laser driver with the PIP technique (chip area: 1.3×0.97 mm^2).

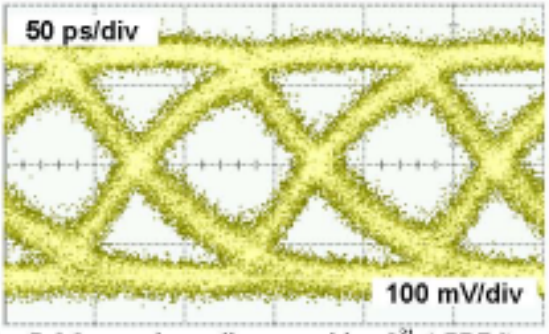

Fig. 7. Measured eye diagram with a 2^{31}-1 PRBS at 10 Gb/s under a 20 dB attenuation. The actual output voltage swing is 3 V_{p-p}.

IV. CONCLUSION

In this paper, we reported the design of CMOS broadband amplifiers for the front-end blocks in optical communication systems. Three amplifiers were demonstrated using the proposed π-type inductor peaking (PIP) technique. Using standard 0.18-μm CMOS technology, the 40 Gb/s and 10 Gb/s transimpedance amplifiers can achieve GBP/P_{DC} of 180.1 and 441.1 GHzΩ/mW, respectively. The laser driver can operate up to 10 Gb/s under a power consumption of 800 mW. The output swing is up to 3 V peak-to-peak with a current of 60 mA.

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