# A Low Phase-Noise Class-C VCO Using Novel 8-Shaped Transformer

Ping-Yi Wang[1], Te-Lin Wu[1], Ming-Yu Chen[1], Yun-Chun Shen[1], Yin-Cheng Chang[1,2], Da-Chiang Chang[2], and Shawn S. H. Hsu[1], *Member, IEEE*

[1]Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan

[2]National Chip Implementation Center, National Applied Research Laboratories, Hsinchu, Taiwan

***Abstract*— A 9 GHz low phase noise class-C voltage controlled oscillator (VCOs) with an 8-shaped transformer configuration using 0.18-µm CMOS technology is presented. By utilizing the 8-shaped transformer, the proposed class-C VCO can be operated at reduced dc power consumption while maintaining circuit performance in terms of phase noise and limiting EMC (Electro-Magnetic Compatibility) issues when the symmetrical structures are considered. Consuming a dc current of 5.5 mA with the supply voltage of 1.8 V, the class-C VCO exhibits a frequency tuning range of 1.4 GHz, a phase noise of -117.4 dBc/Hz at 1 MHz offset frequency away from the 8.94 GHz carrier, and a figure of merit up to 186.4 dBc/Hz.**

**Keywords— 8-shaped transformer, voltage controlled oscillators (VCOs), class-C VCO.**

## I. INTRODUCTION

Being an essential part in the RF front-ends, the voltage controlled oscillator (VCO) is viewed as one of the most power-hungry and noise sensitive components. Accordingly, phase noise and power consumption are the two important parameters for commercial VCOs products. Furthermore, frequency tuning range requirement is increased due to some emerging advanced communication systems, which are pursuing the realization of wide-band and high data-rate applications. Such requirement can be accomplished by having a VCO with wide tuning range and low phase noise simultaneously. However, these two and the low power constraints are trade-offs to one another, making the design challenging to IC designers nowadays.

The integrated inductor of the LC-tank in a VCO plays a key role for the overall circuit performances, especially affecting phase noise significantly. The conventional spiral inductors often cost large chip area as well as suffer from low Q-factors, resulting in poor phase noise performance. A recent study shows that the 8-shaped inductor achieves a significant increment of the density of integration, self-resonator frequency, and the Q-factors compared to the planar spiral inductor [1]-[2]. The 8-shaped inductor is capable of increasing the isolation from coupling inductors as well as avoiding the magnetics pulling effect in the VCO circuits. The topology of such inductor is as shown in Fig. 1. In this proposed VCO, such novelty was adopted and extended to construct an 8-shaped transformer-based in order to utilize the benefit both from the class-C topology and the transformer structure itself, and hence reduce the EMC issues.

Due to the phase noise constraints, LC-based VCOs are usually chosen over the ring-type oscillator. For a classical LC-tank oscillator, the cross-coupled pairs operate at traditional class-B region and into deep triode region, causing the poor phase noise performance. Recently, Andreani *et al.* has introduced a class-C harmonic exploiting the advantages of using resistors or transformers to bias the gate of transistors which can operate in class-C region, resulting in the transistors operating at the saturation region. Using such circuit skill, the dc bias circuit saves as much as 30 % of power for the same phase noise performance [3]. A similar idea which is from asymmetric-width transformer -based Armstrong VCO was used in [4]. The cross-coupled pairs of transformer based Armstrong VCO operates at class-B region and consumes larger dc current for maintaining the phase noise performance. In this work, we presented a differential VCO with 8-shaped transformer coupling technique optimized for small chip area and good phase noise performance. By using the 0.18 µm CMOS technology, a 9 GHz VCO circuit is implemented and demonstrated.

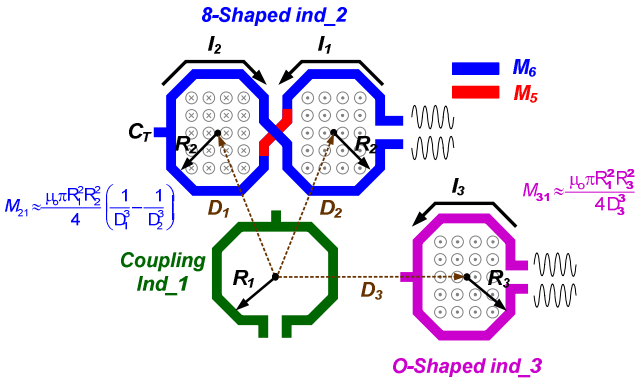


Fig. 1. The concept of the EMC issues for 8-shaped inductor [2].

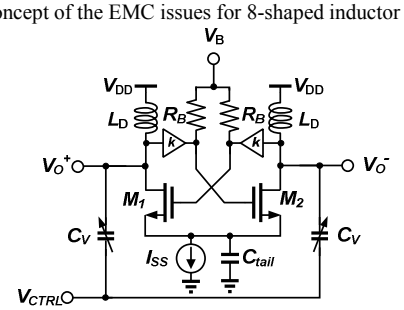


Fig. 2. The model of class-C VCO circuit

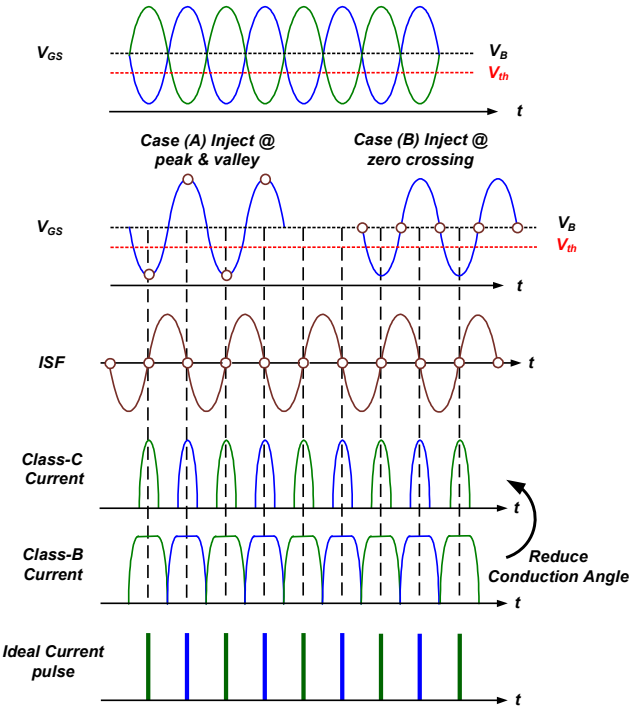


Fig. 3. Operation of class-C VCO.

## II. CIRCUIT DESIGN

### A. Class-C VCO

The Fig.2 shows the circuit model of the class-C VCO. $M_1$ and $M_2$ represent the transconductance stage to guarantee the oscillation stability, $k$ is the voltage feedback paths gain factor, $I_{ss}$, $C_{tail}$, and $R_B$ are the DC bias current, tail current bypass capacitors, and gate bias resistors, respectively.

To improve the phase noise performance, the gate bias voltage should be set as low as possible. However, the lower gate bias voltage causes the startup problems. To turn on the transistor, the oscillator amplitude has to satisfy Eq. (1)

$$V_{DD} - A_t > V_B + kA_t - V_{th}$$
$$A_t < \frac{V_{DD} - V_B + V_{th}}{1+k} \quad (1)$$

where $V_B$ is the gate bias of the transistor, $V_{th}$ is the threshold voltage, $k$ is the feedback factor, and $A_t$ is the amplitude. For example, assuming $k = 0.5$ and $V_B$ closed to the $V_{th}$, the maximum allowed $A_t$ is approximately 2/3 power supply voltage.

The impulse sensitivity function (ISF) shows the sensitivity to the phase noise of the oscillator. The output waveform, ISF, and the current of the transistors were shown in the Fig.3. In the case (a), the noise current injected at the peak or valley of the voltage waveform (zero sensitivity of ISF), and increased the amplitude of the output signal. In order to achieve the stability of the oscillation, the output signal will recover to the original state, having no excess phase; in the case (b), the noise current injected at the zero cross point of output waveform (maximum sensitivity of the ISF), and also increased the amplitude of the output waveform. However, the voltage increased causes a phase shift and it cannot be recovered even if the amplitude is stable.

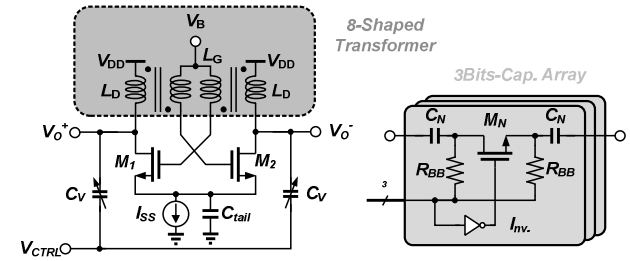


Fig. 4. The proposed class-C VCO circuits

According to the previous discussion, the current of the oscillator should be conducted at the timings when the ISF shows zero sensitivity, and class-C VCO realizes such ideal current conduction [3]. Using the larger tail capacitor $C_{tail}$, the conduction angle is much lower than half period, and causes the current waveforms become sharper and shaper. The other parameter is the independent gate bias ($V_B$), which is set equal or lower to the threshold voltage ($V_{th}$), causing the conduction time become shorter and shorter. Using both techniques of reducing gate-bias voltage ($V_B$) and current source shunt capacitor ($C_{tail}$), the conduction angle results in shorter and impulse-shaped current waveform, improving the phase noise performance.

The proposed class-C VCO with 8-shaped transformer is depicted in the Fig.4. The dimension of each cross-coupled device ($M_1$ and $M_2$) is 50 µm/0.18 µm. The tail biasing current generator is implemented with an NMOS transistor of dimensions of 750 µm/0.5 µm operating in the saturation region, minimizing the 1/$f$ up-conversion to the tank. The MOS varactor is implemented with an Accumulation-Mode MOS (A-MOS) varactor with a gate length of 0.5 µm, finger of 14, respectively. The capacitance of the varactor is 90 to 125 fF throughout the entire tuning curve. In order to cover the process variation, the coarse tuning capacitor bank is needed. The coarse tuning is achieved by 3-bits digital controlled word using binary weighted capacitors array with the capacitances be 50 fF, 100 fF, and 200 fF, respectively. The resistor-biased capacitor cell exhibits a better trade-off between tuning range and phase noise [5]. The simulated overall tank $Q$ ranges from 10.0 to 11.5 across the tuning range, including the open drain buffer needed for the measurement.

### B. 8-shape transformer

According to the conclusion in the previous discussion, the so called 8-shaped transformer applied to the proposed class-C VCO has only one turn in each branch. Fig.5. shows the proposed 8-shaped transformer with the width of coils $W$ of 15 µm. The spacing is designed as 2 µm to achieve a coupling factor $k$ of 0.6 with the horizontal diameter and vertical diameter $D_X$ and $D_Y$ of 240 µm and 200 µm, respectively. The port 1, port 2, port 3, and port 4 connect to the drain and gate of the cross-coupled transistors. The port 5 and port 6 is the dc bias path. The extracted parameters of the 8-shaped transformer are $L_D$, $L_G$, $n$, $k$, $Q_D$, and $Q_G$ of 817 pH, 836 pH, 0.99, 0.62, 11.8 and 11.2, respectively. The

L-shaped pattern grounded shield (PGS) [6] is implemented with metal one layer to isolate the magnetic coupling from the substrate and improve the *Q* factor of transformer. Comparing with the conventional octagonal-shaped with diameter *D* of 240 μm, the self-inductance in each branch is exactly only 60 % of that of 8-shaped under the same Q factor. The simulated results of the 8-shaped transformer are shown in the Fig.6.

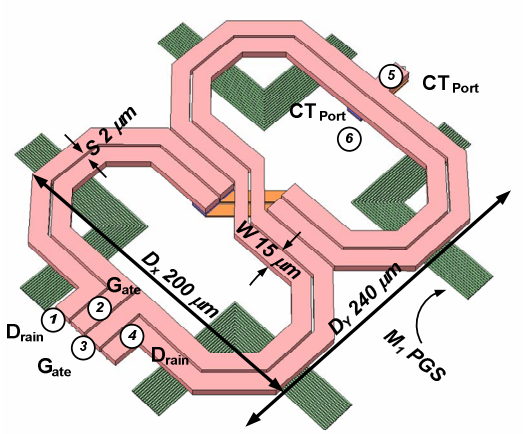


Fig. 5. The proposed 8-shaped transformer.

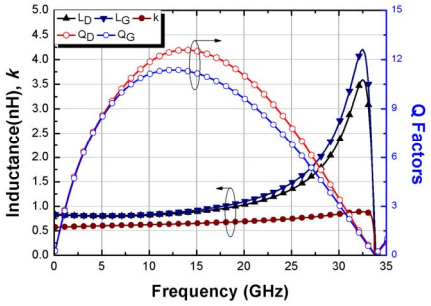


Fig. 6. Simulated results of the 8-shaped transformer.

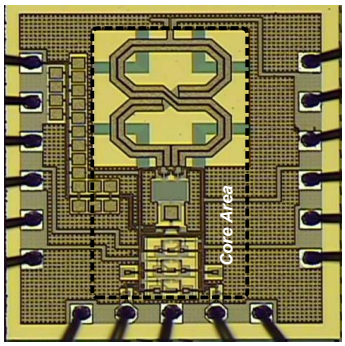


Fig. 7. Chip photograph of the proposed VCO with a chip size of 0.53 mm$^2$, including RF and DC bias pads.

## III. Experiment Results

The chip photograph of the proposed VCO is as shown in Fig. 7 with a chip size of 0.53 mm$^2$, including RF and dc bias pads. The circuit simulation was carried out by the simulation tool ADS. Sonnet was used to simulate the parameters of the transformer. Under a 1.8-V supply voltage, the dc power consumption of the core circuit and buffer are 10 mW and 25 mW, respectively. The output spectrum was measured by using the Agilent E4407B spectrum analyzer, and phase noise was measured by using the Agilent E5052B signal source analyzer. Fig. 8 shows the measured output spectrum with the oscillation frequency of 9.14 GHz and output power of –3.5 dBm, with the cable loss 2.5 dB. Fig. 9 shows the measured frequencies range versus the tuning voltage. The measured frequency range is about 1.5 GHz over the entire tuning range. Fig. 10 shows the measured output power versus the tuning voltage. The output power is higher than -3.5 dBm over the tuning range. The measured phase noise at 8.97 GHz is -117.4 dBc/Hz at 1 MHz offset frequency as shown in Fig. 11. The time-domain output waveform with the mean duty cycle 50 % is shown in the Fig. 12. The measured performance compared with previous works as summarized in Table I. The proposed VCO shows a good FOM with a small chip area.

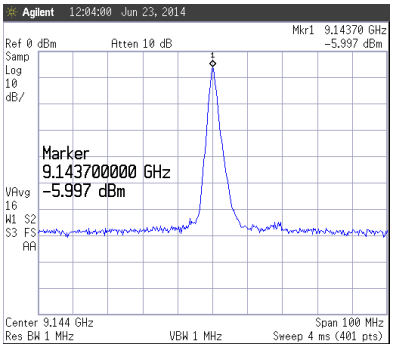


Fig. 8. Measured output spectrum of the VCO.

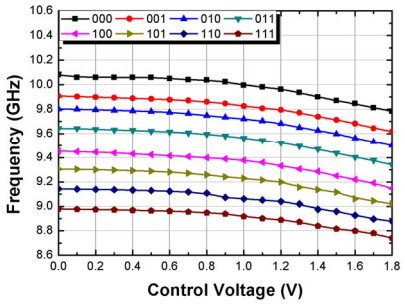


Fig. 9. Measured output frequencies versus tuning voltage.

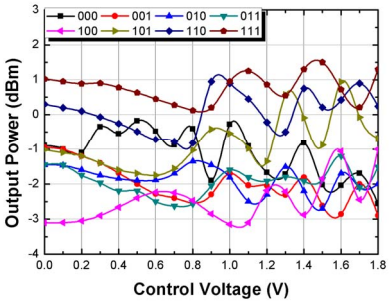


Fig. 10. Measured output power versus tuning voltage.

TABLE I
COMPARISONS OF THE PREVIOUSLY REPORTED VCOS AND THIS WORK

| Ref | CMOS Process | Freq. (GHz) | Phase Noise @ 1MHz (dBc/Hz) | Tuning Range (%) | Range of Control Voltage (V) | Output Power (dBm) | $V_{DD}/I_{DD}$ (V/mA) | FOM (dBc/Hz) | Area ($mm^2$) | Topology |
|---|---|---|---|---|---|---|---|---|---|---|
| [7] | 180nm | 11.05 | -110.42 | 10.5 | 0-0.6 | -9 | 0.6/6.83 | 185.2 | 0.36 | Negative-Gm Back-Gate Tuned |
| [8] | 180nm | 10.29-11.1<br>21.16-22.93 | -115.9<br>-106.8 | 7.57<br>8.03 | 0-1.8 | -9.1<br>-13.5 | 1.8/8.44 | 184.63<br>181.81 | 1.73 | Dual-LC tank |
| [9] | 180nm | 4.78-5.11<br>12.19-12.61 | -117.16<br>-112.15 | 8.22<br>3.27 | 0-1.8 | -8.59<br>-11.48 | 0.8/3.2<br>0.8/2.82 | 187.2<br>190.5 | 0.35 | Dual-LC transformer tank |
| [10] | 180nm | 11.22 | -109.35 | 2.36 | 1.6-2 | -21.07 | 1.8/3.8 | 181.8 | 0.33 | Back-gate TF feedback |
| [11] | 180nm | 9.3-10.4 | -89[a]<br>-119[b] | 11.16 | 0-4 | 4.8 | 1.8/3.22 | N.A | 0.3 | Complementary Cross-Coupled |
| [12] | 180nm | 11.24-11.87 | -110.8 | 5.45 | 0.6-1.4 | -26 | 1.8/4.5 | 183 | 0.45 | Cascode with Q-enhancement |
| **This work** | **180nm** | **8.7-10.1** | **-117.4** | **14.89** | **0-1.8** | **-3.5** | **1.8/5.5** | **186.4** | **0.53** | **8-shaped Transformer** |

[a]measured at 100 kHz offset frequency. [b] estimated by -20dB/decade slope.

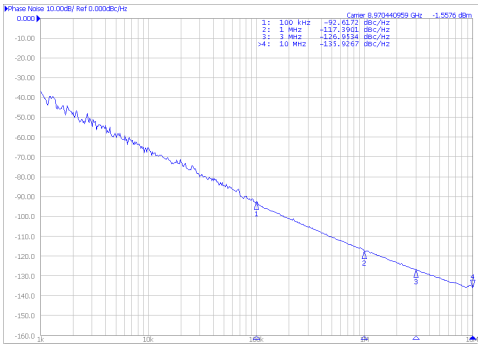

Fig. 11. Measured phase noise at 8.97GHz.

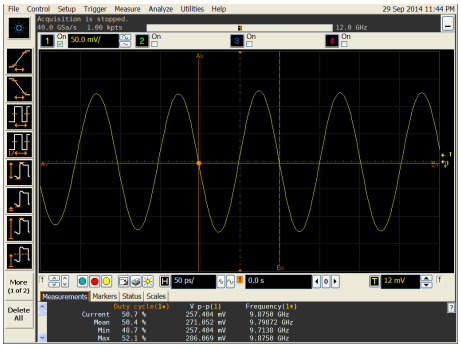

Fig. 12. Time domain waveform.

## IV. CONCLUSION

This work successfully demonstrated a 9 GHz VCO operating at 1.8-V with a phase noise performance of -117.4 dBc/Hz at 1 MHz offset frequency. The proposed VCO combines the advantage of 8-shaped transformer, which could relax the EMC issues, and class-C technique could achieve the low phase noise. The measured results showed that the proposed VCO can achieve a higher FOM maintaining low power consumption and tuning range compared with the reported works. The proposed VCO is suitable for the application in high performance frequency synthesizers.

## ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC), Hsinchu, Taiwan for chip implement and high frequency measurement support by Shawn-Guann Lin and Ya-Wen Ou.

## REFERENCES

[1] Tesson, O, "High quality monolithic 8-shaped inductors for silicon RF IC design," in *IEEE topic meeting on SiRF,* Jan. 2008. pp. 94-97.

[2] Andrew Poon, Andrew Chen, Hirad Samavati, and S. Simon Wang "Reduction of inductive crosstalk using quadrupole inductors," *IEEE J. of Solid-State Circuits*, vol. 44, no. 6, pp. 1756-1764, Jun. 2009.

[3] A. Mazzanti, and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2716-2729, Dec. 2008

[4] E. H. Armstrong, "Some recent developments in the audio receiver," *Proc. IRE*, pp. 215–238, Sep. 1915.

[5] H. Sjoland, "Improved switched tuning of differential CMOS VCOs," *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Process*., vol.49, no. 5, pp. 352–355, May 2002

[6] C. Patrick Yue, and S. Simon Wong, "On-chip spiral inductors with patterned ground shield for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May. 1998.

[7] Y. C. Yang, C. H. Chang, J. M. Lin, and J. H. Weng "A 0.6 V 10 GHz CMOS VCO Using a negative-Gm back-gate tuned technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 3, pp. 163-165, Mar. 2011.

[8] S. L Liu, K. H. Chen, and Albert Chin. "A dual-resonant mode 10/22-GHz VCO with a novel inductive switching approach," *IEEE Trans. Microw. Theory Tech*, vol. 60, no.7, pp. 2165-2177, Jul. 2012.

[9] S. L. Jang, Y. K. Wu, C. C. Liu, and J. F. Huang, "A dual-band CMOS voltage-controlled oscillator implemented with dual-resonance LC tank," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 12, pp. 816–818, Dec. 2009

[10] N. J. Oh, and S. G. Lee, "11-GHz CMOS differential VCO with back-gate transformer feedback," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 733–735, Dec. 2005

[11] L. Jia, J. G. Ma, K. S. Yeo, and M. A. Do, "9.3-10.4 GHz-band cross-coupled complementary oscillator with low phase-noise performance," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 4, pp. 1273–1278, Apr. 2004.

[12] B. Park, S. Lee, S. Choi, and S. Hong, "A 12 GHz fully integrated cascade CMOS LC VCO with q-enhancement circuit," IEEE *Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 133–135, Feb. 2008