A Miniature 10MHz–3GHz Sub 1-dB NF Cryogenic Inductorless Noise-Canceling Low-Noise Amplifier for Qubit Readout

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***Abstract*—This paper presents an inductorless wideband cryogenic low-noise amplifier (LNA) by the current reuse feed-forward noise canceling technique in 40-nm CMOS. The proposed LNA consists of a complementary input stage with self-forward body bias (SFBB) for low-power operation, which can also compensate for V_{th} reduction and improve r_{out} under cryogenic temperature. A noise-canceling stage is used to suppress the channel noise, achieving a sub-1dB noise figure at room temperature. The LNA attains a measured gain (S_{21}) of 25.6 dB with a minimum noise figure of 0.63 dB at 1.8 GHz. At 4K, it shows a measured gain of 29 dB with a 3-dB bandwidth across 10MHz–3GHz under a power consumption of 19.4 mW. The circuit only occupies a core area of 0.018 mm^2.**

***Keywords*—Noise canceling, Cryogenic LNA, inductorless, Self forward body bias, Current reuse, Quantum computing, Qubits.**

I. Introduction

Quantum computing is a new paradigm and one of the most promising technologies in recent years to solve refractory problems that would impossible to cope with classical computing [1]-[2]. Over the past decade, different qubit technologies have been proposed such as the superconducting qubit, ion trap, photonic qubit, and gate-based spin qubit [3]. However, CMOS-based qubit is still the most attractive solution owing to the large-scale integration level, high reliability, and low cost, which allows for handling millions of qubits for practical quantum computing applications. The CMOS-based controller circuits of spin qubits and transmons have been reported in [4]. The circuit can control 128 qubits on a single chip, and the electronics can operate near the qubits to greatly simplify the system.

LNA is one of the most critical blocks in the qubit readout stage that must operate at deep cryogenic temperature to amplify the weak signals from qubits and meet the lowest possible noise temperature and high gain [2], suppressing noise from the subsequent receiver stages, as shown in Fig. 1. Most reported LNAs with superior RF characteristics for cryogenic quantum computing are implemented with III-V compound semiconductor (InP) [5] or silicon-germanium (SiGe) HBTs [6]-[7], which can ensure signal fidelity requirements for qubits readout but suffer from high system complexity, packaging deficiency, and challenges for integration of large numbers of qubits. Previously published LNAs in the cryo-CMOS show a relatively high-power consumption of 51.1 mW at RT and 39 mW at 4.2 K [10]. Also, a narrow band noise matching with a relatively small gain (S_{21}) of only 13.4 dB at 4.1K has been reported in [11].

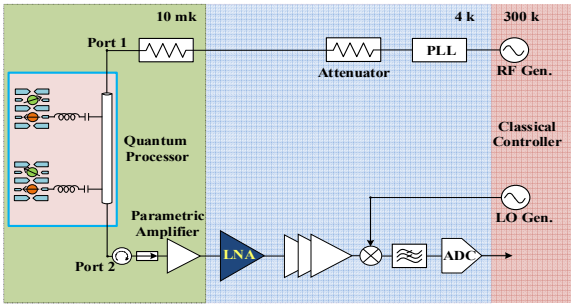


Fig. 1. Block diagram of qubits readout circuits.

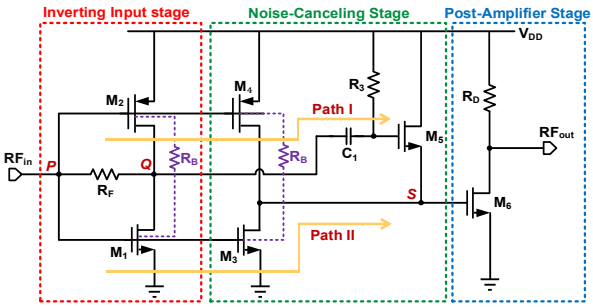


Fig. 2. Circuit topology of the proposed noise-canceling LNA.

In this work, we focus on the CMOS LNA of the receiver block for spin qubits readout based on single electron transistor RF reflectometry with an operating frequency at around several hundred MHz [3]. The proposed inductorless LNA fits the frequency range of the targeted applications. To the best of our knowledge, compared with the reported works, the proposed inductorless CMOS LNA shows excellent NF, gain, bandwidth, and small group delay, while with low power consumption. Also, the circuit occupies a core area of only 0.018 mm^2, which is significantly smaller than other proposed works.

II. Circuit Topology and Design Considerations

Fig. 2 shows the proposed sub 1-dB noise figure inductorless noise-canceling self-forward body bias low-noise amplifier. Noise-canceling (NC) is an appealing technique for LNA design to achieve a very low noise figure (NF). The common-gate (CG) noise-canceling technique has been reported in [13], in which the common-source (CS) stage is used to suppress the channel thermal noise of the main CG amplifier by proper sizing of the transistors. However, this

topology still suffers from a relatively large NF (> 2 dB) due to input impedance, and the noise figure of the common-gate (CG) transistor is inversely proportional to its transconductance g_m. In this paper, we propose a complementary CS noise-canceling topology to design an inductorless LNA as illustrated in Fig. 2.

A. Inverting Input Stage

The first stage is the inverting input stage formed by the complementary common-source transistors M_1 (90 µm) and M_2 (90 µm), feedback resistor R_F for self-bias, and resistor R_B for body bias [14]. The self-bias topology without additional biasing circuits helps to reduce parasitics and chip area. Different from typical inverter stage design using a larger PMOS than the NMOS, the size ratio of input transistors M_1 and M_2 is close to one for simultaneous input and noise matching, which also improves g_m/I_d while keeping the bias voltage at node P as the desired value. The simplified input impedance of the complementary stage with C_{gd}, and r_{out} neglected can be approximately calculated as:

$$Z_{in} = \left[\frac{1}{j\omega}\left\{\left(\frac{C_{gs1}+C_{gs3}}{C_{gs1}C_{gs3}}\right)\middle\|\left(\frac{C_{gs2}+C_{gs4}}{C_{gs2}C_{gs4}}\right)\right\}\right]\middle\|\left[\frac{1}{(g_{m1}+g_{m2})}\right] \quad (1)$$

At low frequencies, the approximate value of input impedance can be simplified to $1/(g_{m1}+g_{m2})$.

The self-forward body bias (SFBB) can compensate for the increased V_{th} at cryogenic temperature, keeping a similar V_{th} at RT to achieve low-power operation. SFBB also alleviates the output impedance reduction due to cryogenic temperature and short-channel effect. As shown in Fig. 2, the self-forward body bias resistor R_B is connected between the bodies of complementary transistors M_1, M_2, M_3, and M_4 to form a voltage divider self-bias loop for the body-source P-N junction. With an appropriately designed R_B, the current I_B in this loop between the two body terminals of NMOS and PMOS can be controlled. The simulated results shown in Fig. 3 indicate that r_{out} increases and I_B reduces with increased R_B of both transistors. As a result, gain and NF of the LNA can be enhanced due to a reduction in V_{th} and I_B, and increased r_{out}, which also helps to reduce the requisite value of V_{GS} for biasing.

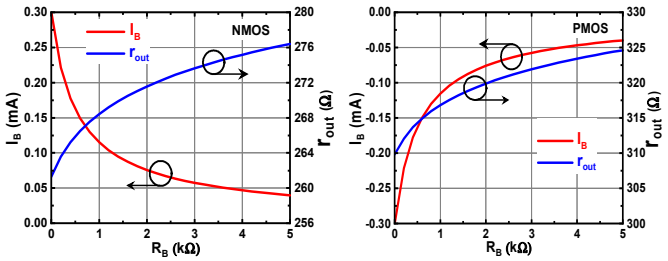
B. Noise-Canceling Stage and Post-Amplifier Stage

The second stage is the current reuse feed-forward noise canceling stage composed of M_3 (144 µm) and M_4 (96 µm) for eliminating channel thermal noise of the inverting input stage, and M_5 (15 µm) for combing the signal from the two paths. Due to inverting operation of input transistor M_1, the noise current of M_1 after being amplified creates in-phase noise voltage between node P and node Q, through the feedback resistor R_F. Also, the out-of-phase amplified voltage signals appear at P and Q, respectively. The noise and signal voltage of node Q (out-of-phase) then enter the source follower transistor M_5, appearing at node S (path I). On the other hand, the noise and signal voltages with the same phase at node P follow path II, and are both amplified and inverted through transistor M_3. As a result, the out-of-phase noise voltages cancel out at node S while the signal voltages are added up. Note that the minimum channel length is not used for M_3 and M_4. Instead, a 60-nm channel length of both transistors is selected to reduce the carrier quasi-ballistic transportation through the junction, which helps to suppress transistor channel shot-like noise [12] and increase gain due to improvement in the output impedance.

The post-amplifier stage is a common-source amplifier stage for gain enhancement without using additional gate bias. This stage also serves as a buffer stage for 50-Ω output impedance matching. The total voltage gain of LNA can be expressed as $A_{v,core} \times A_{v,buffer}$, where the simplified value of $A_{v,core}$ is (R_L is the 50 Ω load):

$$A_{v,core} = [g_{m5}(1-(g_{m1}+g_{m2})R_F)-(g_{m3}+g_{m4})]R_{out} \quad (2)$$

where $R_{out} \cong 1/g_{m5}$ and $A_{v,buffer} = g_{m6}(R_D \| R_L)$.

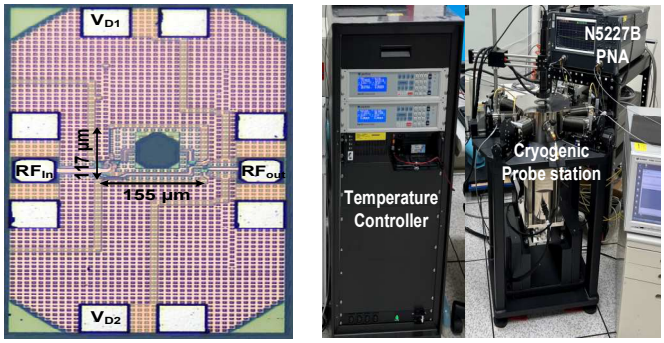


(a) (b)

Fig. 3. Simulated results of substrate current I_B and output resistor r_{out} versus R_B (a) NMOS. (b) PMOS.

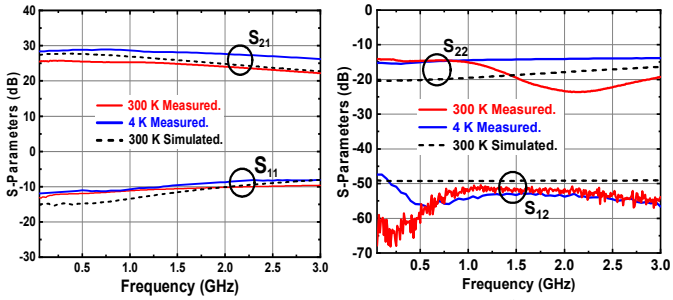
III. Measured Results and Dissuasion

Fig. 4(a) shows the chip micrograph of the fabricated inductorless noise-canceling LNA in 40-nm CMOS with a core area of only 0.018 mm^2. The S-parameters at room temperature were measured by on-wafer probing using the Keysight (PNA-XN5247B) vector network analyzer, consuming 43.4 mW from a 1.2-V power supply.



(a) (b)

Fig. 4. (a) Chip micrograph of the proposed LNA. (b) Cryogenic probe station measurement setup.



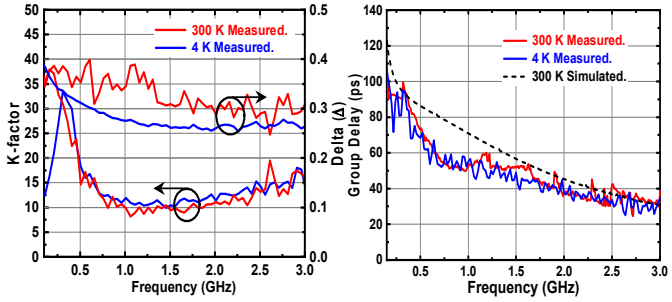
(a) (b)

Fig. 5. Measured (both RT and 4K) and simulated (a) S_{21} and S_{11}. (b) S_{22} and S_{12}.

Table 1. Performance comparison of reported cryogenic LNAs

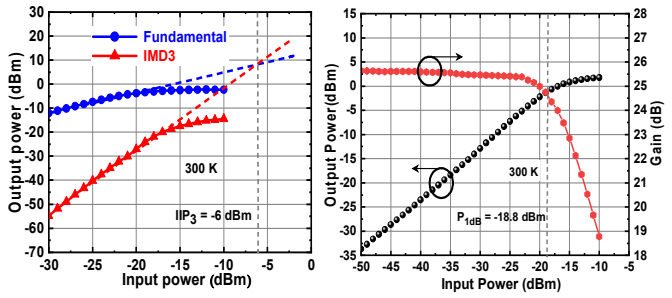
Ref.	This Work	TCAS-I'19 [8]	MWCL'22 [9]	JSSC'21 [10]	RFIC'22 [11]	JSSC'22 [12]
Topology	Noise Canceling + Current Reuse + SFBB	Cascode CS	CS Folded-Cascode	Cascode +R-C loading + XFMR load	Cascode + L- loading + Current Mirror	Cascode inverter + C-feedback + Gate L
Technology	40 nm CMOS	180 nm CMOS	65 nm CMOS	40 nm CMOS	14 nm FinFET CMOS	28 nm
Inductor	No	Yes	Yes	Yes	Yes	Yes
Voltage (V)	1.2	1.8	1.2	1.4	N/A	1.04
Frequency (GHz)	0.01 ~ 3	2.0 ~ 2.12	0.9 ~ 1.8	4.6 ~ 8.2	5.8 ~ 8.3	6 ~ 8
Meas. Temp. (K)	4	77	20	4.2	4.1	4.2
Power (mW)	19.4	15	125	39	2.57	4.2
Gain (dB)	29	18	37.2	39.2 ~ 44.8	13.4	> 54^ (simulated)
NF (dB)#	0.63 ~ 1.4	1.52 ~ 2	N/A	0.75 ~ 1.3	N/A	2.5 ~ 3.5
NF (dB)*	N/A	0.48	0.03 ~ 0.13	0.23 ~ 0.65	0.53 ~ 0.57	0.4 ~ 0.7
S_{11} (dB)	-11.2 ~ -8.3	-40 ~ -15	>10	-26 ~ -5.8	>10	< -4
Area (mm^2)	0.018+	N/A	1	0.72	0.56	0.2+

#Room temperature; *Cryogenic temperature; +Core Area; ^Room temperature simulation



(a) (b)

Fig. 6. (a) Measured K-factor and delta. (b) Measured and simulated group delay (GD).



(a) (b)

Fig. 7. (a) Measured input third-order intercept point (IIP_3) at 0.8 GHz (10MHz frequency spacing). (b) Measured 1-dB compression point at 0.8 GHz.

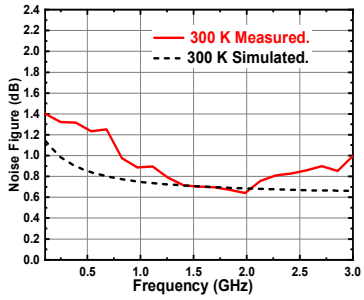


Fig. 8. Measured and simulated NF referring to 300 K.

The cryogenic S-parameters measurements were also performed on-wafer using a Lake-shore CPX probe station at 4K with Keysight N5227B PNA, as shown in Fig. 4(b) of the setup. Note that the total power consumption of LNA decreases to 19.4 mW at 4 K. Fig. 5(a) and 5(b) show the measured and simulated S-parameters at room temperature and the measured results at 4 K. At room temperature, the LNA attains measured $S_{21,max}$ of 25.6 dB at 0.8 GHz, and f_{3dB} of 10 MHz–2.7 GHz with S_{11} better than -10 dB. While at 4 K, the LNA shows measured $S_{21,max}$ of 29 dB at 1 GHz, and f_{3dB} of 10 MHz–3 GHz and S_{11} is (-11.2 ~ -8.3 dB) for 10 MHz–3 GHz. In addition, the LNA shows measured S_{22} better than -15 dB and S_{12} better than -50 dB in the 3-dB bandwidth. Fig. 6(a) presents the stability factor of the LNA, which indicates unconditional stability at both temperatures. The overall measured group delay (GD) less 90 ps for both 300 K and 4 K agrees very well with the simulated results as shown in Fig. 6(b).

Fig. 7(a) shows the measured two-tone linearity tested at 0.8 GHz and 0.81 GHz as an IIP_3 of -6 dBm at room temperature. Fig. 7(b) shows the measured $P_{1\text{-}dB}$ at 0.8 GHz of -18.8 dBm, which is sufficient for the weak reflected power from the qubit. Fig. 8 shows the simulated and measured NF at room temperature, which was done by Agilent N8975A noise figure meter. The LNA attains NF of 0.63–1.4 dB with a minimum value of 0.63 dB at 1.8 GHz, across 10 MHz–2.7 GHz. Note that the noise figure measurement was not conducted at 4K due to the limitation of on-wafer cryogenic measurement capability. Table I shows the performance comparison of cryogenic LNAs. The proposed inductorless low-noise amplifier achieves a remarkable performance among the best compared with previously reported cryogenic LNAs.

IV. Conclusion

In this paper, a miniature 10 MHz–3 GHz wideband inductorless LNA achieving a 0.63-dB noise figure at room temperature has been demonstrated in 40 nm CMOS. The topology using complementary self-forward body bias (SFBB)

for the transistors with a noise-canceling topology was proposed. The SFBB can effectively compensate for the increase of threshold voltage and alleviate the degradation of output impedance at the cryogenic temperature. Also, the noise-canceling technique allows the signal to be added while the undesired noise is canceled for obtaining low noise and high gain performance under low power consumption. The proposed inductorless LNA with a core area of only 0.018 mm^2 is suitable for practical quantum computing applications with large-scale CMOS-based qubits.

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