A 64-Gbaud Transimpedance Amplifier in 130nm SiGe Technology with Effective Broadband Techniques

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***Abstract*—In this paper, a 64-Gbaud transimpedance amplifier in 130nm SiGe technology is presented. The π-network broadband technique and shunt-shunt *RC* feedback are proposed to achieve high gain and wide bandwidth simultaneously. The small-signal results show a transimpedance gain of 50.2 dBΩ with a 3-dB bandwidth exceeding the measurement limit of 67 GHz. An eye-diagram of 64-Gbaud can be obtained with the time domain measurements. The proposed TIA consumes 34.5 mW and occupies a core area of only 0.1 mm².**

***Keywords*—transimpedance amplifier, optical receiver, inductive peaking, PAM4, SiGe technology.**

I. Introduction

The exponentially increased data rate of the optical communication system requires high performance front-end amplifiers [1]-[6]. In addition to improve the amplifier bandwidth, the four-level pulse amplitude modulation (PAM4) scheme has attracted many attentions for obtaining a high data rate recently. Compared with the conventional non-return-to zero (NRZ) signaling, PAM4 allows a doubled bit rate. If a front-end amplifier can achieve a high bandwidth while operating with PAM4 signal format, a much enhanced data rate could be expected. However, this also poses a tremendous challenge in circuit design. Fig. 1 shows the block diagram of a typical optical communication system including the transmitter (Tx) and receiver (Rx). In the receiver end, the transimpedance amplifier (TIA) is one of the most critical blocks, which dominates the overall performance of receiver especially the bandwidth and sensitivity.

Different bandwidth extension techniques were reported for TIA design [6]-[8]. The capacitance of photo diode (CPD) often limits the receiver bandwidth. Also, the parasitic capacitances associated with the active devices in the circuit are crucial. The inductive peaking technique is effective in such high operating speed, while the issues of stability and group delay become critical [5]. In this paper, we propose a TIA topology using both series and shunt inductive peaking with shunt-shunt RC feedback in the transimpedance gain stage. The input CPD is also absorbed into a π-network for bandwidth enhancement. A very large 3-dB bandwidth with a relatively flat frequency response can be achieved regarding the transimpedance gain. Fabricated in 130nm SiGe technology, the TIA shows a measured transimpedance gain > 50-dBΩ gain and a bandwidth > 67 GHz. The PAM4 measurements demonstrate a data rate up to 64 Gbaud.

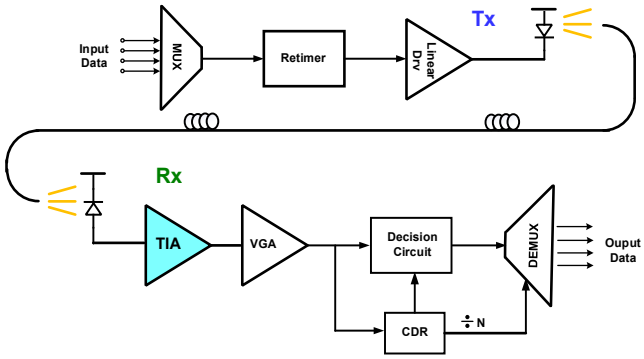

Fig. 1. Block diagram of a typical optical communication system.

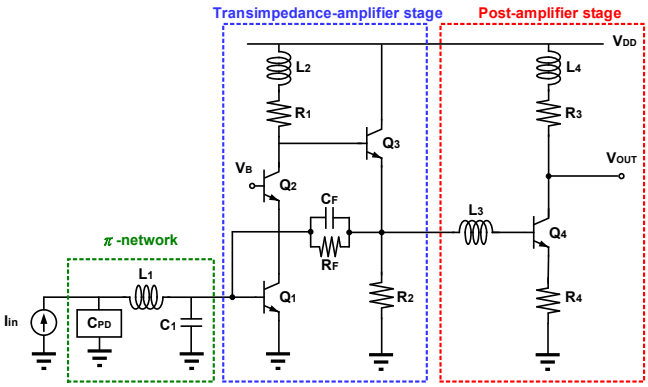

Fig. 2. Circuit topology of the proposed TIA.

II. Circuit Topology and Analysis

Fig. 2 shows the proposed TIA topology, which can be divided into three parts based on the design considerations, including the π-network, the transimpedance gain stage, and the post-amplifier stage.

A. Input π-network

The parasitic capacitance of photo diode (PD) C_{PD} plays an important role to limit the overall bandwidth of the TIA, which can introduce a dominant pole at the input node as $\tau = 1/C_{PD}Z_{in}$. As illustrated in Fig. 2, L_1 and C_1 are designed to form a π-network together with C_{PD}. Compared with using only a series L_1 to resonant with C_{PD} for bandwidth enhancement, the additional C_1 can further flatten the transimpedance gain to achieve a more desired frequency response, as illustrated in Fig. 3. Also, absorbing C_{PD} as a part of the input network can alleviate the impact of parasitic PD capacitance on the overall TIA bandwidth. Note that an

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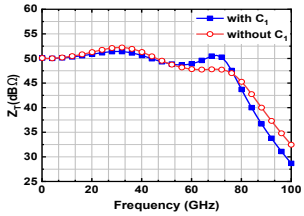

Fig. 3. TIA transimpedance gain w/i and w/o C1 at the input network.

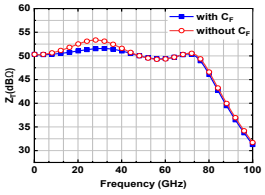

Fig. 4. TIA transimpedance gain w/i and w/o C_F in the shunt-shunt feedback.

on-chip MIM capacitor of ~ 60 fF is employed to emulate the effect of C_{PD} in the design, which is a typical value for a high-speed photo diode. It should be mentioned that the increased gain roll-off rate beyond f_{3dB} with C_1 can also reduce the input referred noise as shown in Fig. 3.

B. Transimpedance Gain Stage

The transimpedance gain stage includes a cascode amplifier (Q_1, Q_2, R_1, L_2), followed by an emitter follower (Q_3, R_2). A *RC* shunt-shunt feedback is employed connecting the emitter of Q_3 back to the base on Q_1. The cascode topology with the shunt inductive peaking can achieve a very high gain with a wide bandwidth. The emitter follower allows a low output impedance for the post-amplifier stage.

Lowering the input impedance Z_{IN} is essential to achieve a high-speed TIA, and the shunt-shunt resistive feedback is often adopted as an effective technique [12]. As shown in Fig. 2, a capacitor C_F is used in parallel with R_F to form an *RC* shunt-shunt feedback, which introduces an additional zero in the feedback network. The frequency dependent feedback provides a freedom to further optimize the frequency response. In practical design, C_F can be used to adjust the gain peaking frequency. The ripple of transimpedance gain Z_T can be reduced with C_F as shown in Fig. 4, which is helpful to optimize the group delay.

C. Post-amplifier Stage

The post-amplifier stage is a common-emitter amplifier with both series and shunt inductor peaking L_3 and L_4 respectively for bandwidth enhancement. Note that the series inductor L_3 combining with the parasitic capacitance at the emitter of Q_3 and base of Q_4 can also be viewed as a π network to effectively broaden the bandwidth. It should be emphasized that linearity is a critical issue to meet PAM4 operation requirement. The adopted 130nm SiGe technology exhibits a very large transconductance. Using the source degeneration resistor R_4 allows reducing the voltage gain and resulting in an improved linearity with increased bandwidth simultaneously. The post-amplifier also works as a buffer stage with a 50 Ω output impedance for the high frequency measurement environment.

III. Measurement Results and Discussion

Fig. 5(a) shows the chip micrograph of proposed TIA fabricated in 130nm SiGe technology with a core area of only 0.1 mm^2, which was tested by on-wafer probing. The *S*-parameters were measured with Agilent N5247A network analyzer with a total power consumption of 34.5 mW. Fig. 5(b) shows the measured *S*-parameters with an S_{21} of 15.6 dB at low frequencies and a bandwidth up to 67 GHz limited by the

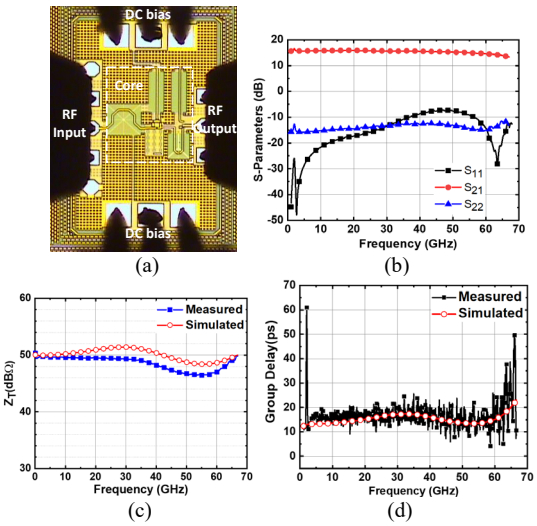

Fig. 5. (a) Chip micrograph of the proposed TIA. (b) Measured *S*-parameters. Simulated and measured (c) Z_T, and (d) group delay of the TIA.

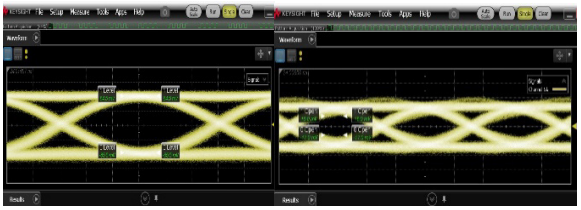

Fig. 6. Measured electrical NRZ eye-diagrams (a) 50-Gb/s (b) 64-Gb/s (PRBS 2^7-1, $V_{in,pp}$ = 25 mV, 50Ω, 60mV/div).

Fig. 7. Measured electrical PAM4 eye-diagrams (a) 50-Gbaud (b) 64-Gbaud (PRBS 2^7-1, $V_{in,pp}$ = 50 mV, 50Ω, 65mV/div).

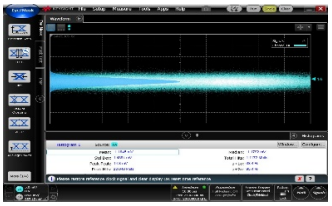

Fig. 8. Measured output integrated noise of the proposed TIA.

Table 1. Performance summary and comparison with prior works

Ref.	2014 [9]	2019 [10]	2013 [11]	2017 [12]	2018 [13]	This work
Technology	65 nm CMOS	16 nm FinFET	130 nm BiCMOS	40 nm CMOS	130 nm BiCMOS	130 nm SiGe
Modulation format	NRZ	PAM-4	NRZ	PAM-4	PAM-4	PAM-4
Bit rate	52 Gb/s	106.25 Gb/s	50 Gb/s	28 Gbaud	50 Gbaud	64 Gbaud
Bandwidth (GHz)	50	27	53.8	16	42	> 67
Z_T (dBΩ)	55	78	56.7	N/A	68.5	50.2
Input-referred noise ($\frac{pA}{\sqrt{Hz}}$)	22.4	16.7	12.3	20.2	8	29.1
Power consumption (mW)	49.2	60.8	21.2	120	150	34.5
Chip area (mm^2)	0.48$^+$	0.19	0.16	0.21$^+$	0.42	0.1$^+$

$^+$Core area

equipment. The transimpedance gain Z_T can be obtained from the measured S-parameters expressed as [13]

$$Z_T = Z_0 \times \frac{S_{21}}{1+S_{11}} \quad (1)$$

where Z_0 is the characteristic impedance 50 Ω. The measured transimpedance gain is shown in Fig. 5(c), which is 50.2 dBΩ at low frequencies with a 3dB bandwidth exceeding 67 GHz. Fig. 5(d) compares the measured and simulated group delay, which is below 26 ps up to 60 GHz.

Measurements of the electrical eye-diagram with both NRZ and PAM4 signal formats were performed by the pattern generator (Anritsu MP1800A) and the sampling scope (Keysight 86100D). Fig. 6(a) and 6(b) show the measured NRZ eye-diagrams with the data rates of 50 Gb/s and 64 Gb/s, respectively. Fig. 7(a) and 7(b) show the measured PAM-4 eye-diagrams with the data rates of 50 Gbaud and 64 Gbaud, respectively.

Fig. 8(a) presents the output integrated noise of TIA with input open circuited, measured by the sampling scope (Keysight 86100D). The average input referred noise current can be determined by the following equation [13],

$$I_{n,in,avg} = \frac{I_{n,in,total}}{\sqrt{noise\ bandwidth}} \quad (2)$$

Table 1 shows the performance summary of the TIA with the comparison of prior works. The proposed TIA demonstrates the largest bandwidth and achieves the highest bit rate with a low input-referred noise. The performance of the proposed TIA is among the best compared with the works listed in Table 1.

IV. Conclusion

In this paper, a high performance transimpedance amplifier has been demonstrated in 130 nm SiGe technology. A π-network absorbing the photo diode parasitic capacitance was designed at the input to improve the frequency response. The cascode transimpedance gain stage with RC shunt-shunt feedback was effective for achieving a very wide bandwidth. Also, the series and shunt peaking techniques were employed in the proposed circuit to further enhance the bandwidth and gain. The measured results showed a 50.2 dBΩ transimpedance gain and larger than 67 GHz bandwidth. A clear eye-diagram up to 64-Gbaud can be obtained. The proposed TIA demonstrated performance among the best compared with prior published works.

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