A 64-Gb/s 4.2-Vpp Modulator Driver Using Stacked-FET Distributed Amplifier Topology in 65-nm CMOS

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***Abstract*—A high swing, 64-Gb/s optical modulator driver is demonstrated in 65 nm CMOS technology. The design is based on the distributed amplifier (DA) topology together with stacked-FET and shunt peaking techniques to obtain high gain and large bandwidth, while is also capable of protecting the MOS transistor under large output voltage swing. The stacked-FET distributed amplifier can reach an operating data rate of 64-Gb/s with 4.2 Vpp, which achieves the largest voltage swing at the highest data rate compared with other works in a similar CMOS technology.**

***Keywords*—distributed amplifiers, silicon photonics, broadband amplifiers, high power amplifiers, electrooptic modulators.**

I. Introduction

It is predicted that the number of connected devices could surge to 50 billion by 2020 with the revolution of 5G communications and Internet of Things (IoT). With the tremendous growth of data transmission rate, the high speed optical communication with advantages of large bandwidth, low loss and less interference plays an essential role as the backbone network in the upcoming 5G era [1]-[4]. Fig. 1 shows the transmitter end of an optical communication system, where the optical modulator is essential for high speed fiber communication because the direct modulation of laser has a limited bandwidth. Today, the silicon-based Mach-Zehnder Modulators (MZM) has been demonstrated for a modulation rate above 50-Gb/s [5]. However, the modulator drivers are required to provide sufficient output swing for achieving a sufficient extinction ratio [1]. Under the large output swing, the driver circuits may encounter the gate-oxide breakdown issue especially in CMOS technology. Typically, the gate-oxide breakdown voltage of advanced process such as node 65, 40, and 28 nm is less than 1 V. Several protection techniques were reported [3]-[4].

In this paper, a 64-Gb/s 4.2 Vpp differential modulator driver fabricated in 65 nm CMOS is demonstrated. The proposed modulator driver employs the distributed amplifier (DA) topology with stacked-FET stages to achieve a large output swing, whilst preventing transistor breakdown. In addition, the characteristics of high gain and large bandwidth can be obtained simultaneously.

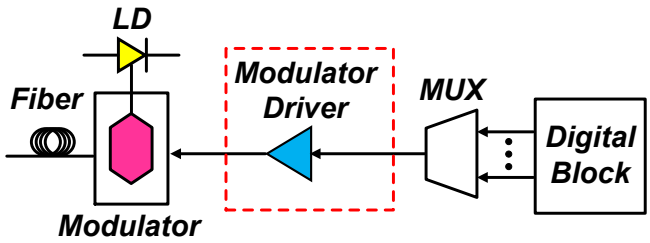

Fig. 1. Transmitter block diagram in an optical communication system.

II. Circuit and Analysis

A. Distributed Amplification

The distributed amplifier (DA) is a widely used topology for various applications. By advantages of combining external inductors and intrinsic parasitic capacitors to form the artificial transmission line with carefully sizing the transistors and inductors, a wide bandwidth can be obtained [6]-[10].

Normally, the gate and drain lines are very long due to several stages of gain cells, which are required to achieve enough gain and output power. In this design, the spiral inductors with patterned ground are used in order to increase the Q factor of inductors. For the unit gain cells, instead of the conventional cascade topology (see Fig. 2(a)), the stacked-FET (Fig. 2(b)) is used to prevent gate-oxide breakdown which is only about 1 V in 65 nm CMOS technology. One of the reasons that limits the bandwidth of DA is the low self-resonant frequency of gate line and drain line inductor. To obtain high output power, sizes of transistors must be increased. The inductances of gate and drain lines must be increased also to compensate the transistor parasitic capacitances and maintain the characteristic impedance, which results in low self-resonant frequency and reduced bandwidth. In practical design, the transistor sizes of gain cells must be carefully selected with optimized inductor layout to obtain wide bandwidth and sufficient output swing.

B. Stacked-FET Topology

To prevent transistor breakdown under large output swing, the stacked-FET topology is adopted which has been reported for RF power amplifier design [11]-[12]. Compared with the conventional cascode topology as shown in Fig. 2(a), the stacked-FET employs three transistors stacked in series to

distribute the drain voltage as shown in Fig. 2(b), which allows improved output swing. One major issue for such vertically amplified configuration is the large gate-drain voltage drop on the top transistor if the gate voltage is fixed. In the proposed design, R_i is the biasing resistor to provide DC voltage, and the added gate capacitance C_i forms a voltage divider with the transistor parasitic gate-source capacitance $C_{gs,i}$ to let the amplified signal at each source of the stacked transistors appear at the gate through $C_{gs,i}$. As illustrated in Fig. 2(b), the gate voltage can swing with the input signal to reduce the voltage drop between drain and gate nodes, thus obtaining gate-oxide breakdown protection.

It should be emphasized that the biased resistor R_i plays a role in the proposed design, which is quite different from the narrow band RF applications. By neglecting the effect of gate-drain capacitance C_{gd}, the input impedance Z_{si} looking into the source of each transistor can be derived as,

$$Z_{si} \approx [1 + j\omega C_{gs,i}(R_i \parallel \frac{1}{j\omega C_i})] \cdot \frac{1}{g_{m,i}} \quad (1)$$

where $g_{m,i}$ is the intrinsic transconductance of each stacked transistors. With a large R_i, Z_{si} can be simplified as

$$Z_{si} \approx [1 + (\frac{C_{gs,i}}{C_i})] \cdot \frac{1}{g_{m,i}} \quad (2)$$

As a result, Z_{si} becomes frequency independent. From a different point of view, R_i and $C_{gs,i}$ form a high pass filter, hence a large R_i can push the cut-off frequency to a very low value. The high pass effect can be seen in Fig. 3(a). With R_1 = 10k Ohm, Z_{s1} remains constant down to a very low frequency, while the high pass characteristics is clearly observed for R_1 of 0.5 and 1k Ohm. The result is consistent with the prediction from (2). The extension of low frequency operation can not only improve the signal integrity, but is also critical to the breakdown protection of transistor, as demonstrated in time domain simulation. Fig. 3(b) indicates an increased voltage drop between node D_1 and G_1 with reduced R_1 (see Fig. 2(b)). For R_1 = 0.5k and 1k Ohm, protection would fail if a long run of 1 or 0 are transmitted for optical communication (V_{DG} exceeds 1 V). Although with the advantage of improved output swing of stack-FET topology, one issue is that the parasitic capacitance looking into the source of stacked-FET is much higher than the cascode topology due to Miller effect with increased Z_{si} as shown in Fig. 4, which will result in limited bandwidth. A shunt peaking common-source amplifier is added in each unit gain cell to resolve this problem in the proposed design. According to simulation, the circuit can only achieve a 3-dB bandwidth about 28 GHz without shunt peaking technique. With shunt peaking, the 3-dB bandwidth can reach up to 34 GHz. The entire circuit configuration is shown in Fig. 5. Note that differential topology is used consisting of four gain stages in each distributed amplifier.

III. Results and Discussion

A. Small-Signal Measurements

The proposed modulator driver using stacked-FET stage distributed amplifier was implemented in 65 nm CMOS as shown in Fig. 6(a). The differential S-parameters were measured by the 4-port Keysight N5247A network analyser

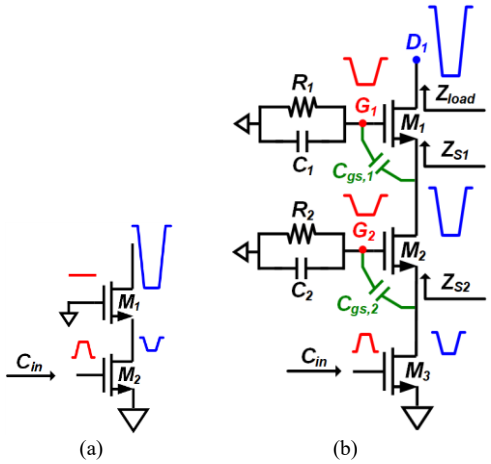

Fig. 2. (a) Cascode topology. (b) Stacked-FET.

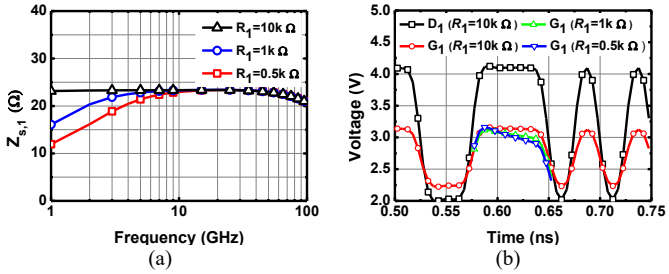

Fig. 3. (a) Simulated Z_{S1} with R_1=10k, 1k and 0.5k Ohm. (b) Simulated waveform at D_1 and G_1 with different R_1

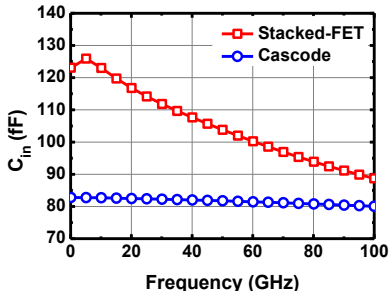

Fig. 4. Comparison of input capacitance of stacked-FET and cascode topology.

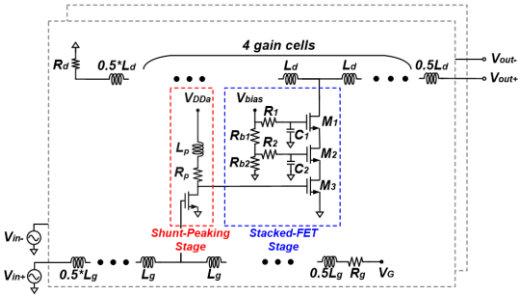

Fig. 5. Circuit topology of the proposed modulator driver.

with a total power consumption of 960 mW. The driver achieves a power gain of 15 dB and a 3-dB bandwidth of 34 GHz as shown in Fig. 6(b). Although the 3-dB bandwidth is relatively small, the gain maintains above 8 dB up to 45 GHz. The input and output reflection coefficients remain below -10 dB up to about 50 GHz as shown in Fig. 6(c) and 6(d).

Table 1. Comparison of state of art modulator driver.

Ref.	Technology	Data-Rate (Gb/s)	Gain (dB)	BW (GHz)	Swing (V)	Power (mW)	Area (mm^2)
[1]	65nm CMOS	25	-	-	3.3	480	0.72
[2]	65nm CMOS LP	30	11.5	-	1.68*	323	0.13+
[3]	90nm CMOS	40	17	28.2	4	650	0.936
[4]	45nm CMOS SOI	40	7.6	33	4.5	437	0.38
This Work	65nm CMOS	40/64	15	34	4.5/4.2	960	1.54

*Single-ended; +Core area

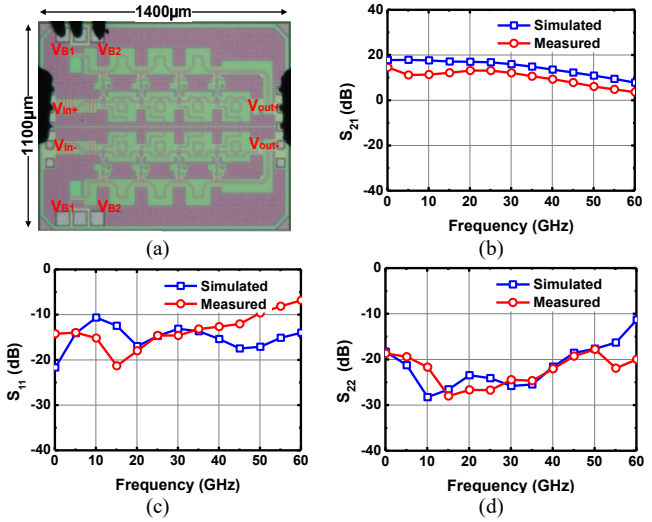

Fig. 6. (a) Chip photo (b) Measured and simulated S_{21} (c) S_{11} and (d) S_{22}

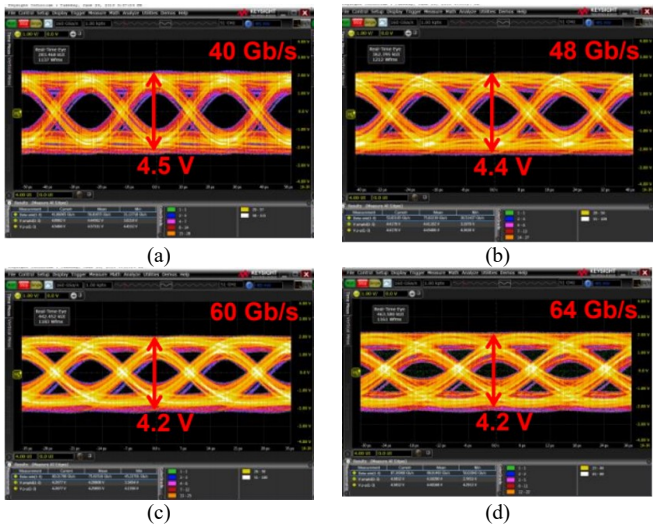

Fig. 7. Measured eye diagrams: (a) 40-Gb/s: (b) 48-Gb/s: (c) 60-Gb/s: (b) 64-Gb/s

B. Large-Signal Measurements

The large-signal measurements were performed using the Anritsu MP1800A pattern generator and the Keysight DSOZ504A Infiniium real time oscilloscope. Note that the differential eye diagram was measured up to 64-Gb/s. Fig. 7(a), 7(b), 7(c) and 7(d) show the measured electrical eye diagrams of the modulator driver with differential output at 40-Gb/s, 48-Gb/s, 60-Gb/s and 64-Gb/s, respectively. The measured results demonstrate that the differential voltage swing can reach up to 4.5 V_{pp} at 40-Gb/s including the cable loss. Even at the speed of 64-Gb/s, a clear eye with 4.2 V_{pp} output swing can still be observed. Table I shows the comparison with previous works. Compared with [1] and [2] also by 65 nm CMOS, the proposed circuit based on the DA and stacked-FET topology has the advantage of high speed operation with large output swing. In addition, this design achieves a higher gain and bandwidth using a standard CMOS technology compared with [4], but the power consumption and chip area also increase.

IV. Conclusion

A modulator driver with high operating speed and large output swing based on distributed amplifier with stacked-FET gain cell were demonstrated in 65 nm CMOS. The stacked-FET topology with RC network allows achieving large output swing with breakdown protection. The increased parasitic capacitances of stacked-FET topology was resolved by a shunt peaking amplifier in the gain cell. The circuit achieved differential output swing of 4.5 and 4.2 V_{pp} at 40 and 64-Gb/s, respectively.

Acknowledgment

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