A Sub-6 GHz Compact GaN MMIC Doherty PA with a 49.5% 6 dB back-off PAE for 5G Communications

Sih-Han Li[1,2], Shawn S. H. Hsu[1], Jie Zhang[2], and Keh-Ching Huang[2]
[1]Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan
[2]Electronics and Optoelectronics System Research Laboratories,
Industrial Technology Research Institute, Hsinchu, Taiwan.

***Abstract*—This paper presents a sub-6 GHz MMIC Doherty power amplifier (DPA) for 5G communication applications based on a 0.25-μm GaN HEMT process. The impedance inverter of the DPA is realized by combining a compact transmission line network with two shunt capacitors. Also, the ratio of power cells in the main and auxiliary amplifiers is optimized to achieve a high efficiency in output power back-off. The measured peak output power and P_{1dB} are 38.7 and 32.1 dBm, respectively at 5.9 GHz. The power-added-efficiency (PAE) at a 6-dB output power back-off is up to 49.5 %.**

***Index Terms*—Gallium Nitride (GaN), MMIC, Doherty, power amplifier, PAE, 5G communication.**

I. Introduction

The rapid growth of data communications over wireless networks is foreseen to continue at an accelerating pace into next decade. The 5G communications definitely play a critical role in this roadmap, and the frequency spectrum is allocated below 6 GHz and up to millimeter-wave range [1]. It is expected that the sub-6 GHz band would be utilized ahead of the mm-wave frequency with a strong commercial demand. Compared with the current 4G LTE architecture, a major difference in the 5G blueprint is the widely deployed small cells for achieving ultra-dense networks. One important issue to realize high efficiency small cells is the power amplifier (PA) of the transmitter. The GaN-based devices are an excellent choice for such applications owing to the high electron saturation velocity and large breakdown voltage [2].

The Doherty power amplifier (DPA), in which the load impedances can be modulated by combining a main amplifier and an auxiliary amplifier with an impedance inverting network (IIN), has proven to be a very good candidate to achieve a high efficiency in output power back-off. This configuration allows obtaining an excellent signal amplification efficiency with modulation schemes of high peak−to-average power ratio (PAPR), which are employed to many modern wireless communication systems.

In this work, we propose using GaN technology to design a sub-6 GHz MMIC DPA for small cell applications in 5G communications. The IIN is designed initially with a 100-ohm system to reduce the circuit complexity. Using the proposed impedance conversion technique to combine with properly designed power cells, the limitation from process is overcome and the output networks are effectively simplified. The similar approach is applied to the input networks and a compact DPA is achieved.

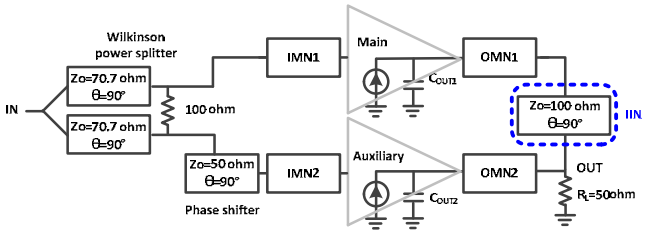


Fig. 1. Function blocks of the proposed DPA.

II. Circuit Design and Analysis

Fig. 1 shows the proposed DPA configuration including the Wilkinson power splitter, phase shifter, input/output matching network (IMN/OMN), main and auxiliary amplifiers, and the impedance inverter network (IIN). The main amplifier is biased at class AB, while the auxiliary amplifier is at class C in typical design. As a result, the auxiliary amplifier is turned off at lower power level to maintain the efficiency. Also, the impedance converter plays a critical role for the load modulation to achieve a high power back-off PAE.

Although widely used, one challenge remains for DPA design, especially for MMIC implementation, is to obtain a compact on-chip impedance converter. In the conventional design, the impedances of both amplifiers are matched to 50 ohm, and an impedance converter in addition to the quarter-wave transformer is needed to change the overall impedance back to 50 ohm [3]. This indeed causes two issues. The transmission line (TML) based impedance converter could occupy a considerable chip area. Also, the IC process often results in limitation of the characteristic impedance Z_0 for practical TML. As shown in Fig. 1, a different IIN is proposed to solve these problems. The initial design is based on the 100-ohm TML system to remove the extra impedance converter, followed by the Δ-Y conversion to further simplify the network by combining the IIN with output matching network of the

amplifier. Also, the impedance of the TML is adjusted to the more practical values in the final design according to the adopted 0.25-μm GaN technology. Another critical concern is design of the power cells in the main and auxiliary amplifiers, which is considered together with the IIN to achieve a compact and high efficiency DPA.

A. Design of Power Cells

The target output power level of the proposed DPA is about 10 W (40 dBm) for 5G small cell applications. The transistor peripheries of the power cells are determined mainly based on this criteria. In addition, achieving high gain and high PAE simultaneously is an important design consideration. It should be emphasized that a relatively large ratio of the transistor size in the auxiliary to main amplifier is essential for high back-off PAE in DPA design [4]. The sizes of the power cells selected in the main and auxiliary amplifiers are 6 × 100 μm and 12 × 100 μm with the corresponding f_T/f_{max} of 27/49 GHz and 25/43 GHz, respectively. With the help of load-pull simulation, the optimum output impedances (mainly for high back-off PAE) of the main amplifier and auxiliary are 23.3-j42.2 ohm and 7.3-j25.9 ohm, respectively, as illustrated in Fig. 2(a). As mentioned, the 100-ohm system is employed to simplify the impedance conversion design. Fig. 2(a) also indicates that the output matching networks in both signal paths (see Fig. 1) can be realized easily by only using two shunt inductors L_{OUT1} and L_{OUT2} to achieve 100 ohm.

B. Design of IIN and IMN/OMN

As illustrated in Fig. 1, the output networks in our initial DPA design employ the 100-ohm TML for impedance inversion network. However, the corresponding line width becomes a main issue in the adopted GaN technology, which is only around 12 μm for the 100-ohm TML. With the maximum DC current density around 30 mA/μm in a double-metal TML structure, the line width is impractically narrow for achieving the desired current level and high output power. Fig. 2(b) illustrates the proposed solution to this issue. First, the *IIN* is equivalent to a π network (L_T and C_T) as shown in Fig. 2(b)-i, where C_{out1} and C_{out2} are the equivalent output capacitances for the power cells, and L_{OUT1} and L_{OUT2} represent the shunt inductors for the OMN of amplifiers. The π-type inductor network (L_T, L_{OUT1}, and L_{OUT2}) is then transformed to a Y-type network network (L_A, L_B, and L_C) by the Δ-Y conversion (see Fig. 2(b)-ii). Finally, the lumped network is converted back to TML-type design for low loss consideration. Note that two shunt capacitors (C_{ADJ1} and C_{ADJ2}) are added to the output nodes of the amplifiers, which allows implementing the TML with more suitable characteristic impedance and line width, and also for a compact MMIC layout, considering the adopted GaN technology. As shown in Fig. 2(b)-iii, Z_A and Z_B are 75 ohm and Z_C is 60 ohm in our final design, corresponding to the linewidths of 35 μm and 65 μm respectively. Also, the electrical lengths of the TMLs are 23.4°, 11.9°, and 7.7° for θ_A, θ_B, and θ_C, respectively.

A similar approach is applied to the design of input network including power splitter, phase shifter, and IMN, which can significantly reduce the chip size of the proposed MMIC. For example, the length of a 90-degree TML for the power combiner and phase shifter is around 5000 μm at 6 GHz, which consume a considerable chip area, causing severe issues in practical layout. By the similar design technique mentioned above, the power splitter and phase shifter can be combined with the IMNs, and the circuit size can be reduced effectively. Fig. 3 shows the details of overall circuit topology of the proposed DPA in our final design.

III. Measured Results and Discussion

Fig. 4 shows the chip micrograph of the fabricated DPA by WIN Semiconductors 0.25-μm GaN technology with a chip size of 2.49 mm × 1.56 mm. The DPA is biased from a 28-V DC supply with a total DC current of 142 mA. Fig. 5(a) shows the large-signal measurement results of the DPA at 5.9 GHz. A peak output power of 38.7 dBm with a PAE of 47.3 % can be achieved. Also, the amplifier shows a P_{1dB} of 32.1 dBm with an associated PAE of 48.8 %. It should be emphasized that an excellent PAE up to 49.5 % is obtained at 6 dB back-off output power, as shown in Fig. 5(b).

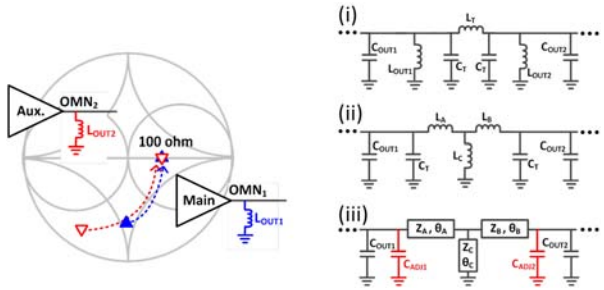


Fig. 2. (a) Output impedance matching for the main and auxiliary amplifiers. (b) Design of IIN and OMN by different impedance conversion techniques.

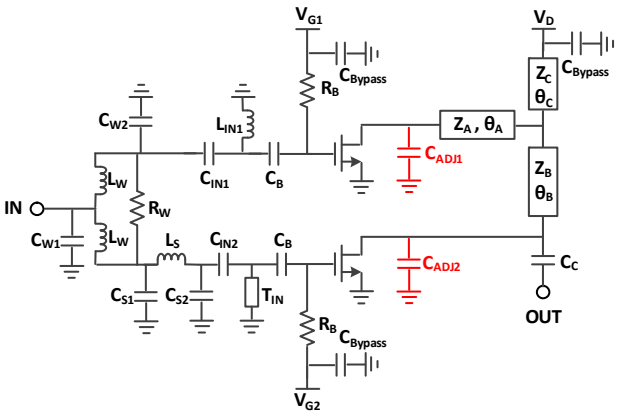


Fig. 3. Circuit schematic of the proposed DPA.

TABLE I
COMPARISON WITH PRIOR WORKS

Ref.	Tech.	Freq. (GHz)	Gain (dB)	Peak P_{out} (dBm)	P_{1dB} (dBm)	PAE at Peak P_{out} (%)	PAE at P_{1dB} (%)	PAE at 6dB back off (%)	Chip-Size (mm×mm)
[5]	GaN 0.25 µm	6.8–8.5	13.5	35	22	38–50	21	35	2.1 × 1.5
[6]	GaN 0.25 µm	5.8–8.8	10	36	30	39	42	31-39	2.9 × 2.9
[7]	GaN 0.25 µm	14.6	7	36	30	40	29[#]	28	3.1 × 1.6
[8]	GaN 0.25 µm	2–6	12.8–13.7	41	--	27–34	--	--	4 × 1.9
This Work	GaN 0.25 µm	5.9	14.4	38.7	32.1	47.3	48.8	49.5	2.49 × 1.56

[#]Drain efficiency

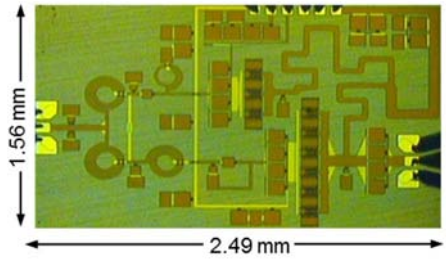
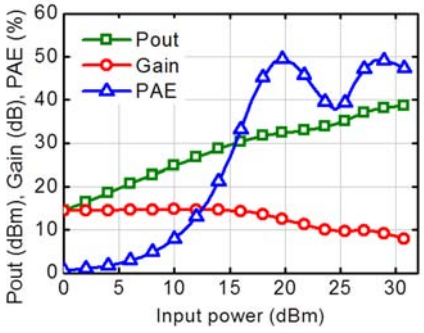
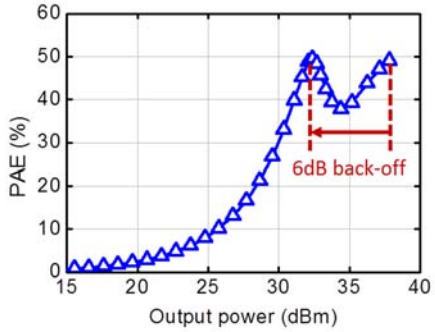


Fig. 4. Chip micrograph of the fabricated DPA in WIN 0.25-µm GaN technology.



(a)



(b)

Fig. 5. Measured results of (a) Pout, gain, and PAE vs. input power (b) PAE vs. output power at 5.9 GHz.

Performance of the proposed DPA is summarized in TABLE I, showing that the DPA can support applications requiring linear amplification at sub-6 GHz. Compare with previous reported results, this work shows the highest 6 dB output power back-off PAE with a very compact area. Also, the output power level and gain are among the highest.

IV. CONCLUSION

A high performance sub-6GHz MMIC Doherty power amplifier for 5G communications has been demonstrated in 0.25-µm GaN technology. With the proposed techniques, the impedance inverter network was combined with the output matching network to achieve a very compact layout, and the limitation of TML characteristic in the adopted technology can be overcome successfully. The measured results showed an maximum output power up to 38.7 dBm, and the PAE at a 6-dB back-off P_{out} can achieve 49.5%, which is among the highest compared with previous works in a similar technology.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC) and National Nano Device Laboratories (NDL) for chip implementation and measurement support.

REFERENCES

[1] IMT-2020 (5G) Promotion Group. (Feb. 2015). *White Paper on 5G concept.* [Online]. Available: http://www.imt-2020.org.cn/zh/documents/download/4

[2] C. W. Tsou, H. C. Kang, Y. W. Lian and S. S. H. Hsu, "AlGaN/GaN HEMTs on silicon with hybrid Schottky-Ohmic drain for RF applications," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4218-4225, Nov. 2016.

[3] Y. Yang, J. Yi, Y. Woo, and B. Kim, "Optimum design for linearity and efficiency of a microwave Doherty amplifier using a new load matching technique", *Microwave Journal*, vol. 44, no. 12, Dec. 2001.

[4] M. Iwamoto, A. Williams, Pin-Fan Chen, A. G. Metzger, L. E. Larson and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2472-2479, Dec. 2001.

[5] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman and C. Fager, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922-930, Feb. 2013.

[6] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov and C. Fager, "A GaN MMIC modified Doherty PA with large bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3006-3016, Dec. 2014.

[7] R. Quaglia, V. Camarchia, J. J. Moreno Rubio, M. Pirola and G. Ghione, "A 4-W Doherty power amplifier in GaN MMIC technology for 15-GHz applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 4, pp. 365-367, April 2017.

[8] D. W. Kim, "An output matching technique for a GaN distributed power amplifier MMIC using tapered drain shunt capacitors," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 9, pp. 603-605, Sept. 2015.