A V-band CPW Bandpass Filter with Controllable Transmission Zeros in Integrated Passive Devices (IPD) Technology

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Abstract — A 60 GHz CPW bandpass filter (BPF) with two controllable transmission zeros is proposed. The BPF, which utilizes the spiral defected ground structure (DGS) and interdigital structure as the resonators, is designed and fabricated on the integrated passive device (IPD) technology. The proposed filter has the measured 3dB bandwidth of 8.53 GHz (56.54–65.07 GHz) with the insertion loss of 4.84 dB including pads. The center frequency is 60.81 GHz, and the maximum return loss is better than 25 dB in the passband. A good agreement between the simulated and measured results has been shown. By comparing to other reported Si-based V-band BPFs, this work achieves a good fractional BW (FBW) of 14% with a compact size of 0.18mm^2.

Index Terms — 60 GHz, system-in-package (SiP), bandpass filter (BPF), CPW, and defected ground structure (DGS).

I. Introduction

The availability of 7 GHz bandwidth in the 60 GHz unlicensed band has been drawing a lot of attention for the next generation wireless communication with high data rate transmission. The bandpass filter (BPF) is one of the most important passive components in radio transceivers to ensure compliance with spectrum regulations. However, the passive circuits always occupy large chip area. To meet the demand of cost and compact design, the system-in-package (SiP) technology is popular to realize millimeter-wave radio front-end by using the integrated passive device (IPD) technology. Unlike the single chip solution has all passive components embedded together with the active circuits. The SiP technology provides flexibility in choosing components to be integrated in a large system on performance and cost concerns. The IPD can provides passive components with large sizes or serves as a carrier substrate. The highly integrating capability, low-cost, and low loss at high frequencies of IPD technology make it become attractive for millimeter-wave BPF design.

For the trends of V-band application, several 60 GHz BPFs had been proposed and were complied with the 802.11ad standard. Two microstrip BPFs with sinuous-shaped resonators [1] showed a great insertion loss below 4dB, but the wide passband over 30 GHz degraded the selectivity. A high selectivity of 10% fractional bandwidth (FBW) was achieved by a coupled-line BPF [2] with the penalty of high insertion loss of 9.3 dB. A planar ring resonator structure BPF [3] implemented in the 0.18um CMOS presented a good selectivity with a fair insertion loss of 4.9 dB. But the chip size of 1.71 mm^2 was too large for integration. A dual-mode rectangular ring BPF [4] showed better performance on both insertion loss and selectivity. But the extra on-chip capacitors were needed to minimize the chip size. In [5], the shielded CPW transmission lines were optimized to construct the BPF with excellent performance. However, the low insertion loss relied on the circuit configuration which made its low frequency transmission cannot be eliminated. Such high demand makes the BPF design with complexity may not be accomplished in a short time. A straightforward design methodology is desired for synthesizing the BPFs in V-band.

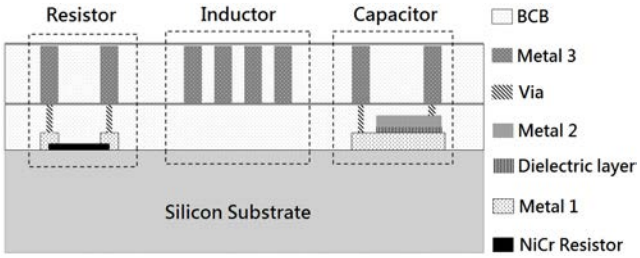

Fig. 1. The cross-section of the IPD technology.

In this work, a 60 GHz CPW BPF with two transmission zeros by using interdigital and DGS structures as series and parallel resonators is proposed. The filter is implemented in a silicon substrate IPD technology as shown in Fig. 1. In section II, the design concept and the full-wave EM simulation of the proposed BPF are depicted. The experimental results and performance comparison are discussed in section III.

II. 60 GHz BPF Design

A. IPD technology

The technology used in this work is the IPD technology which is a passive only process for wireless communication systems or RF applications. Passive components like filter, balun, phase shifter or power divider can be implemented using this process with high resistivity silicon substrate for low cost and high volume production. It enables customers to integrate passive-only circuits with other active devices for multi-chip module (MCM) applications. It has three Cu layers with BCB dielectric layers as shown in the Fig. 1. The interlayer SiN dielectric can form the MIM capacitors, and the NiCr layer is used for RF resistor implementation. The most

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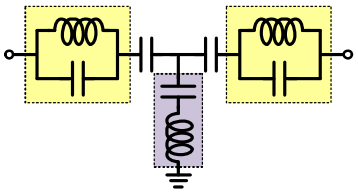

Fig. 2. The equivalent circuit of the proposed BPF.

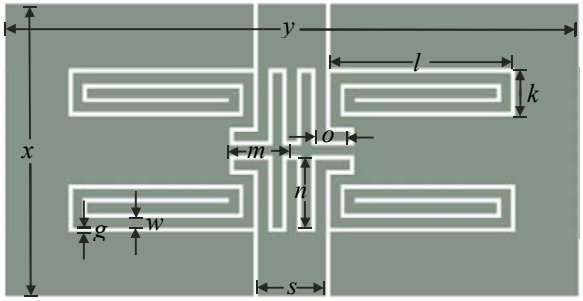

Fig. 3. Layout with dimensions of the proposed uniplanar BPF.

thick layer Metal-3 (12 μm) is designated for inductors, transmission lines, and high Q passive elements.

B. BPF Design

Demand for different bandwidth regulation in 60 GHz, the BPF design is desired to be flexible and time-saved on bandwidth adjustment in the redesign iterations. This concept becomes the design target of this work. A BPF design with three resonators as shown in Fig. 2 is proposed. The series and parallel resonators are utilized to induce two transmission zeros at lower and upper stopband, respectively. And the capacitors are used to eliminate the DC to low frequency transmission. For achieving the BPF performance in V-band, the top metal layer Metal-3 is used in this design. But the layout constraint of this IPD technology makes the BPF design become a challenge. The design rule of Metal-3 has the minimum metal spacing of 5 μm which limits the amount of coupling between metal lines. To realize the strong capacitive coupling, the interdigital structure is implemented in the BPF as shown in Fig. 3. The large length n dominates the lower band transmission zero by the series resonator. On the other hand, the upper band transmission zero is formed by the two parallel resonators. To reduce the chip area effectively, the spiral DGS [6] is adopted. The spiral DGS consists of spiral defects embedded in the uniplanar ground planes. The size of spiral (width k and length l) dominates the frequency of band rejection. While spacing g and metal width w affect the frequency and Q-factor of the response. The smaller the size of defect, the higher the frequency of transmission zero is induced. Besides, the steep roll-off characteristic without scarifying the passband bandwidth of BPF is also important. Furthermore, the spiral DGS provides stronger slow-wave effect compared to a typical dumbbell DGS. Therefore, it exhibits the high potential property of chip size reduction.

To analyze the performance of the proposed filter, EM simulator ADS momentum is used to characterize the S-

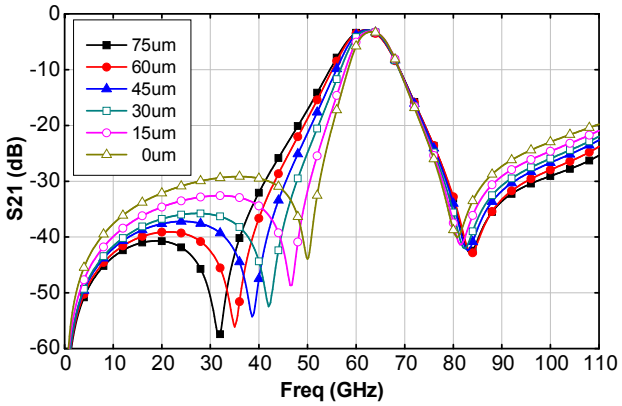

Fig. 4. The effect of the interdigital structure length n on transmission zero at lower band.

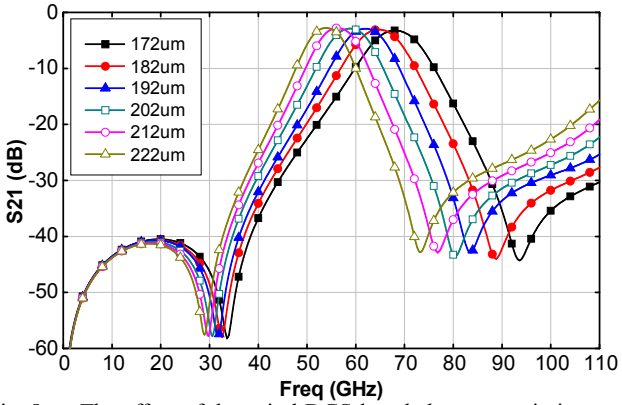

Fig. 5. The effect of the spiral DGS length l on transmission zero at upper band.

parameters over the frequency range up to 110 GHz. The upper band transmission zero around 80 GHz was firstly determined by applying the spiral GDS through calculation. Then the lower band transmission zero can be induced by the interdigital structure. By adjusting the length n from 0 μm to 75 μm, the transmission zero could be moved from 30 GHz to 50 GHz as shown in Fig. 4. Because of the possible application for the V-band front-end, the transmission zero is set around 30 GHz for sub-harmonic rejection. For the upper band, changing l from 172 μm to 222 μm can move the transmission zero from 72 GHz to 93 GHz as shown in Fig. 5. By utilizing these resonators, the desired bandwidth with steep roll-off skirts can be obtained. According to the design goal for covering 57–64 GHz range, the filter was overdesigned and optimized. The dimensions of the proposed filter are specified as follows: l = 192 μm, k = 50 μm, n = 75 μm, m = 50 μm, o = 5 μm, s = 70 μm, w = 10 μm, and all the spacing g in the filter is 5 μm. Including the probing pads, the chip size of the proposed filter is 0.18 mm^2 (x =302 μm, y =594 μm).

III. Experimental Results

The measurement was carried out by a Cascade microwave on-wafer probe station with HP-8510XF GHz vector network analyzer and Agilent E-7350A system from 10 GHz to 110

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

Ref.	Technology	Center Frequency f_0 (GHz)	3dB BW (GHz)	FBW (%)	Min. Insertion Loss (dB)	Max. Return Loss (dB)	Area (mm^2)
[1]	CMOS 0.18 µm	60	31.1	51.8	3.9	20	0.18*
[2]	CMOS 0.18 µm	59.3	6.1	10.4	9.3	15	0.05*
[3]	CMOS 0.18 µm	64	12	18.8	4.9	19	1.71
[4]	CMOS 0.09 µm	59	14.5	24.6	4.2	16	0.12*
[5]	CMOS 0.13 µm	60	10.2	17	4.1	24	0.29
This work	Si-IPD	60.8	8.5	14	4.8	25	0.18

*: core only.

GHz. The simulated and measured S-parameters of the designed BPF are shown in Fig. 6. The measured minimum insertion loss is 4.84 dB including probing pads, which is 2.11 dB worse than that of the simulation. The extra loss is believed to be contributed by the lossy surface of silicon substrate which has been modified by adjusting the surface resistivity of silicon substrate in the future. The 3 dB bandwidth is 8.53 GHz (56.54–65.07 GHz) with the center frequency (f_0) of 60.81 GHz. Though the bandwidth is narrower than the simulation of 9.4 GHz (56.9–66.3 GHz) with the f_0 at 61.6 GHz, it still can cover the 60 GHz application of unlicensed band 57–64 GHz by the overestimation took in the design phase. The measured f_0 only shifts 0.79 GHz lower than the simulated results. And the measured maximum return loss is 25.6 dB. The two transmission zeros provide more than 40dB attenuation at 36.5 GHz and 88 GHz. The measurement and simulation show a great agreement which verify the concept of the proposed design. The measured performance is compared with the previously published results as summarized in Table I. The fractional bandwidth (FBW) is used to quantify the selectivity of a BPF as shown in below.

$$\text{FBW}\,(\%) = \frac{\text{3dB BW}}{f_0} \tag{1}$$

In Table I, [2] achieved the minimum FBW of 10.4, but it suffered from the large insertion loss in the passband. The proposed BPF shows excellent FBW with a reasonable insertion loss, and the chip size is the most compact one among the published BPFs in the Si-based technology.

IV. CONCLUSION

A 60 GHz BPF with spiral DGS and interdigital structures is proposed. Both structures serve as the resonators to control two transmission zeros at stopband. By implementing the proposed filter in the Si-based IPD technology, the minimum insertion loss of 4.84 dB with the 3dB FBW of 14 % is presented. The center frequency is 60.8 GHz, and the maximum return loss is 25.6 dB. The proposed filter shows great performance comparing with other BPFs reported in the previous papers. The compact size of 0.18 mm^2 makes the proposed BPF suitable for V-band applications.

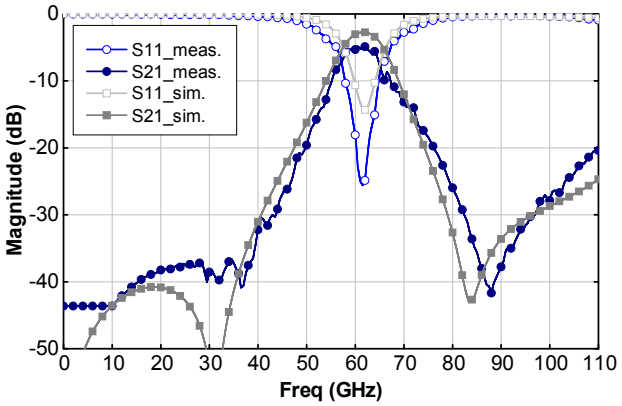

Fig. 6. The measured and simulated S-parameters of the filter.

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