A BiCMOS Monolithic Ka-Band Down-Converter for Satellite Communication Systems

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Abstract — A high performance Ka-band down-converter front-end for satellite communications in 0.18-µm BiCMOS is demonstrated. By using the dual-transformer-feedback design, the low-noise amplifier (LNA) can achieve low noise figure (*NF*) and wide matching bandwidth simultaneously. Also, the G_M-boosted mixer together with the IF amplifier with adaptive bias and 3D inductor provides high gain and high linearity to relax the overall system requirements. The measured *NF* is lower than 6.25 dB with an average conversion gain of 47.5 dB covering the entire RF band from 18.2 to 21.4 GHz. A high linearity (OP_{1dB} > 4.2 dBm) with an excellent gain flatness (±1.5dB) are achieved under a power consumption of only 80 mW. Compared with previously reported works, the presented design has the highest gain and linearity, lower *NF*, and a smallest chip size (core area: 0.24 mm^2).

Index Terms —SiGe BiCMOS, down-converter, double G_M-boosted, adaptive bias circuits, low-noise block (LNB).

I. Introduction

The satellite communication systems have attracted significantly attention recently for remote access of internet and digital broadcasting of HDTV. Many fully-integrated satellite receivers were previously reported for Ku-band (10.7-12.9 GHz) applications [1]-[2], but only a few were studied at the Ka-band (18-40 GHz) using the Si-based technology [3]-[5]. Compared with the Ku-band design, operation at Ka-band allows much higher download/upload data rates with a smaller antenna size, which has a large potential market for various applications. However, the high operating frequency also poses a serious challenge of a fully-integrated solution using Si-based technology. In this study, we propose using a low cost 0.18-µm BiCMOS technology (f_T of only 70 GHz) to achieve a monolithic Ka-band down converter with low noise, high gain, and high linearity under a low power consumption for satellite communications.

In a satellite communication system, the low-noise block (LNB) is of critical importance to the overall receiver performance. Typically, the LNB circuits should guarantee a noise figure (*NF*) lower than 0.6 dB and provide a conversion gain up to 60 dB. The cascaded GaAs HEMT amplifiers are often employed to achieve the system specification and relax the requirements of the succeeding circuit blocks, as illustrated in Fig. 1. Nevertheless, the specifications required for the LNA, mixer, and IF amplifier are still stringent in practical design, where the noise figure should be no more

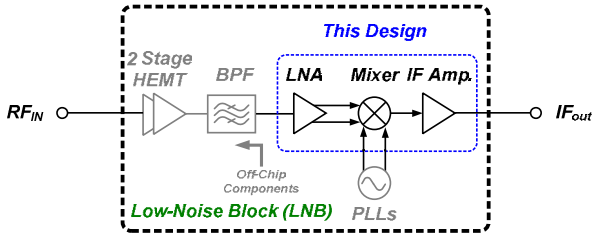

Fig. 1. System block of a Ka-band low-noise block (LNB) [2].

than 8 dB in the entire RF band, and a conversion gain of 40 dB with an output P_{1dB} higher than 0 dBm are also the appropriate characteristics. A 24/31 GHz dual band down-converter was realized in 0.18-µm BiCMOS [3], and the circuit achieved a *NF* lower than 9.5 dB, a gain of about 20 dB with an output P_{1dB} of about -6 dBm. A Ka-band VSAT for satellite connection was reported [4]. Using a 0.25-µm BiCMOS technology (f_T= 130 GHz), a *NF* of 8 dB has been obtained with a conversion gain of 25 dB and output P_{1dB} of -5 dBm. Also, a Ka-band receiver front-end with a 0.13-µm BiCMOS (f_T= 200 GHz) was reported [5], which attained a conversion gain of 17 dB, *NF* of 8.9 dB, and an output P_{1dB} of -8 dBm. As can see, it is really a challenging task to design a down-converter to keep high power gain, low *NF*, and sufficient output P_{1dB} simultaneously. In this work, we propose using a dual- transformer-feedback technique and G_M-boosted mixer circuit topology to achieve an impressive power gain and low *NF*. The adaptive bias technique with the 3D-inductor structure in the IF amplifier also provides excellent output P_{1dB} under a low power consumption and small chip area.

II. Circuit Design

The low-noise amplifier (LNA) is a critical block for the overall circuit performance, which in this design should provide both power and noise matching in a wide frequency range. The widely used LNA configuration with source degeneration inductor suffers from a design trade-off between the matching bandwidth and the optimal noise figure, which can be solved by the transformer feedback technique [6]. In this study, we propose using the dual-transformer-feedback topology to further enhance the circuit performance, which promises much improved matching bandwidth and increased G_M for suppressing the internal noise sources.

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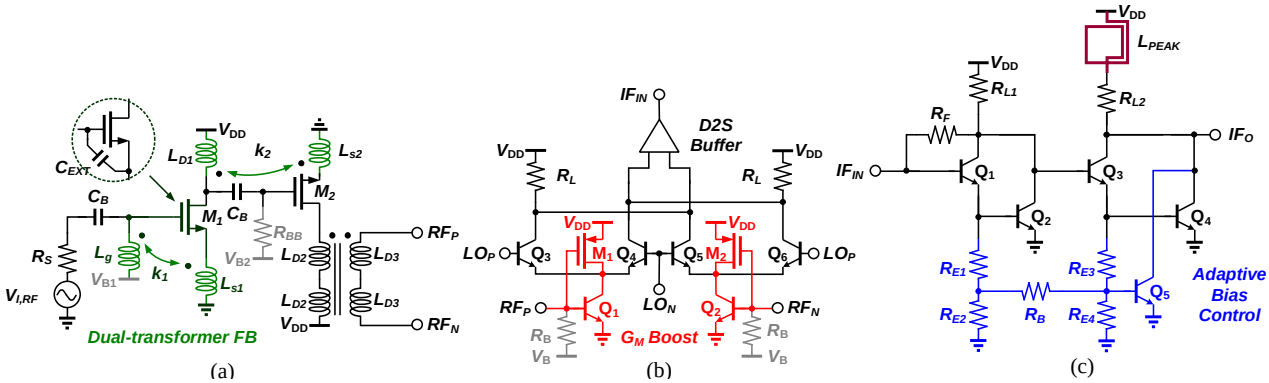

Fig. 2. (a) LNA with dual transformer feedback, (b) G_M-boosted mixer, (c) IF amplifier with adaptive bias and 3D inductor (L_{PEAK}).

The input admittance and effective G_M can be expressed as follows [6]:

$$Y_{in} = \frac{1+nk}{j\omega L_g(1-k^2)} + \left(\frac{C_{EXT}}{G_M L_{s1}}\right)\frac{(1+\frac{k}{n})^2}{(1-k^2)} \quad (1)$$

$$G_{M,eff} = g_m(1+\phi) \quad (2)$$

where n denotes the turn ratio n of $\sqrt{L_g/L_{s1}}$, ϕ represents the source and gate current feedback ratio, and k is the coupling factor. Note that MOSFETs are chosen for LNA design even with a lower transconductance than the BJTs. The main consideration is a relatively low bias current required but with comparable *NF* performance. In order to minimize the *NF* and additional noise contributed from the following stage, the 2nd stage of the LNA also adopts a transformer-based inductive source degeneration to achieve noise matching. The coupling with the peaking inductor of 1st stage can further enhance the circuit bandwidth and also reduce the chip area. The balun at the output of LNA converts the RF signal to a differential form.

The circuit topology of the double-balanced mixer is shown in Fig. 2(b), aiming for better port-to-port isolation and linearity with a high gain and low *NF*. As shown in the figure, $Q_{1\text{-}2}$ and $M_{1\text{-}2}$ are the inverter-type G_M stage to convert the RF input voltage to its current form, where the BJTs are chosen owing to the much higher transconductance than MOSFETs. Compared with the conventional common-emitter topology, the inverter-type G_M stage exhibits higher power gain and linearity with less noise. The $Q_{3\text{-}6}$ with resistive load R_L act as the mixing stage which converts the RF signal to the IF with a wide bandwidth.

The proposed IF amplifier is consist of cascaded feedback Darlington cell amplifier, as shown in Fig. 2(c). The Darlington amplifier is well-known to provide high gain and high linearity. However, the bandwidth is rather limited compared with a simple common-emitter stage. To overcome this problem, a series peaking inductor L_{PEAK} is used for enhancing the gain flatness at high frequencies in a wide IF bandwidth. Also, a local feedback resistor R_F is employed to further improve the signal bandwidth of the 1st stage pre-amplifier. It should be highlighted that $R_{E1\text{-}4}$ and R_B are the

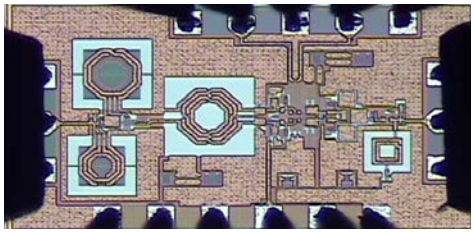

Fig. 3. Photograph of the proposed down-converter circuit.

proposed adaptive-control circuits to improve the linearity of IF amplifier. Via the resistive feedback network, the base voltage of Q_5 is proportional to the input power, and thus that of Q_4 (V_{BE4}) also increases with P_{in}, resulting in higher collector currents (I_{C4} and I_{C5}) for enhanced linearity. Note that Q_5 is initially biased at class-AB with a lower quiescent current for high efficiency at low output power level. The L_{PEAK} is a peaking inductor which is designed in a 3-D structure, consisting of 6 metal layers to obtain large inductance with a very small area (90×90 μm^2). With rigorous EM simulations, the extracted parameters show a self-inductance of 2.5 nH and a quality factor of about 2 at 2 GHz. With the 3-D inductor, the output P_{1dB} and signal bandwidth can be improved by about 4 dB and 400MHz without consuming extra DC power.

III. Measured Results and Discussion

The down-converter circuit of the receiver was implemented with the standard TSMC 1P6M 0.18-μm BiCMOS process. The chip photograph is shown in Fig. 3 with a total chip size of 0.4 mm^2, including the RF and dc bias pads (core area of only 0.24 mm^2). The LNA consumes 9 mA under a 1.8 V supply voltage, and the overall receiver front-end consumes 30 mA resulting in a total power consumption of 80 mW.

Fig. 4 shows both the simulated and measured RF input return loss of the down-converter. As can see, the input is well matched, where S_{11} is smaller than -10 dB over the entire RF-band from 18.2 to 21.4 GHz. Fig. 5 shows the measured noise figure, ranging from 5.25 to 6.25 dB in the desired IF range. Fig. 6 presents the average conversion gain and output P_{1dB}

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

	Technology (f_T GHz)	Supported Band (GHz)	Gain (dB)	NF (dB)	S_{11} (dB)	OP_{1dB} (dBm)	OIP_3 (dBm)	P_{DC} (mW)	Area (mm^2)
[3]	SiGe 0.18μm (70)	24-31	21/18	8/9.5	<-12	> -6[(a)]	3/1	60	0.7
[4]	SiGe 0.25μm (130)	19.2-22.2	25	8[(b)]	<-10	> -5	>2.5	188/360[(c)]	N.A.
[5]	SiGe 0.13μm (200)	31-33.4	17[(d)]	8.9	<-12	> -8	>2	5.8[(e)]/35.5	0.26[(e)]/1
[7]	CMOS 0.18μm (50)	20-30	18.7[(d)]	7.1-14.2	<-17.6	>2[(a)]	>11.1	5.2	0.67
[8]	CMOS 0.18μm (50)	21-29	23.7±1.4	4.1-5.1	<-8.8	> -4	> 6.1	40	1.33
This work	SiGe 0.18μm (70)	18.2-21.4	47.5±1.5	5.25-6.25	<-10	> 4.2	> 14	80	0.24[(e)]/0.4

(a): estimated from OIP_3. (b): single-sideband NF. (c): including PLL. (d): without IF amplifier. (e): core only.

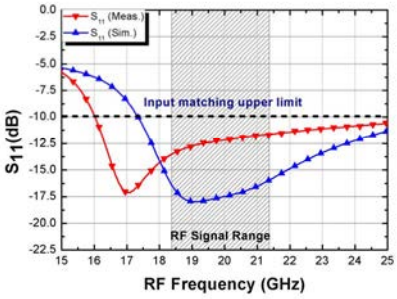

Fig. 4. Measured and simulated S_{11} of the down-converter.

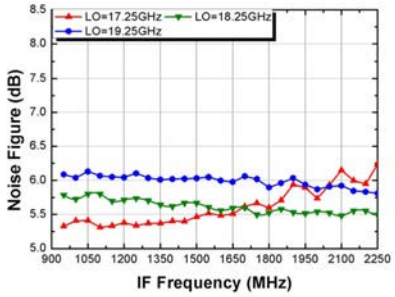

Fig. 5. Measured *NF* versus IF frequency at three LO frequencies.

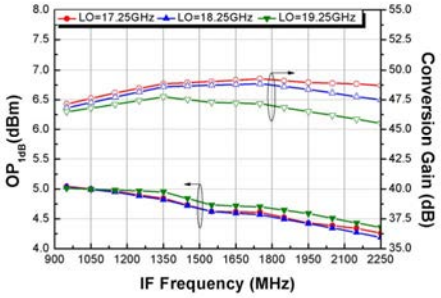

Fig. 6. Measured conversion gain and output P_{1dB} versus IF frequency at three LO frequencies.

versus IF frequency under an LO power of 5 dBm. The obtained conversion gain is around 47.5 dB with gain flatness within ±1.5 dB and an output P_{1dB} above 4.2 dBm. The measured performance and the comparison with the previously published results are summarized in Table I. The proposed down-converter shows excellent power gain and high linearity, while maintaining a low noise figure with a very compact chip area by a low cost 0.18-μm BiCMOS technology.

IV. CONCLUSION

A monolithic Ka-band down-converter with a low *NF* and excellent power gain and high linearity has been successfully demonstrated. We proposed several design techniques including a dual-transformer-feedback LNA, a G_M-boosted mixer, and IF amplifier with adaptive-bias control and 3D inductor to obtain the desired circuit specifications using a low cost 0.18-μm SiGe BiCMOS technology. The receiver front-end achieved a high conversion gain of 47.5 dB (gain flatness ± 1.5 dB), a linearity above 4.2 dBm, and an *NF* below 6.25 dB with a smallest chip area (0.24 mm^2) compared with previous reported results. The proposed down-converter design is suitable to be used in high data rate satellite communication systems for various emerging applications.

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