A Fully Integrated Ku-Band Down-Converter Front-End For DBS Receivers

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Abstract **— A fully integrated Ku-band down-converter front-end for digital broadcast satellite (DBS) receiver in a 0.18 μm SiGe BiCMOS technology is presented. To meet the specifications in different areas, the circuit can cover a wide RF range (10.7-13.45 GHz) with four LO frequencies, and down convert the RF signal to L-Band (950-2150 MHz). Compared with previous works, the presented down-converter using a low cost technology to achieve a low noise figure (< 6 dB), high gain (> 51 dB), and high linearity (OP_{1dB} > 5.5 dBm) under low power consumption (32 mA; 135 mW) with an excellent gain flatness (±1 dB) and a very small chip area (0.6 mm^2). This is also the first report of the DBS down-converter covering four different LO frequencies, to the best of our knowledge.**

Index Terms **—BiCMOS, DBS, down-converter, Ku-Band, receivers, LNB.**

I. INTRODUCTION

Digital broadcasting via satellite is rapidly expanding globally, which can deliver video to users and also provides high speed internet access. Among different digital broadcasting satellite (DBS) regulations, the RF operation in Ku-band, generally in 10.7−12.75 GHz (LO= 9.75 GHz for high band and 10.6 GHz for low band), for television broadcasting attracts much attention due to its great commercial value. In a DBS receiver, the low-noise block (LNB) down-converter plays a critical role in determining the signal quality [1]. Considering harsh weather conditions and losses of the antenna cable, an LNB usually has to guarantee a noise figure (NF) lower than 0.6 dB and provide a power gain up to 60 dB. Many existing LNBs are realized using discrete components with expensive III-V technology and a relatively low integration level to achieve the required system performance [2]. Note that two or three cascaded GaAs pHEMT amplifiers are typically placed in front of the down-converter to achieve such a low NF and high gain.

In this paper, a fully integrated LNB down-converter for DBS applications is presented, which consists of a low-noise amplifier (LNA), a mixer, and an IF amplifier, as shown in Fig. 1. Good results of integrated Ku-band down-converters using silicon-based technologies have been reported previously [2]-[5]. However, achieving low NF and high gain simultaneously under low power consumption with a small chip area still remain challenging. Also, obtaining small gain variation and high linearity in the required bandwidth are rather difficult. In this work, a high performance fully integrated Ku-band down-converter is demonstrated using a low cost 0.18-μm silicon bipolar technology. The proposed circuit allows wide band operation (from 10.7-13.45 GHz with four different LO frequencies) with excellent gain flatness under small power consumption. Also, only four inductive components are employed in our design to minimize the chip area. The high gain and low noise characteristics help to relax the requirement from discrete pHEMT amplifiers and reduce the system costs.

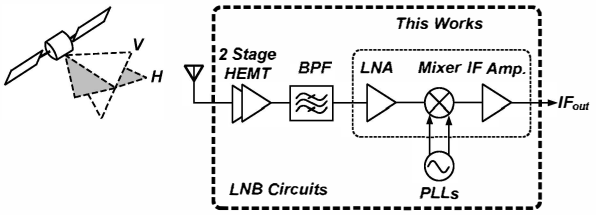

Fig. 1. System block of a Ku-band DBS down-converter.

II. DOWN-CONVER DESIGN

A two-stage single-ended LNA is employed in this design. The first stage LNA is optimized for noise performance with moderate power gain and the second stage is designed for high power gain. A passive balun is used as the load of the second stage of LNA for inductor peaking and also converts the signal to differential. The mixer stage is implemented in a double-balanced active configuration for better port-to-port isolation and high linearity. An active balun with folded-cascode topology converts the signal back to single-ended for the IF amplifier. The final stage is a two-stage self-biased IF amplifier with a 3D inductor as the load to achieve a high linearity and high power gain with a small chip area.

A. Design of Low-Noise Amplifier

The key to realize a low noise figure while maintain a high gain is to ensure simultaneous input and noise matching. A conventional common-emitter (CE) amplifier with inductive degeneration was typically used in previous reported Ku-band down-converter for LNA design [2]-[5]. However, this topology exhibits a limited bandwidth for both gain and NF. In this design, the reactive transformer feedback technique is used, which offer advantages of improved gain, stability and particularly the noise and power matching capability for LNA in a wide frequency range [6]. The proposed two-stage LNA with a single-ended input and differential output is shown in Fig. 2(a). The primary coil in the transformer is connected in parallel to the base of Q_1, and the secondary coil is connected in series to the emitter to form negative feedback (k ~ 0.55). The second stage is realized with the cascode configuration with

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a transformer- -based passive balun to maximize the power gain by inductive peaking and also convert the LNA output from single-ended to differential. In this design, the transformer balun has a smaller than 2° and 0.5 dB phase and magnitude errors, respectively in the entire band. The LNA is biased at only 3.5-mA DC current with a power gain exceeding 25 dB.

B. Design of Double-Balanced Mixer

Fig. 2(b) shows the proposed active double-balanced

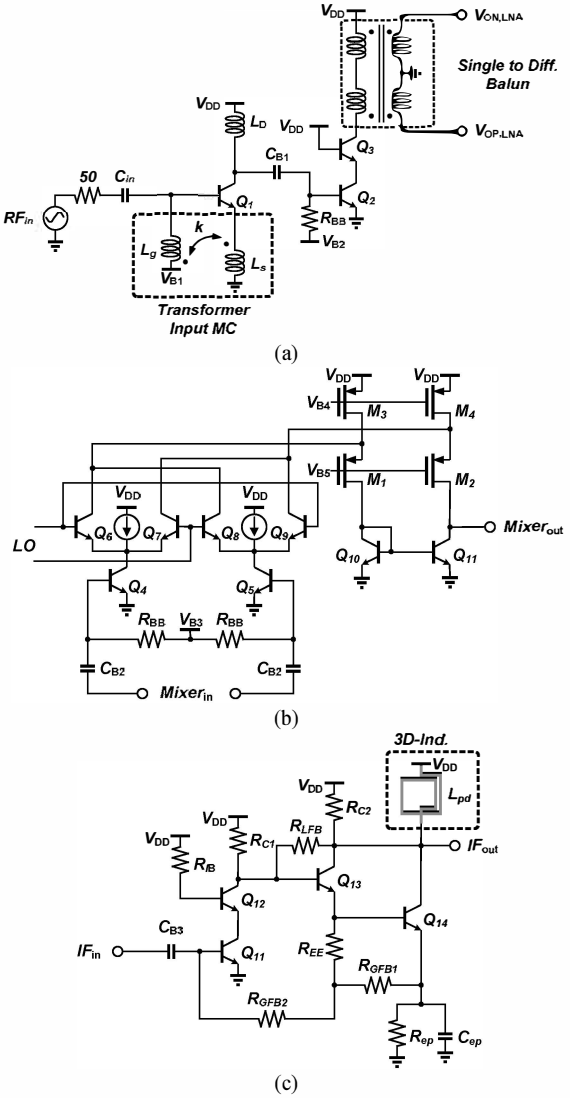

Fig. 2. Three circuit blocks in the proposed DBS down-converter. (a) low-noise amplifier, (b) mixer with active load, and (c) IF amplifier.

mixer with good linearity and port-to-port isolation. The RF input transistors $Q_{4\text{-}5}$ act as the transconductance stage to convert the signal to a current form, and $Q_{6\text{-}9}$ function as the switching stage. The current bleeding techniques are used to improve conversion gain and reduced the NF. To improve the conversion gain, the folded-cascode topology is employed, which also converts the differential signal to single-ended for the IF amplifier. The mixer is designed with a moderate gain of about 5 dB with a DC bias current of 5 mA and the current drawn by current bleeding is about 1mA.

C. IF Amplifier

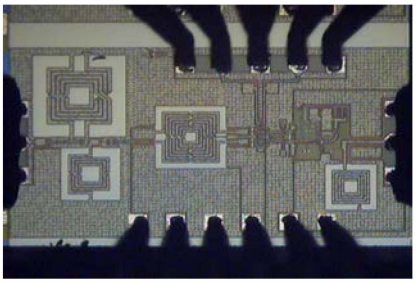

Fig. 3. Chip micrograph of the down-converter front-end.

The proposed two-stage IF amplifier is shown in Fig. 2(c). The cascode topology ($Q_{11\text{-}12}$) is used in the first stage to increase the gain over the IF band. The second stage ($Q_{13\text{-}14}$) is constructed by the Darlington pair with local feedback R_{LFB} and shunt peaking L_{pd} to improve the output P_{1dB} and the signal bandwidth. The global feedback (R_{GFB2}) from the emitter degeneration resistor (R_{EE}) to the base of Q_{11} can reduce the IF amplifier input impedance and match to the mixer output. The capacitor C_{ep} creates a zero to enhance the high frequency gain. Note that L_{pd} is designed by a 3D inductor using six metal layers to obtain a large inductance in a compact chip area. The relatively small quality factor is suitable for broadband design, and the normally needed external RF chokes for the IF amplifier can be removed. Based on EM simulation, a large inductance of 29 nH can be obtained with a quality factor ~ 2 in a dimension of only 90×90 μm^2, and the self-resonant frequency is ~ 5 GHz. With the 3D inductor, the bandwidth and output P_{1dB} can be improved by about 500 MHz and 4 dBm. The measured IF amplifier exhibits a power gain up to 21 dB and OP_{1dB} of +5.5 dBm. The IF amplifier is biased at a total DC current of 20 mA.

III. Measurement Results

The down-converter front-end was implemented in the standard TSMC 1P6M 0.18-μm BiCMOS process. This technology provides devices for RF mixed-signal designs, including the NPN HBT with 70/90 GHz f_T/f_{max}, and 0.18-μm CMOS. The chip micrograph is shown in Fig. 3 with the die size of 1060×570 μm^2 (core area: 960×450 μm^2). The LNA consumes 3.5 mA from a 1.8 V supply voltage and the down-converter consumes 32 mA with the total power consumption of 135 mW.

Fig. 4 shows the RF input return loss of the down-converter. The input is well-matched to achieve smaller than -10 dB over the entire RF band (10.7-13.45 GHz). Fig. 5 shows the measured noise characteristic of the down-converter front-end, which is between 5 to 5.8 dB in the range of 950-2150 MHz IF frequency. The measured

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

	Technology (f_T GHz)	Supported Band (GHz)	Gain (dB)	NF (dB)	S_{11} (dB)	OP_{1dB} (dBm)	OIP_3 (dBm)	P_{DC} (mW)	Area (mm^2)
[2]	SiGe 0.80μm (46)	10.7-12.8	38±7	7	<-10	> 5	16	540[(b)]	N.A.
[4]	SiGe 0.25μm (110)	10.7-12.8	43±1	6-7	<-10	7	16	130/260[(c)]	1[(d)]
[7]	SiGe 0.13μm (200)	8-18	56[(a)]	6.7-7.8	<-8.5	>-10	N.A.	180	1.81
This work	SiGe 0.18μm (70)	10.7-13.5	51±1	5-5.8	<-10	> 5.5	> 18	135	0.60[(e)]

(a): include variable-gain amplifier. (b): include PLL. (c): include PLL (d) include PLL but need external RF chocks. (e): core area only 0.43 mm^2.

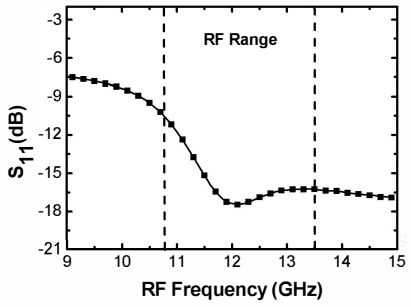

Fig. 4. Measured S_{11} of the down–converter front-end.

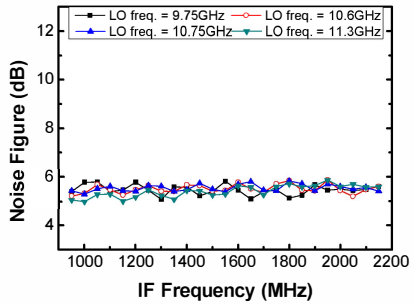

Fig. 5. Measured NF versus IF frequency at four different LO frequencies.

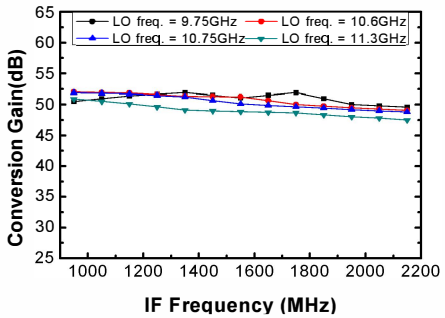

Fig. 6. Measured CG versus IF frequency at four different LO frequencies.

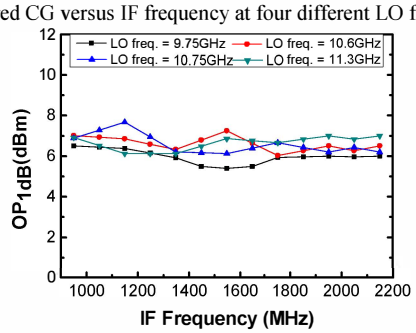

Fig. 7. Measured OP_{1dB} versus IF frequency at four different LO frequencies.

conversion gain is averaged at about 51 dB with a gain flatness within ± 1dB (for the first three LO frequencies of 9.75, 10.6, and 10.75 GHz), as shown in Fig. 6. The measured average OP_{1dB} is above 5.5 dBm in the entire band, as shown in Fig. 7. The measured performance and comparison with previous works are summarized in Table I. Using a low-cost technology with a relatively low f_T, the proposed down-converter achieves low NF and high gain in a wide frequency range under a low power consumption with excellent gain flatness and a very small chip area.

IV. CONCLUSION

A fully integrated Ku-band down-converter front-end was demonstrated in a low cost 0.18-μm silicon bipolar technology. With a compact chip area (core area only 0.43 mm^2), the presented design achieved a high gain of 51 dB, low NF of 5-5.8 dB, and high linearity of above 5.5 dBm under low power consumption of 135 mW. Integration of the down-converter with a low phase noise PLL is in progress. The proposed down-converter provides a low cost and low power solution to the Ku-band DBS applications for various standards.

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