A V-Band Low-Noise Amplifier with 5.3-dB NF and Over 8-kV ESD Protection in 65-nm RF CMOS

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***Abstract*—This paper presents an ESD-protected V-band (f_0 at 58 GHz) low-noise amplifier (LNA) in 65-nm CMOS. Instead of using the conventional diode-based RF ESD design, a high current capability spiral inductor and a high breakdown MOM capacitor are employed as effective bi-directional ESD protection network, and also as part of the input matching by the co-design approach. The measured results demonstrate an over 8-kV HBM ESD protection level with a *NF* of 5.3 dB and a power gain of 17.5 dB at 58 GHz, under a power consumption of 18 mW. To our best knowledge, this LNA presents a highest ESD protection level and a lowest *NF*, compared with prior arts in a similar frequency range.**

***Index Terms*— CMOS, electrostatic discharge (ESD), low-noise amplifier (LNA), and millimeter wave (mm-Wave).**

I. INTRODUCTION

The millimeter-wave wireless communication at around 60 GHz has attracted tremendous interests in both academia and industries recently, which permits a compact system size and high data transmission rate up to multi-Gb/s [1]-[3]. Owing to the rapid progress in technology, CMOS shows the capability of high f_T and f_{max} under low power operation, and becomes the most suitable candidate for realizing a fully-integrated 60 GHz transceiver. However, the reduced gate oxide thickness and hence lowered gate oxide breakdown voltage make the device more vulnerable to electrostatic discharge (ESD) [4]. Also, the large chip size for SOC with accumulated charges in the substrate also increases the susceptibility of the circuits to ESD for volume production [5]. Moreover, the ESD protection level is in general proportional to the capacitive parasitics if using the conventional ESD devices such as diodes and silicon-controlled rectifier (SCR) [6]-[8]. These pose a significant challenge of designing robust on-chip ESD protection for a 60 GHz transceiver in advance CMOS technology.

In this paper, we propose of using an *LC* high-pass network (low-pass for ESD current) co-designed with the entire input matching network to realize a robust ESD network up to 8 kV while maintaining a very low noise of only 5.3 dB for a 60 GHz LNA in 65-nm CMOS. The grounded shunt inductor L_{ESD} provides a direct current path to bypass the ESD current and the series capacitor C_{ESD} offers a robust current block to protect the core circuit. Together with a power clamp connected from V_{DD} to V_{SS}, an ESD network which provides two bi-directional current paths (total four paths) is completed. Compared with the LNAs using the inductor-based ESD devices [1], [9], [10], the inductor L_{ESD} here is neither for RF choke [1] to make the ESD diode invisible at RF frequencies nor for resonating out the diode or pad parasitic capacitances [9], [10]. As a result, a relatively small L_{ESD} is allowed (only ~ 60 pH) in this design, which reduces the chip area and also shortens the ESD current signal path to improve the protection level. Also, the co-design approach using both L_{ESD} and C_{ESD} as a part of the input matching greatly relaxes the design tradeoff between the RF performance and ESD protection level in the conventional plug and play approach. The additional matching network element also makes the optimization among noise, gain, and power consumption easier. By co-optimization of ESD protection and RF characteristics, the proposed V-band LNA demonstrates a *NF* of 5.3 dB, a power gain of 17.5 dB, and an ESD level of over 8 kV under a power consumption of 18 mW in 65-nm CMOS.

II. CIRCUIT TOPOLOGY

Fig. 1 shows the circuit configuration of the proposed LNA with the complete ESD protection network. The LNA employs a two-stage cascode topology. With the reduced Miller effect, the cascode topology has higher power gain and improved input/output isolation compared with the simple common-source topology. The inductive source degeneration (L_S) is used in the first stage for simultaneous noise and power matching, together with L_{G1}, C_{ESD}, and L_{ESD} forming the input matching network. Also, the inductive loads (L_{D1} and L_{D2}) are used for gain peaking in both stages. The capacitor C_{12} serves as the DC block between the two stages, also works together with L_{G2} and L_{D1} as the inter-stage matching. The inductor L_{D2} and capacitor C_{D2} are also utilized as the output matching network to 50 ohm for measurement. The transistor size is determined by investigating the noise and gain characteristics as a function of finger width and bias. With the excellent scalability of MOS transistors, the current density for best device performance is similar for a wide variety of transistor sizes [11], which is about 0.2 mA/μm (under V_G of ~ 0.7 V) in the employed 65 nm CMOS technology. With this guideline and also the low-power design consideration, the second

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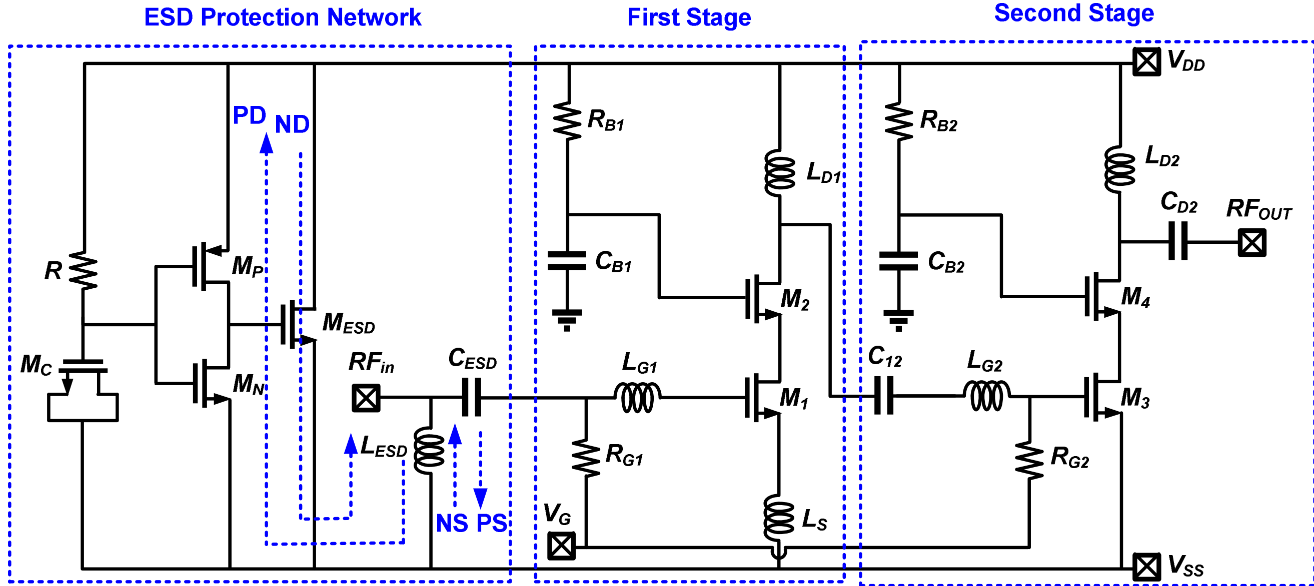

Fig. 1. Schematic of the proposed LNA consisting of the spiral inductor L_{ESD}, MOM capacitor C_{ESD}, and a power clamp for ESD protection.

cascode stage also use the same transistor size.

The ESD protection network includes a shunt inductor L_{ESD} and a series capacitor C_{ESD}, and a power clamp, as shown in Fig. 1. As a part of the matching network, the high-pass L_{ESD}-C_{ESD} network acts like typical passive elements under normal RF operation. However, it becomes a low-pass network to the ground for the ESD current with relatively low frequencies. During ESD zapping, L_{ESD} provides a low-impedance bi-direction path to bypass the discharge current, and C_{ESD} further blocks ESD current to protect the core circuit. It is critical that the L_{ESD} and C_{ESD} must be able to sustain high current and voltage during ESD zapping. In this design, a half-turn spiral inductor with a width of 10 µm is adopted, which uses the top metal layer with a thickness of 3.4 µm to enhance the current handling capability. Also, the metal-oxide-metal (MOM) capacitor with a breakdown voltage up to 75 V is used to realize C_{ESD}. As a part of the matching network, determination of L_{ESD} and C_{ESD} are co-designed with L_{G1} and L_{S} in the early RF design stage for noise and gain optimization. This approach permits using relatively small L_{ESD} and C_{ESD}, and the reduced parasitics leads to an excellent noise performance of the LNA.

The power clamp consisting of M_{C}, M_{P}, M_{N}, and R with a linear characteristic is employed. Switching of the inverter (M_{P} and M_{N}) during the ESD zap is controlled by the RC time delay of the MOS capacitor M_{C} and P-type poly resistor R to ensure the large ESD transistor M_{ESD} functions correctly. It is worth mentioning that the ESD protection limitation in this design should be the power clamp instead of L_{ESD} and C_{ESD}, differing from the typical diode- or SCR-based RF ESD design [6]-[8], [12]. With a large enough width and short enough length, the IR drop across of L_{ESD} is very low. Also, the robust MOM capacitor C_{ESD} has a much higher breakdown voltage than the gate oxide. Consequently, the power clamp will be damaged by the discharge current before L_{ESD} and C_{ESD}. Since the L_{ESD} and C_{ESD} are not the bottleneck of the ESD level, the co-design procedure becomes relatively straightforward, compared with the previous work using co-design approach but with diode- or SCR-based ESD devices in which the ESD level is the main consideration when choosing the ESD devices [6]-[8], [12]-[15]. In the proposed approach, the designer can mainly focus on the optimization of gain and noise instead of the ESD protection level when selecting L_{ESD} and C_{ESD}.

III. Results and Discussion

The proposed ESD-protected LNA was fabricated in a 65-nm CMOS process. The on-wafer measurements were performed for both RF and ESD characteristics. Fig. 2 shows the measured *S*-parameters and *NF* of the LNA under a 1.5 V supply with an associated total current of 12 mA. The LNA achieves a peak gain of 17.5 dB, a *NF* of 5.3 dB, and the input and output return losses are greater than 15 and 10 dB, respectively at 58 GHz. The *S*-parameters and *NF*s were also measured before and after ESD zap. The almost identical results verify that the ESD current has been successfully bypassed via L_{ESD} to the ground or V_{DD} without damaging the core circuit.

Fig. 3 shows the transmission line pulse (TLP) testing results for the LNA. The results present a second breakdown current It_2 over 7 A, corresponding to an ESD level over 10.5 kV ($V_{\mathrm{HBM}} \sim It_2 \cdot 1.5\ \mathrm{k}\Omega$) for PD and ND modes. Note that in the PS and NS modes, the ESD network behaves like a short circuit due to L_{ESD} and the TLP current is conducted to the ground directly. Since the leakage current cannot be monitored across L_{ESD}, the ESD protection level is verified together with the RF characteristics before and after ESD zapping. The results show that the ESD level is above 8 kV (limited by the equipment HANWA-W5100) for both the PS and NS modes.

Table I compares this work with recently published mm-wave ESD-protected LNAs. The proposed LNA achieves a low *NF* of only 5.3 dB under a power consumption of only 18 mW, and demonstrates an ESD protection level over 8 kV, which is the highest compared with prior arts.

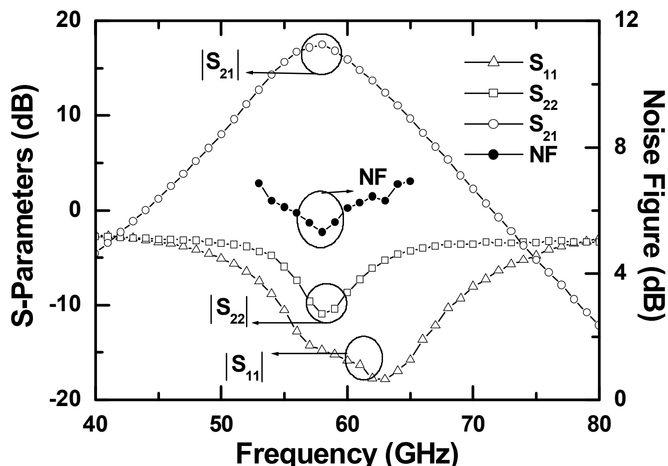

Fig. 2. Measured S_{11}, S_{21}, S_{22}, and *NF* of the ESD-protected LNA.

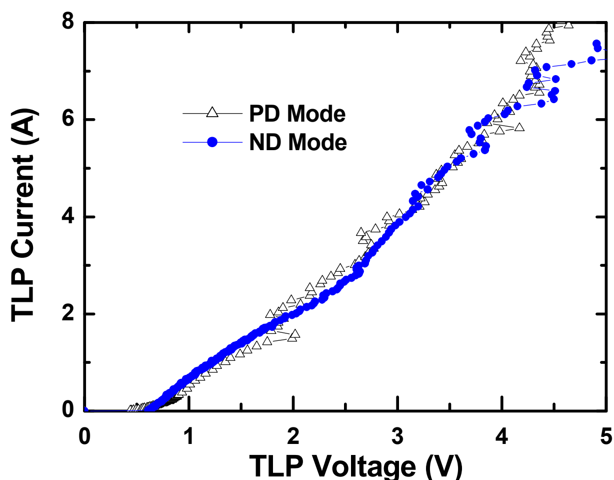

Fig. 3. Measured TLP *I-V* curves of the ESD-protected LNA.

IV. CONCLUSION

In this paper, we demonstrated a V-band LNA (f_0= 58 GHz) with an excellent ESD protection level over 8 kV in 65 nm CMOS. By the ESD/matching co-design approach, the grounded L_{ESD} with high current capability and series C_{ESD} with a high breakdown voltage were incorporated into the matching network and optimized for noise and gain simultaneously. The proposed LNA achieved a noise figure of 5.3 dB and a power gain of 17.5 dB, under a power consumption of only 18 mW.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED LNAS WITH PRIOR ARTS

Ref.	This Work	[1]	[9]
Tech. (nm)	65	130	65
Freq. (GHz)	58	60	77
NF (dB)	5.3	8.6	7.8
Power (mW)	18	65	37
S_{21} (dB)	17.5	20.4	10.5
S_{11} (dB)	-15	-15	< -10
HBM (kV)	> 8	6.5/1.5	4.05
Area (mm^2)	0.51	0.715	0.414

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