High Speed and Low Power Silicon-Based Receiver Front-end for Optical Interconnect

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***ABSTRACT* — We demonstrate an optical receiver front-end using a CMOS TIA with a germanium-on-silicon PD. The amplifier only occupies 0.09 mm^2 with 12 mW power consumption, and achieves a 27.5 GHz 3-dB bandwidth. The integrated silicon-based receiver shows well opened eye diagrams up to 20 Gb/s.**

***Index Terms* — Transimpedance amplifier (TIA), optical interconnect (OI), CMOS, Ge-on-Si PD, receiver front-end.**

I. Introduction

The excessively increased amount of data transmission requires very high speed networks for data communication. Using optical interconnect (OI) has attracted much attention recently from both industry and academia [1]. Compared with the conventional electrical interconnect, OI promises a wider bandwidth, less power consumption, smaller delay, and the immunity from electromagnetic interference. For high speed applications, the electrical front-end circuits are critical and often a bottleneck to limit the overall data rate [2]-[5].

One straightforward approach for improving the bit rate for optical communication is the multi-channel configuration. The operating speed for each channel can thus be relaxed, while still achieving an overall high data rate. However, the cost, area, and power consumption of each channel become even more critical than the single channel design. Compared with the III-V based design for the optical receiver front-end, the CMOS technology allows low power operation with high integration level of other circuit blocks. Also, the Si-based solution including CMOS and germanium-on-silicon photo detector (PD) has the advantage of low cost and the potential for a fully integrated OI receiver. Such photo detectors are well suited to the silicon photonic platform given their compatibility with CMOS processing and performances which have demonstrated responsivities around 0.8A/W and data rates of 40 Gb/s at 1.55 μm [6].

In this paper, the transimpedance amplifier (TIA), which is one of the most critical circuit blocks in the optical receiver front-end is realized by 90 nm CMOS. The germanium-on-silicon PD is used to combine with the TIA to demonstrate a complete silicon-based optical receiver front-end. With the proposed design technique of inverter type input stage with T-coil transformer peaking, the TIA has a very compact area with the power consumption among the lowest compared with other published results. The integrated germanium-on-silicon PD and CMOS TIA also demonstrate well opened eye diagrams with high speed operation.

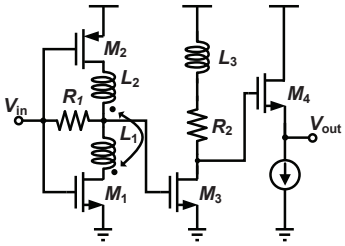


Fig 1. Circuit schematic of the proposed low power transimpedance amplifier (TIA) with transformer peaking.

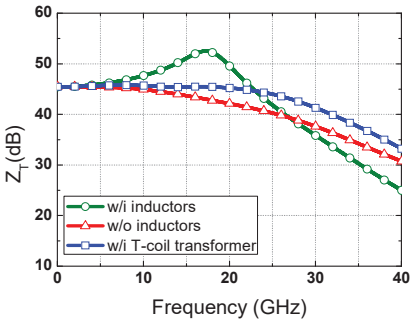


Fig 2. Simulated transimpedance gain with different TIA designs. The proposed T-coil transformer shows the widest bandwidth and the best gain flatness.

II. Design of Transimpedance Amplifier

Fig. 1 shows the circuit schematic of the proposed TIA, where the first stage is an inverter (M_1, M_2) with resistive feedback R_1 and two coupled inductors (L_1, L_2) for transformer peaking. Also, a post amplifier (M_3, L_3, R_2) is used to further increase the overall gain of the TIA, followed by a voltage buffer stage (M_4) for the 50-Ω measurement environment. Compared with the typically used regulated cascode (RGC) configuration [2] as the input stage of TIA, we propose a new topology using an inverter type voltage amplifier combined with T-coil transformer peaking, which allows low power operation while maintaining a wide bandwidth.

The inverter-type amplifier is an excellent choice for achieving wide bandwidth with low power, since it provides a large transconductance from both NMOS and PMOS ($g_{m,n}$+$g_{m,p}$). However, a second dominant pole due to the parasitic capacitances of the transistors could exist close to the first pole (originated from Z_{IN} of TIA and parasitic capacitance of PD) in the inverter type shunt-shunt feedback voltage amplifier, which becomes the bottleneck of the operating speed in this topology. By introducing inductive

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PUBLISHED WORKS

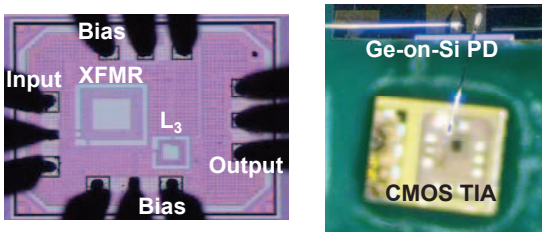
Ref.	[3]	[4]	[5]	This
Process	180 nm CMOS	90 nm CMOS	65 nm CMOS	90 nm CMOS
V_{DD} (V)	1.8	1	1.6	1.5
Z_T (dBΩ)	51	78.3	55	50
Date Rate (Gb/s)	40	25	40	40
IRNC (pA/√Hz)	55.7	32.2	--	20
DC Power (mW)	60.1	44.4	107	12
Core Area (mm^2)	0.5	0.1	0.5	0.09

components in the circuit, the parasitic capacitances can be resonated by the inductance to extend the bandwidth and enhance the gain. By properly design the transformer, the zero and poles are placed at the desired frequencies for broadening the bandwidth. The simulated transimpedance gain Z_T of the TIA with and without the peaking transformer is shown in Fig. 2. The proposed TIA reaches more than 55% bandwidth improvement than the one without any peaking technique, and 20% more than that with non-coupled inductor peaking (with individual L_1 and L_2). It should be emphasized that the transformer design with combined inductors in the layout can also significantly reduce the chip area.

III. PHOTO DIODE AND INTEGRATION

Fig. 3(a) shows the chip micrograph of the proposed TIA in 90 nm CMOS, which occupies a core area of only 0.09 mm^2. Fig. 3(b) is the photo of the integrated silicon-based receiver front-end with the PD using bond wires. The germanium-on-silicon photo diode was fabricated at CEA-Leti through the ePIXfab program and consists of a germanium detection region which is butt-coupled on-chip to a silicon waveguide. The maximum data rate from our particular design is around 25 Gb/s. Fig. 4 compares the simulated and measured Z_T of the proposed TIA under bias of 12 mW. An excellent agreement between the simulated and measured gain (~ 50 dBΩ) can be observed. The slightly reduced bandwidth (29.1 GHz vs. 27.5 GHz) may be attributed to the parasitic effects in the actual layout not included in the simulation. Also, the measured group delay is ~ 20 ± 10 ps, which also agrees well with the simulated result. Fig. 5(a) and 5(b) show the measured eye diagrams at 10 Gb/s and 20 Gb/s, respectively. Note that the TIA is capable of 40 Gb/s operation with a 3-dB bandwidth up to 27.5 GHz. Higher data rates in the eye diagram measurements would be possible with a faster photo diode. The parasitic effects introduced by the bond wires can also limit the data rate achieve once integrated, which can be improved by flip-chip bonding in the future.

Table I compares our TIA with other published results also using CMOS technology. Owing to the relatively simple circuit topology using the inverter input stage and the effectiveness of the transformer peaking technique with the inverter type input stage, the proposed design has a relatively smaller core chip area compared with other published results. Also, the power consumption is among the lowest.



(a) (b)

Fig. 3. (a) Chip micrograph of the proposed TIA (b) CMOS TIA integrated with the Ge-on-Si PD by bond wires.

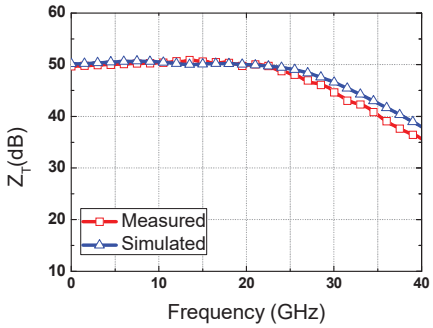
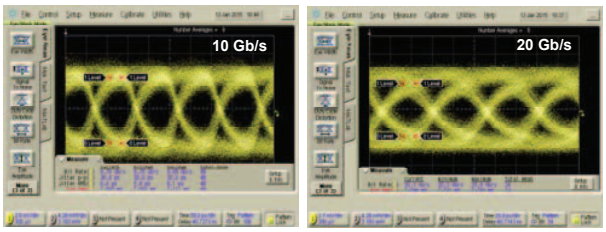


Fig. 4. Measured transimpedance gain Z_T of the proposed TIA under power consumption of 12 mW.



(a) (b)

Fig. 5. Measured eye diagrams for integrated TIA with Ge-on-Si PD at (a) 10 Gb/s and (b) 20 Gb/s respectively.

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