A High Efficiency Compact Class F GaN MMIC Power Amplifier for 5G Applications

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***Abstract* — A high performance compact MMIC class F power amplifier is demonstrated for 5G small cell applications by a 0.25-µm Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) technology. Both the 2nd and 3rd harmonic terminations are considered in the output matching network, and optimized utilizing the backside via parasitic inductance. Also, the device drain-source parasitic capacitance is considered together into the matching circuit for improving the bandwidth and high frequency operation. The measured peak output power P_{out} of the amplifier is 36.6 dBm at 6 GHz. Also, the measured peak power-added-efficiency (PAE) at a 1.5 dB gain compression is 65.8 %. Also, the measured 3-dB bandwidth is 1800 MHz. The design has a chip size of only 2.56 mm^2.**

***Keywords* — Gallium Nitride (GaN), MMIC, class F, power amplifier, PAE, 5G communications.**

I. INTRODUCTION

Efficiency of a power amplifier (PA) is a critical parameter for 5G transmitter operation, which is the most power hungry block in the system front end. Also, the need for a compact PA design becomes a significant factor for the small cells in 5G applications. Another important design consideration is the bandwidth (BW). With an increased BW of the PA, more different wireless communication standards could be accommodated, which allows simplifying the transmitter design [1], [2]. With the superior material properties of GaN such as wide bandgap and high saturation velocity under a large electrical field, the GaN-based MMIC is an excellent candidate for the 5G applications [3], [4].

The class F power amplifier is a widely used topology for various such applications. Fig. 1 shows the basic concept of class F PA design [5], which can achieve a theoretical 100% efficiency by using a quarter-wave transmission line (*TL*) to short circuit the even harmonics and provide high impedance to the odd harmonics, and with the series *LC* network resonating at the fundamental tone for the output power. Different approaches have been proposed to realize high performance class F PAs [6]-[8]. However, challenges still remain such as the efficiency and chip size owning to the relatively complicated output network with high order harmonic terminations. In addition, the device parasitics could seriously degrade the PA performance if not considered properly, especially the large output capacitance of the power transistor. In this paper, a class F MMIC power amplifier is presented with both second and third harmonic terminations using a 0.25 μm GaN HEMT technology provided by WIN Semiconductor, aiming for 5G small cell applications. A high efficiency, high output power, and wide BW MMIC is demonstrated.

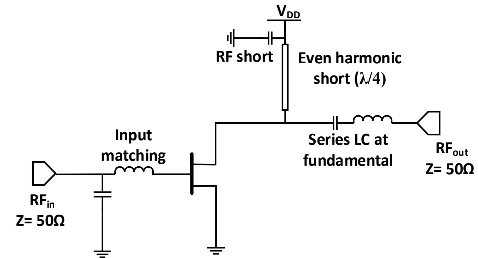

Fig. 1. A typical class F PA topology.

II. CIRCUIT DESIGN AND ANALYSIS

Fig. 2 shows the proposed class F power amplifier, including input/output matching network (IMN/OMN) for both fundamental tone and harmonics, stability network, and also the intrinsic device is highlighted. Note that C_{DS} is mainly contributed from the capacitance coupling between drain and source through the substrate, and L_D is introduced by the drain fingers and interconnect in the layout. The *TL* with different characteristic impedances together with the metal-insulator-metal (MIM) capacitors and the inductance of backside via L_{Bvia} are employed for the fundamental and harmonic matching/termination networks, and no spiral inductors are used. To achieve a proper class F operation, the device is biased at deep class AB. Also, the amplifier is optimized to achieve high output power and PAE simultaneously.

The IMN consists of two cascaded *L*-Type networks including a series transmission line TL_1 and a shunt short circuit stub TL_2, and also the MIM capacitors C_1 and C_2 form the other *L* network, which allows a wideband operation. The stability network in the proposed design consists of two sets of *RC* networks, namely, the R_{SP}-C_{SP} connected in parallel to the signal path and the R_{SS}-C_{SS} connected in series to the gate of transistor. We employ both types of stability networks to ensure the circuit stability.

It is critical to select the size of power cell for the targeted output power level of the proposed class F PA, which is about 4-5 W (36-37 dBm) in this design for 5G small cell applications. The adopted 0.25 μm GaN technology (WIN Semiconductors) is fabricated on a 4 mil (100 μm) thick SiC substrate with the nominal maximum drain current density and transconductance of 1040 mA/mm and 390 mS/mm,

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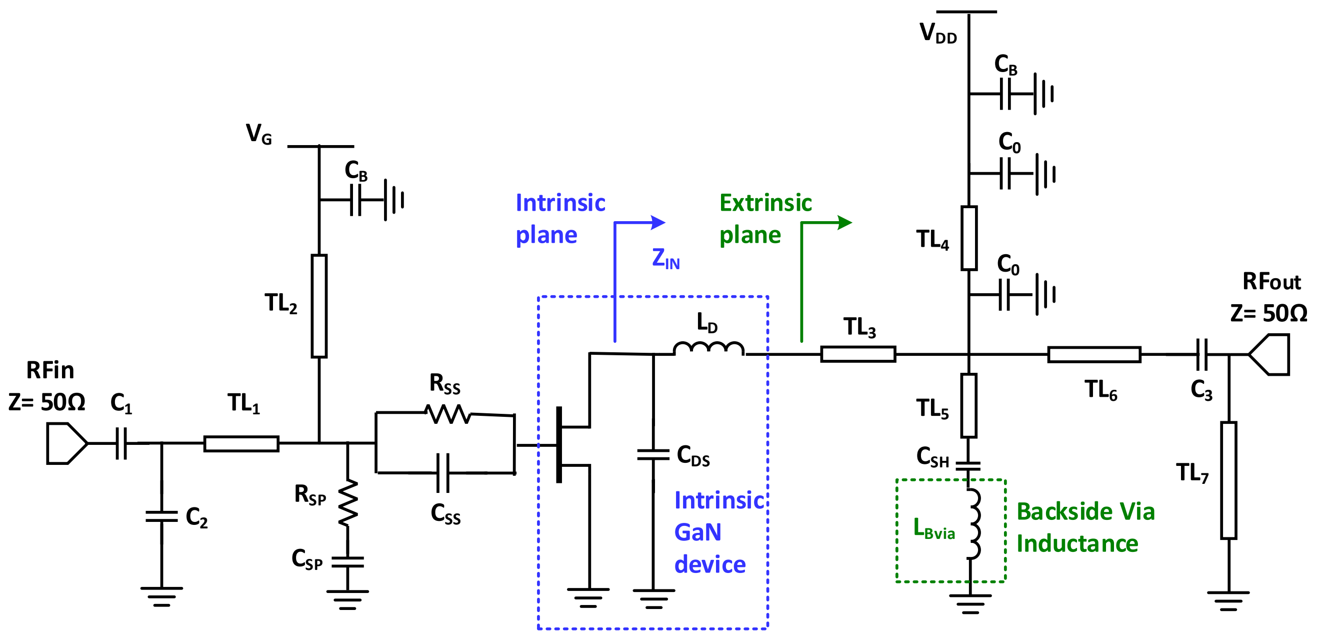

Fig. 2. Circuit topology of the proposed class F PA.

respectively. The suggested drain bias voltage is 28 V. The power cell selected in the amplifiers is 4×200 μm (4 fingers) with the corresponding f_T/f_{max} of ~ 30/70 GHz. The load-pull simulation under ~ 2.5 dB gain compression is performed to find the impedance point for simultaneously achieving high PAE and output power. Fig. 3(a) shows the simulated matching trajectories from 3 to 20 GHz based on the selected transistor size under the designed bias point at the device intrinsic and extrinsic planes respectively, as illustrated in Fig. 2. Note that the extrinsic plane is the output terminals of the transistor, where it interfaces with the output matching network. On the other hand, the intrinsic plane is a nonphysical plane separating the voltage-controlled current source in the equivalent circuit model from the device parasitics such as C_{DS} and L_D, as explained in [5]. As can be seen, the simulated optimal impedance points for the 2nd and 3rd harmonics are very close to short and open respectively when referred back at the device intrinsic plane, which is consistent with the theory prediction for achieving the optimal performance of class F PA. Fig. 3(b) shows the simulated waveforms of the amplifier using the harmonic terminations shown in Fig. 3(a) at the device intrinsic plane, where the overlap between voltage and current is minimized with harmonic terminations to achieve a high efficiency. It should be mentioned that we are allowed to access the device intrinsic plane of the transistor model to observe the waveform by collaboration with the foundry.

The output matching network can be roughly divided to two parts. The design of TL_6 to TL_7 with C_3 mainly considers the matching of the fundamental frequency. The rest elements are for the 2nd and 3rd harmonic terminations. Compared with the conventional class F topology as shown in Fig. 1, the quarter-wave transmission line is replaced by TL_4 with a relatively high characteristic impedance (~ 70 Ω) and two small shunt capacitors C_0 (~ 0.2 pF). The circuit size can be effectively reduced.

The second harmonic short is realized by the shunt branch TL_5, C_{SH}, and L_{Bvia}, where L_{Bvia} is obtained from the inductance of the backside via directly. Fig. 4 (a) shows the 3D plot of the standard backside via available in the adopted 0.25-µm GaN technology, which is surrounded by the SiC substrate with an oval shape (60 μm × 30 μm) and a height of 100 μm. The via is a hollow cylinder with a sidewall of ~ 4 μm gold. The full-wave EM simulation as shown in Fig. 4 (b) indicates that the backside via can provide a relatively small but stable inductance with a high quality factor over a broad frequency range, almost acting as a pure 3-dimensional inductor, which cannot be obtained by a typical microstrip line or spiral inductor. A wideband inductance L_{Bvia} of ~ 32 pH from 3 to 30 GHz can be obtained with the Q factor up to ~ 60 at 18 GHz. The L_{Bvia} is co-designed with TL_5 and C_{SH} for improved harmonic termination of the class F PA.

The third harmonic impedance optimization is achieved by the combination of LC shunt filter (TL_5, C_{SH}, and L_{Bvia}) and equivalent quarter wave line. We consider the output parasitic capacitance of power transistor C_{DS}, TL_3, and one of the C_0 as a π network. Combining with the equivalent quarter-wave line TL_4 and C_0, the two cascaded π network can achieve a wide bandwidth. It should be emphasized that the overall impedance Z_{IN} (see Fig. 2) looking towards the output port from the intrinsic plane should satisfy the boundary conditions as $Z_{IN}(\omega_0) = R_{opt}$, $Z_{IN}(2\omega_0) = 0$ and $Z_{IN}(3\omega_0) = \infty$ for the class F PA. In practical design, the main parameters for harmonic termination design of Z_{IN} are C_{DS}, L_D, C_{SH}, L_{Bvia}, C_0, and the effective inductances of TL_4, TL_5, and the series TL_3.

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Table 1. Comparison of Previous Published 0.25-µm GaN/GaAs MMIC PAs

Ref.	Topology	Technology	Freq. (GHz)	Small-signal gain (dB)	Peak P_{out} (dBm)	P_{1dB} (dBm)	PAE at Peak P_{out} (%)	3-dB BW (MHz)	Chip-Size (mm×mm)
[3]	Doherty	GaN 0.25 µm	5.9	15	38.7	32.1	47.3	NA	2.49 × 1.56
[4]	Doherty	GaN 0.25 µm	14.6	7	36.0	30	40.0	NA	3.1 × 1.6
[6]	Class F	GaN 0.25 µm	4	11.4	30.4	NA	69	400	3.3 × 2.5
[7]	Class F	GaAs 0.25 µm	13.95	10.5	26.5	NA	57.6	1800	NA
[8]	Class F	GaAs 0.25 µm	5.5	13.7	27.5	NA	70	NA	1.24 × 1.25
This work	Class F	GaN 0.25 µm	6.0	10.8	36.6	35.5	65.8	1800*/2300+	1.6 × 1.6

*Measured small-signal 3-dB bandwidth; +Simulated large-signal 3-dB bandwidth at P_{IN} of 26.5 dBm (around peak PAE).

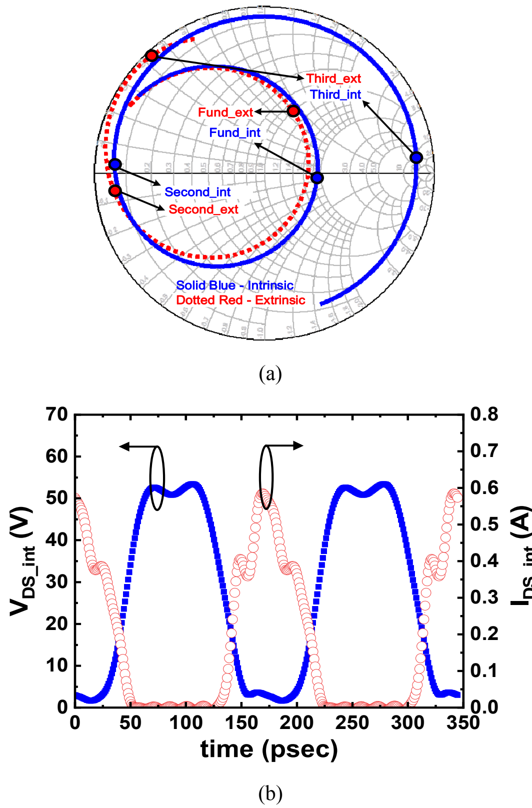

Fig. 3. (a) Simulated matching trajectories from 3 to 20 GHz for the proposed class F PA at the device intrinsic and extrinsic planes. (b) Time domain waveform at device intrinsic plane.

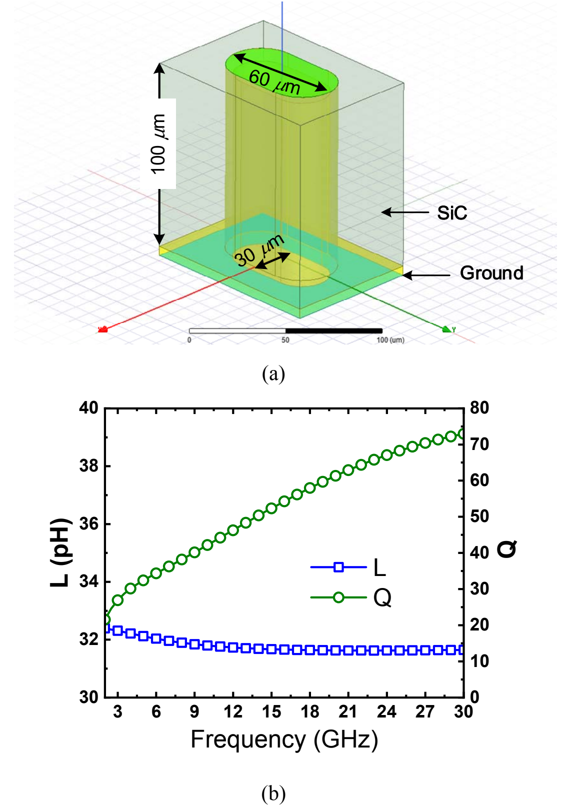

Fig. 4. (a) 3D plot of the standard back via in the adopted 0.25-µm GaN HEMT technology. (b) full-wave (HFSS) simulated results of inductance and quality factor.

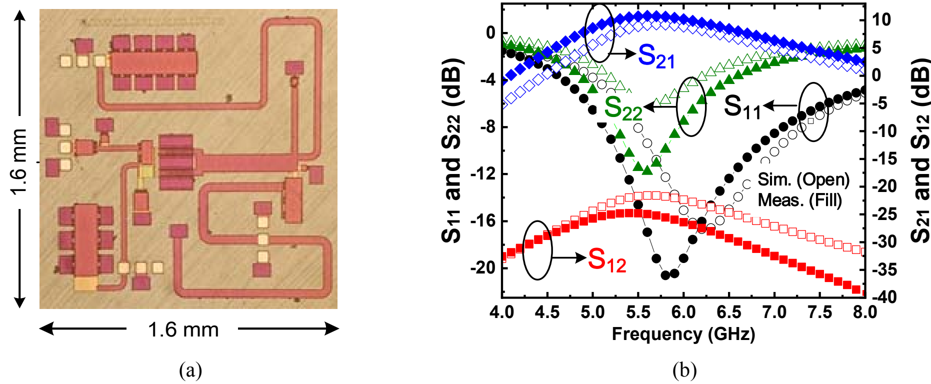

Fig. 5. (a) Chip micrograph of the fabricated class F amplifier. (b) Comparison of simulated and measured small-signal S-parameters.

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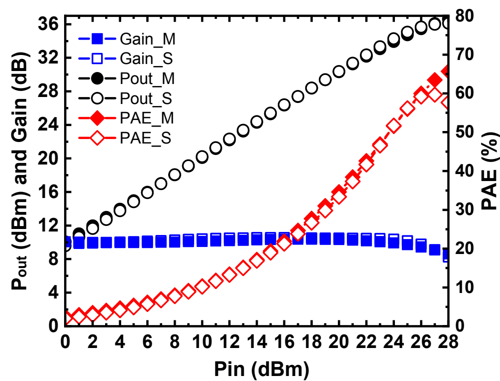

Fig. 6. P_{out}, gain, and PAE versus input power at 6.0 GHz of the class F PA.

III. Results and Discussion

Fig. 5(a) shows the chip micrograph of the fabricated class F PA by 0.25 μm GaN technology with a chip size of 1.6 mm × 1.6 mm (2.56 mm^2). The amplifier was biased from a 28 V dc supply and measured on-wafer. A pre-amplifier was used to enhance the maximum input power to 28 dBm. Fig. 5(b) compares the measured and simulated small-signal S-parameters of the circuit from 4 to 8 GHz at an input power of -20 dBm. The input and output return loss larger than 10 dB is obtained in a range of 5.3 to 6.8 GHz and 5.4 to 5.8 GHz, respectively. The small-signal gain S_{21} around 10 dB is achieved from 5.2 to 6.1 GHz, and the 3-dB BW is about 1800 MHz. Note that the simulated results indicate that the large-signal BW is extended to 2300 MHz under P_{IN} of 26.5 dBm. The measured results shown in Fig. 6 at 6.0 GHz demonstrate that a peak output power of 36.6 dBm with a PAE of 65.8 % can be achieved. In addition, the amplifier shows a P_{1dB} of 35.5 dBm with an associated PAE of 60 %. Table I shows the comparison with previous PAs in 0.25-µm GaN or GaAs HEMT technology.

IV. Conclusion

A high performance compact MMIC class F power amplifier aiming for 5G small cell applications was demonstrated in 0.25 μm GaN HEMT technology. The 2nd and 3rd harmonics were terminated by the output matching network, and optimized with the high quality factor backside via parasitic inductance. The device drain-source parasitic capacitance was also absorbed into the output matching circuit for improving the bandwidth and high frequency operation. The circuit achieved a high PAE of 65.8 % at 1.5 dB gain compression, with 36.6 dBm output power at 6 GHz.

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