A K-Band Power Amplifier with Adaptive Bias in 90-nm CMOS

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***Abstract*—A K-band power amplifier (PA) with adaptive bias circuitry is implemented in 90-nm CMOS technology. The two-stage transformer-coupled differential PA achieves a linear gain of 26.9 dB, a saturation output power (Psat) of 20.4 dBm, an output 1-dB compression point (P1dB) of 18.5 dBm, and a peak power-added-efficiency (PAE) of 17.3% at 21 GHz. With the on-chip adaptive bias control, the bias condition of the amplifier varies dynamically with the input power level, therefore the PAE is optimized. The PAE at P1dB is 13.3%. At the 6-dB back-off power level, the DC power dissipation is reduced by 45% compared to a class-A linear PA.**

Keywords—24 GHz; adaptive bias; CMOS; K-band; power amplifier.

I. INTRODUCTION

K-band spectrum draws great attention in recent years because of its broad range of applications, including short-range automotive radar at 22 – 29 GHz, ISM (industrial, scientific, and medical) band at 24 – 24.5 GHz, unlicensed point-to-point data link, radio astronomy, and satellite communication. CMOS technology is promising to implement such a system for a high-volume market due to its low cost and high-level integration. However, CMOS technology poses critical RF design challenges due to its conductive substrate, low supply and breakdown voltages, limited available gain at high frequency, etc. For power amplifier (PA) design, these constraints translate to the performance limitations on output power, efficiency, gain, and linearity.

The digitally modulated signal with complex modulation scheme enables high-speed wireless communication. The modulated signal has high peak-to-average power ratio (PAPR) that the amplitude variation could be as large as 12 dB due to the transmission distance and the modulation scheme. A highly linear PA is required to satisfy the spectrum mask and the error vector magnitude (EVM) requirements. For a great amount of time, the PA operates in the power back-off region when the high PAPR signal is applied. In general, highly linear CMOS PA has poor back-off efficiency because it is biased with a high gate voltage to maintain its linearity. Back-off efficiency is hence critical for signals with complex modulation scheme because it dominates the overall system efficiency.

In this work, a K-band integrated high power linear PA in 90-nm standard CMOS is demonstrated. The PA is designed with an adaptive bias control to optimize the power-added-efficiency (PAE) at various power levels such that a great output power and back-off efficiency can be achieved simultaneously. Compared to other efficiency enhancement techniques, such as Doherty amplifier and out-phasing amplifier, the PA with adaptive bias control performs a good tradeoff among design complexity, operation frequency, linearity, efficiency, chip area, and output power [1] – [3]. At the 6-dB power back-off, the DC power dissipation of the proposed PA is reduced by 45% and the PA maintains a PAE of 4%, while the PA achieves superior large-signal power performance, including a saturation output power (Psat) of 20.4 dBm, a peak PAE of 17.3%, and a power gain of 26.9 dB at 21 GHz under a supply voltage of 2.4 V. This paper is organized as follows. Section II describes the details of the proposed PA. Experiment results are presented in Section III followed by a conclusion in Section IV.

II. PROPOSED PA WITH ADAPTIVE BIAS

A two-stage PA is proposed for high output power, high efficiency and high linearity with a compact size. This PA is a differential transformer-coupled design in 90-nm CMOS process with nine metal layers with one thick top metal for low-loss passive design and interconnects. All passive components and interconnects are simulated by Sonnet. The schematic is shown in Fig. 1(a).

Fully differential configuration is chosen to minimize the interferences to other blocks, lower the even-order harmonics, and reject common-mode noise. Cascode topology is chosen over the common-source (CS) counterpart because a single cascode stage offers 8 dB more available gain than a CS stage at 24 GHz. In addition, cascode amplifier provides higher isolation than CS amplifier. For each transistor, deep n-well structure is used to suppress the noise coupling through the conductive substrate. The widths of the CS devices (M1/M2, M5/M6) are 72 μm and 192 μm, respectively. The widths of the cascode devices are scaled by a factor of 1.5 of the CS. A shunt feedback formed by RF and CF is added in each stage to extend the operation bandwidth. Considering the tradeoff between gain and bandwidth, the feedback is added across the CS for the first stage and across the cascode for the second stage.

This design utilizes transformers to provide a compact impedance matching and a simple biasing scheme applied at the center-taps. The high-pass characteristic of the transformers ensures stability at low frequencies. At input and output, the transformers serve as baluns to convert single-ended signals to differential ones and vice versa to facilitate

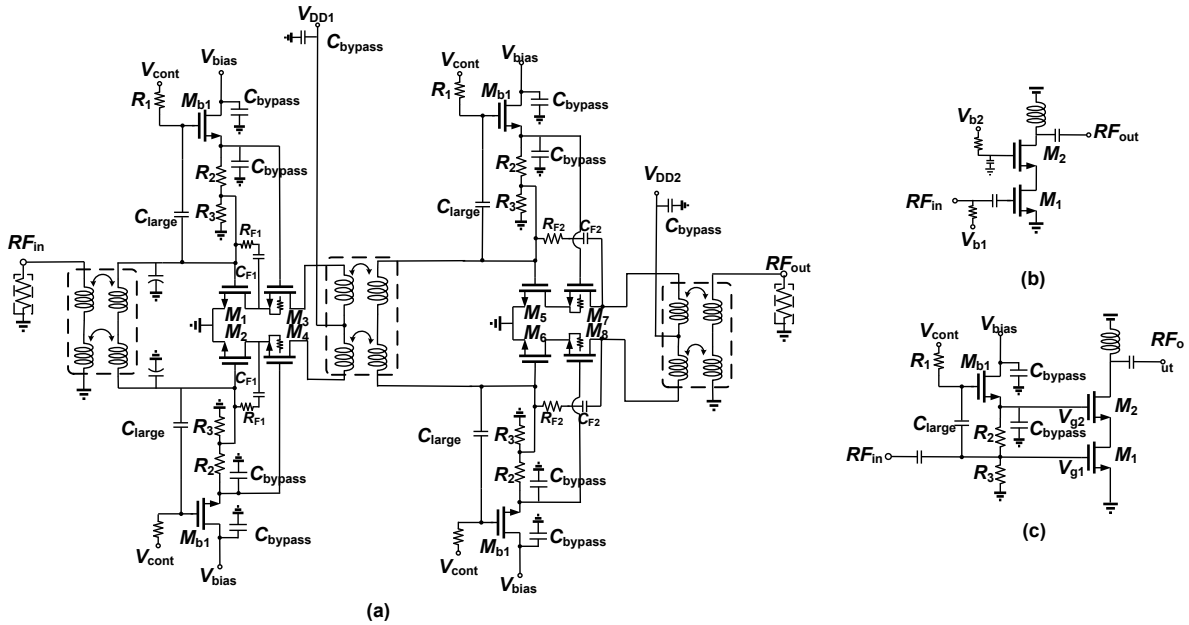

Fig. 1. (a) Circuit schematic of the proposed PA. (b) Conventional PA bias scheme. (c) Proposed bias scheme.

measurement. The width of the input transformer is relatively narrow of 6 μm to minimize the coupling capacitance from coils to substrate to maximize the self-resonant frequency. Both the primary and secondary coils are implemented on the top metal to maximize the quality factors. The width of the inter-stage and output transformers is 10 μm to match with large devices in the last stage and to provide sufficient current-handling capability. Because of its large size, a vertically stacked transformer is adopted for a compact design.

In order to optimize the back-off efficiency, an adaptive bias control (M_{b1}, V_{bias}, V_{cont}, R_1, R_2, R_3) with small power and area overheads is applied to each cascode stage to dynamically adjust its gate biases according to the power level. The conventional DC feed of the PA via resistors is shown in Fig. 1(b), and the proposed bias technique is shown in Fig. 1(c). The input signal is coupled to this control circuit through a large capacitor. Depending on the coupled voltage swing, the control circuit adjusts the gate biases of the cascode amplifier in real-time. In this control circuit, M_{b1} is biased close to the threshold voltage. When input power increases, the coupled signal increases the average gate bias of M_{b1}.

By properly choosing the V_{bias}, M_{b1} enters the triode region and can be treated as a resistor. The equivalent resistance of M_{b1} decreases with the increasing input power. V_{G1} and V_{G2} increase proportionally. The optimal bias curves of the PA are first acquired from simulation to minimize DC power consumption in the low power region and adaptively increase the biases while power increases to achieve the best P_{1dB}. The sizes of M_{b1}, V_{bias}, V_{cont}, R_2, R_3 are selected accordingly so that the provided biases match the optimal ones from simulation. V_{cont} is fed to M_{b1} by R_1 and it sets the initial gate biases of V_{G1} = 0.8 V and V_{G2} = 1.1 V when the input power is low. The bias condition minimizes the DC power dissipation and determines the linear gain of the PA. V_{bias} sets the final gate biases of V_{G1} = 1.7 V and V_{G2} = 2.2 V when the PA

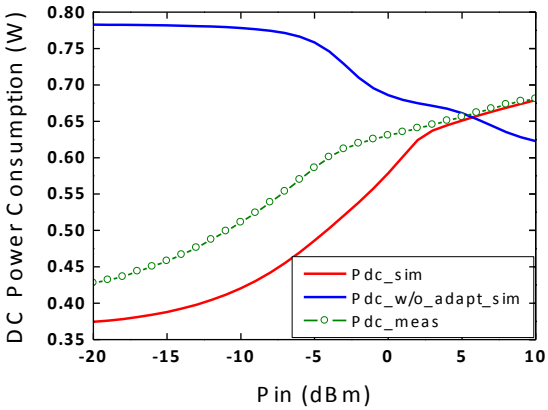

Fig. 2. DC power with and without the adaptive bias control.

reaches its saturation. V_{cont} and V_{bias} are slightly different for the two stages to optimize the efficiency and the P_{1dB}. Part of the input signal couples to the adaptive bias circuitry with a power division ratio proportional to the input impedance of this circuitry and that of the main amplifier. The input impedance of the adaptive bias circuitry is therefore chosen to be small in order to minimize the input power loss. Bypass capacitors are necessary to block unwanted nonlinear addition of signal coupling to the PA input from the adaptive bias circuitry. The parameters of M_{b1}, R_2 and R_3 set the division ratio of V_{G2} and V_{G1}. By selecting the parameters of R_2, R_3, and C_{bypass}, the bandwidth of the loop can be set higher than that of the signal envelope. Therefore, the dynamic gate voltage can promptly track the input signal envelope.

An identical class-A PA is designed with the gate voltages fixed at 1 V and 2.1 V for the CS and the cascode devices for

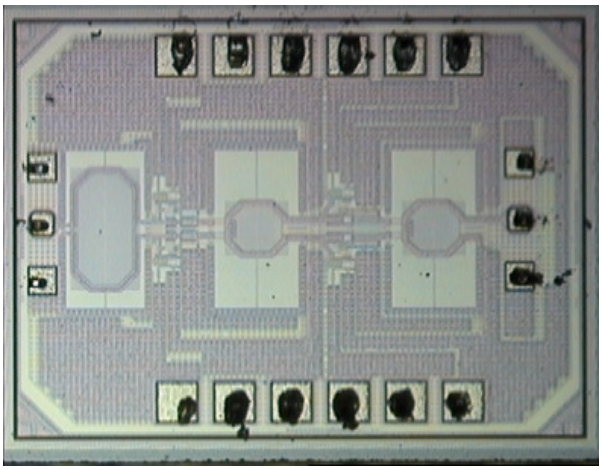

Fig. 3. Chip micrograph of the proposed PA.

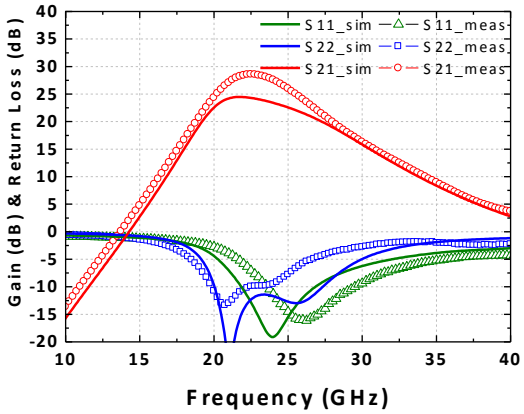

Fig. 4. Measured S-parameters of the proposed PA.

comparison. Fig. 2 shows the comparison of the DC power dissipations of the PA with the adaptive biases and that with the fixed biases. The proposed PA saves 350 mW at quiescent state and 280 mW at the 6-dB back-off. The decreasing of the DC power dissipation of the class-A PA is due to the reduced conduction angle in the large power region. With the adaptive bias control, the linear gain is slightly lowered by 1.6 dB, whereas the simulated PAEs at the P_{1dB} and at the back-off region are improved from 16.5% to 22% and 3.2% to 7.8%, respectively, which present an average improvement of over 39% at P_{1dB} and below.

III. Experimental Results

The chip is fabricated in 90-nm CMOS technology. The chip micrograph is shown in Fig. 3. The PA occupies a compact area of 1 × 0.74 mm^2 including the pads. All measurements are done via on-chip probing. At 2.4 V, the total quiescent power dissipation is 430 mW.

The S-parameters are measured directly from an Agilent N5245A network analyzer. The simulated and measured results are shown with good consistency from DC to 50 GHz in Fig. 4. The PA provides a peak gain of 29 dB at 21 GHz. The gain is greater than 20 dB from 19 GHz to 27 GHz. The

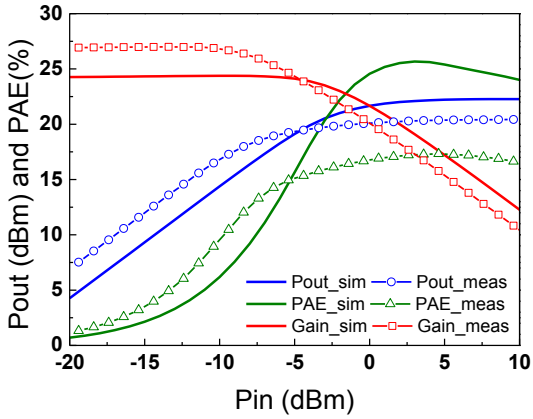

Fig. 5. Measured power performance of the PA at 21 GHz.

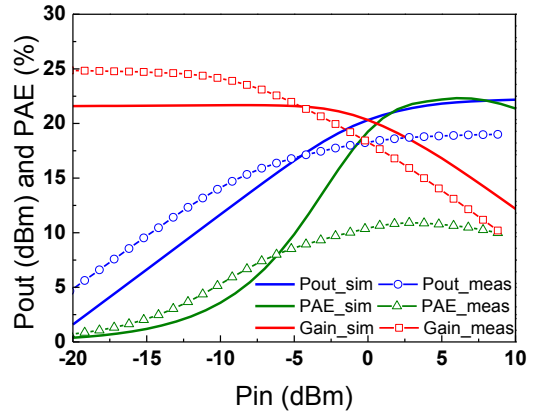

Fig. 6. Measured power performance of the PA at 26 GHz.

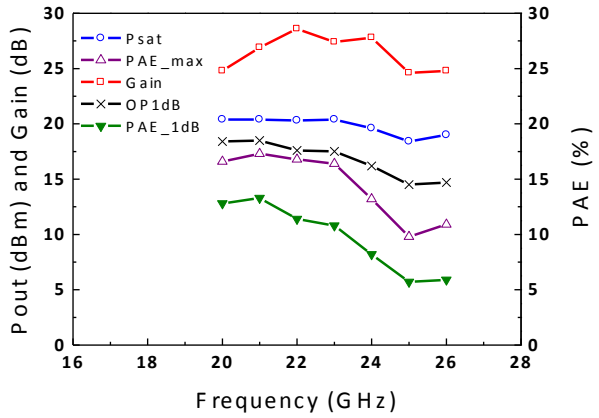

Fig. 7. Measured performance vs. frequency of the PA.

stability factor *k* larger than one across the measured spectrum demonstrates unconditional stability.

Single-tone large-signal power performance of the PA is measured by an Agilent E8257 signal generator and an Agilent E4448A spectrum analyzer. Fig. 5 and Fig. 6 show the power gain, output power, and PAE of the PA at 21 GHz and 26 GHz,

TABLE I
COMPARISON OF K-BAND CMOS POWER AMPLIFIERS

Ref.	Freq. (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE_{max} (%)	PAE_{1dB} (%)	Area (mm^2)	Technology (nm)
[1]	22	11.9	17.4	15.4	12	12	0.4	180
[4]	22	16.3	16.8	14.3	10.7	4*	0.35	180
[5]	20	22.5	20.1	16.2	9.3	3.9	0.79	180
[6]	19	22	23.8	N/A	25.1	N/A	0.96	65
[7]	21	19.5	20	N/A	12.4	N/A	1.68	130
[8]	24	19	19	15.7	24.7	15*	0.37	180
This work	21	26.9	20.4	18.5	17.3	13.3	0.74	90

*: estimated from the figures

respectively. At 21 GHz, the P_{1dB} and P_{sat} are 18.5 dBm and 20.4 dBm and at 26 GHz, the P_{1dB} and P_{sat} are 14.7 dBm and 19 dBm, respectively. The measured peak PAEs at 21 GHz and 26 GHz are 17.3% and 11%, respectively. Fig. 7 showsthe measured gain, P_{sat}, P_{1dB}, peak PAE, and the PAE at P_{1dB} as a function of frequency. Over 18.5 dBm of P_{sat} and 10% of peak PAE are achieved from 20 – 26 GHz.

IV. CONCLUSION

A K-band CMOS PA with an adaptive bias control is designed and demonstrated. With the proposed on-chip adaptive bias circuitry, the operation point is optimized at each power level. The PA operates with low quiescent DC power in the low power region to enhance the PAE in the power back-off while the DC power increases with the input power to maximize the large-signal performance. This PA delivers a Psat of 20.4 dBm and a P1dB of 18.5 dBm at 21 GHz. The peak PAE and the PAE at P1dB are 17.3% and 13.3%, respectively. Table 1 summarizes the measurement results of this PA with the previously published CMOS K-band PAs [1], [4] –[8]. The PA shows superior gain, output power and efficiency in both small- and large-signal regions. This work provides a feasible solution for applications in the spectrum-efficient wireless data link. To authors' best knowledge, this is the first cascode PA with the real-time bias adjustments for all of the transistors to best optimize the PAE and linearity. This PA achieves the highest P1dB among all K-band CMOS PAs without power combining.

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