A Low Phase-Noise 24GHz CMOS Quadrature-VCO Using PMOS-Source-Follower Coupling Technique

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***Abstract*—An effective coupling topology for multi-phase oscillators is proposed and demonstrated in a standard 90nm CMOS technology. Compared with the conventional parallel or series coupling methods, the PMOS-source-follower coupled (PSFC) technique with the coupling transistors operated in the cut-off region can significantly reduce the flicker noise and hence the phase noise of VCO. The proposed PSFC QVCOs at 24.39GHz demonstrates a low phase noise of -106.05dBc/Hz at 1MHz offset with a tuning range of 3.22GHz under the supply voltage and current consumption of 1V and 6.2mA, respectively. The proposed PSFC-QVCO exhibits a better FOM_T of 188.2dBc/Hz and smaller chip area (core area only 0.18 mm^2) than previous works.**

Keywords—CMOS, flicker noise, phase noise, quadrature voltage-controlled oscillators (QVCOs), PSFC-QVCO

I. INTRODUCTION

A high performance voltage-controlled oscillator (VCO) is the key component of wireless transceiver front-end circuits. At present, the most popular method is to let the VCO works at double the desired frequency, and then to obtain the quadrature signals at desired frequency via frequency divisions. However, the higher oscillation frequency and frequency-dividing circuitry result in an increased power level. Another method is the differential VCO using the poly-phase filter to obtain the quadrature signals. Similarly, this approach introduces substantial power consumption. Recently, the quadrature voltage-controlled oscillators (QVCOs) for high frequency applications have been extensively studied due to their potential merits of lower power consumption. Conventionally, QVCOs are formed by coupling two symmetric LC-tank VCOs. The parallel-coupled QVCOs (P-QVCOs) [1] and series-coupled QVCOs (S-QVCOs) [2] are the two most popular topologies for quadrature signal generation. The P-QVCO has the drawback of the poor phase noise performance contributed from the 1/*f* noise of the coupling transistors. In general, the S-QVCO exhibits better phase noise characteristics than the P-QVCO. However, it consumes more voltage headroom and thus is not suitable for low supply voltage applications. A design technique for achieving low supply voltage and low phase noise is using transformer feedback. The transformer feedback technique [3]-[4] presents low phase noise because of the increased output swing. However, the on-chip transformer could occupy a large chip area, and the quality factor of the transformer decreases as the operating frequency increases.

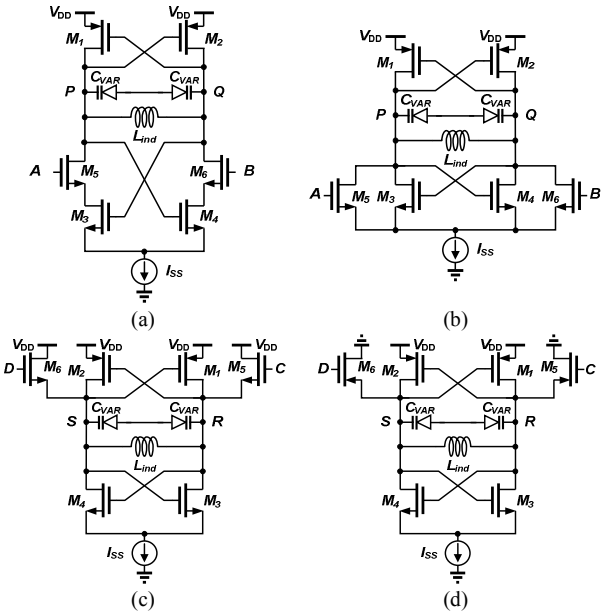

Fig. 1. Half-schematic of (a) conventional series-coupled QVCO (S-QVCO), (b) conventional parallel-coupled QVCO (P-QVCO) , (c) source-follower coupled QVCO [5], and (d) the proposed PMOS-source-follower coupled QVCO

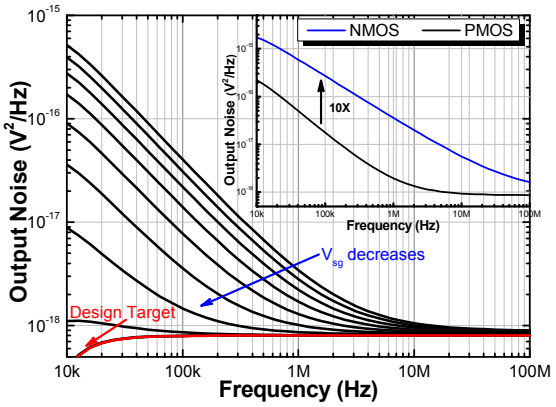

Fig. 2. Simulated results of PMOS and NMOS flicker noise characteristics.

The source-follower coupling technique could suppress the 1/*f* noise upconverted to LC tanks from the coupling transistors, which are operated in the cut-off region [5]. Basically, the NMOS transistor has a higher flicker noise level than that of PMOS when operated in the saturation

region. In this paper, a PMOS-source-follower coupling (PSFC) technique is implemented in 90nm CMOS. The proposed PSFC-QVCO achieves a low phase noise of -106.05dBc/Hz at 1MHz offset from the carrier frequency, corresponding to a figure-of-merit (FOM_T) [6] of 188.2 dBc/Hz. The VCO is operated under dc current only 6.2mA drawn from a 1V supply voltage. The proposed PSFC-QVCO is suitable for the applications in high performance frequency synthesizers.

II. Circuit Design

The PSFC-QVCO is fabricated by using the TSMC commercial standard bulk 90-nm 1P9M CMOS process. The transistor exhibits the unity power gain frequency (f_{MAX}) of 170 GHz and the unity current gain frequency (f_T) of 120 GHz. The passive devices including MIM capacitor, spiral inductor, and poly-silicon resistor are available in this CMOS process. To reduce the substrate loss and unwanted coupling effect, the grounded-coplanar waveguide (G-CPW) structure is employed for the layout design.

Fig. 1 compares different QVCO topologies (half-circuit). Fig.1 (b) shows the conventional parallel-coupled QVCO (P-QVCO). In the complementary VCO, the bias point of output node P (or Q) is usually designed to be approximately $V_{DD}/2$ to ensure the rising and falling time symmetry for reducing the $1/f^3$ noise corner [7]. For the quadrature signal generation, the output node P (or Q) of the other complementary VCO will be directly connected to the gate of the coupling transistors M_5 (or M_6), as a result, V_A (or V_B) is equal to $V_{DD}/2$. Neglecting the small on-resistance of the coupling transistors, the gate-to-source voltage (V_{GS}) is also approximated to $V_{DD}/2$, hence the transistors stay in the saturation region, and generate $1/f$ noise current in the drain of M_5 (or M_6). The switching operation of the coupling transistors will then upconvert the 1/f noise to the resonance frequency, resulting in the phase noise degradation.

It is known that channel charge trapping could be reduced by decreasing V_{GS} of the transistors [8]. In other words, in order to improve the flicker noise performance, V_{GS} has to be decreased. Fig. 2 shows the simulated results of both PMOS and NMOS biased at the same condition with the channel size of 8μm width and 0.1μm length, which is the size of coupling transistor in this design. It can be seen that PMOS has lower flicker noise than NMOS at this bias condition. Furthermore, PMOS with smaller V_{GS} could lead to better flicker noise. Based on this, a new QVCO using PMOS-source-follower coupling (PSFC) technique as shown in Fig. 1(d) is proposed. The source-follower M_5 (or M_6) is utilized as the coupling transistors for quadrature signal generation to make V_C (or V_D) of M_5 (or M_6) equal to the voltage of node R (or S). It will maintain the coupling transistor operated in the cut-off region for a longer time during an oscillation period. Fig. 3(a) shows the simulated waveform of output node V_R (or V_S), which exhibits the quadrature formation. Fig. 3(b) illustrates the detailed operation of coupling transistors turning on when V_{GS} are larger than the threshold voltage (V_{th}). Fig. 4 shows the

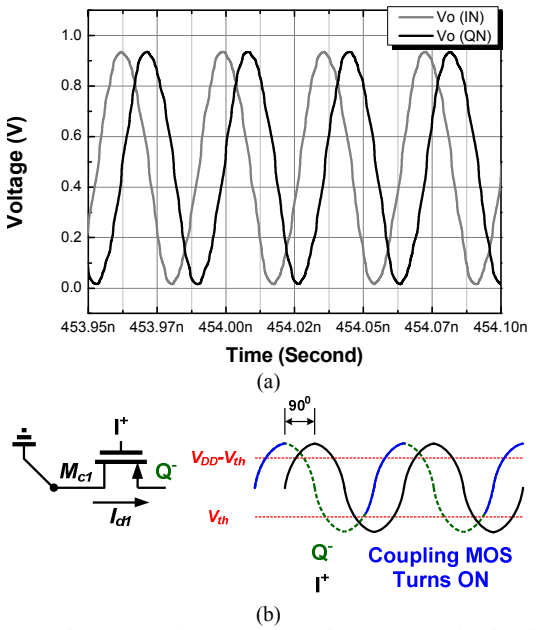

Fig. 3. Quadrature waveform at output node R (or S) (a) simulated results (b) operating concept of coupling transistors.

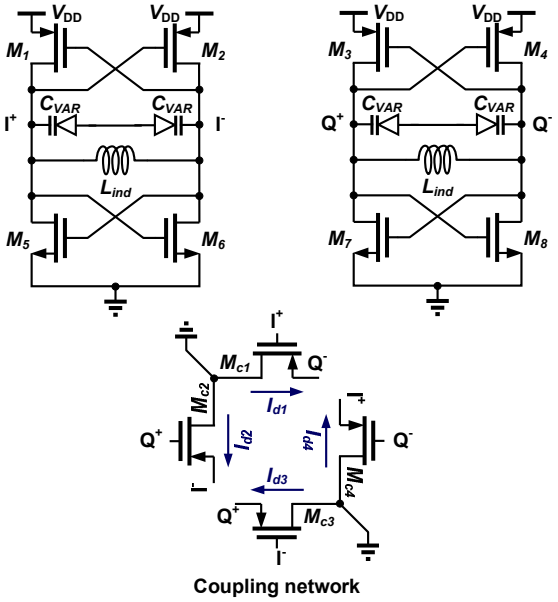

Fig. 4. Quadrature VCO with the PMOS-source follower technique.

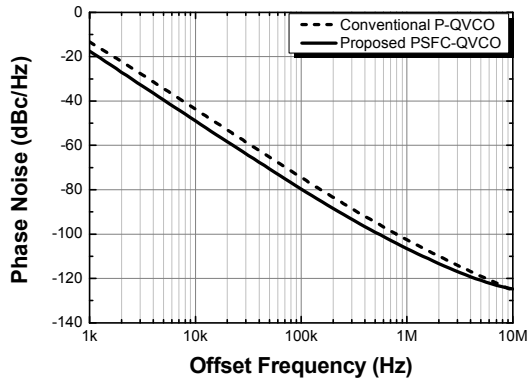

Fig. 5. Simulated phase noise of PSFC-QVCO and P-QVCO.

complete schematic of the proposed QVCO by adopting the PSFC technique. Fig. 5 shows the simulated phase noise performance of the PSFC-QVCO and P-QVCO (with the same architecture, but differ in coupling biasing method). Note the P-QVCO dissipates extra dc power because of the additional coupling transistors. It can be seen that the PSFC-QVCO exhibits improved in-band phase noise up to 5dB than the conventional P-QVCO topology.

Another important performance index of the QVCO is the phase and amplitude error. The quadrature accuracy is proportional to the coupling strength (α) [2]. However, the enhanced coupling strength could lead to the phase noise degradation. Fig. 6 shows the sideband suppression and phase noise as a function of the coupling strength. Another way to interpret the phase error is using the sideband suppression. For typical applications, a phase error better than 2.0° (corresponding to the sideband suppression of better than -42dBc) is desired, which means that α should be designed larger than 0.2. Based on the simulated result in Fig. 6, the phase noise and phase error of the PSFC-QVCO can be achieve at the same time by choosing a proper α of 0.2 (8μm/40μm) in the QVCO design with a phase error of 2.5°.

Since the amplitude and phase errors of the PSFC-QVCO are closely related to the symmetry of layout, the interconnections of the coupling paths should be considered carefully. All signal paths of the coupled transistors are kept as symmetric as possible to ensure minimum output phase error. The output quadrature signal power levels are amplified by the inverter-type buffers to reduce the unwanted loading effect. All the passive components, including the transmission lines, MIM capacitors, and spiral inductors, are simulated with a full-wave EM simulator. The chip photograph of the PSFC-QVCO is shown in Fig.7 with a chip size 0.46×0.82 mm^2 (core area only 0.18mm^2), including RF and dc bias pads.

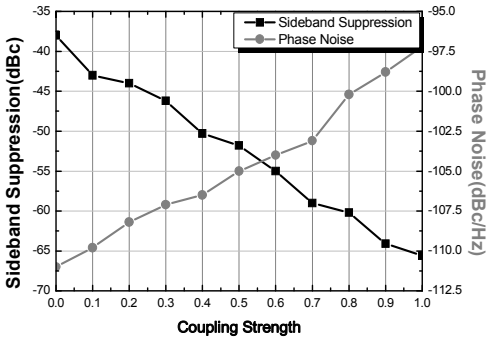

Fig. 6. Simulated sideband suppression and phase noise versus coupling strength.

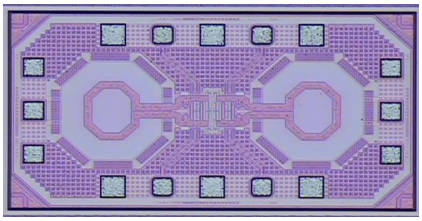

Fig. 7. Chip photograph of the proposed PSFC-QVCO with a chip size of 0.46 × 0.82mm^2, including RF and DC bias pads.

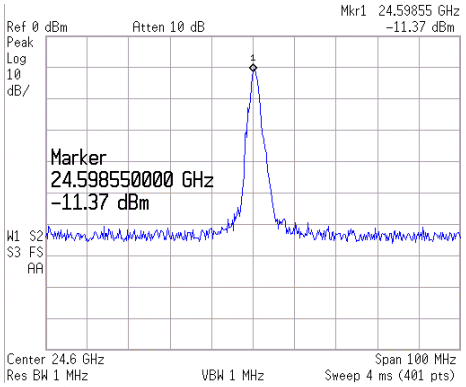

Fig. 8. Measured output spectrum.

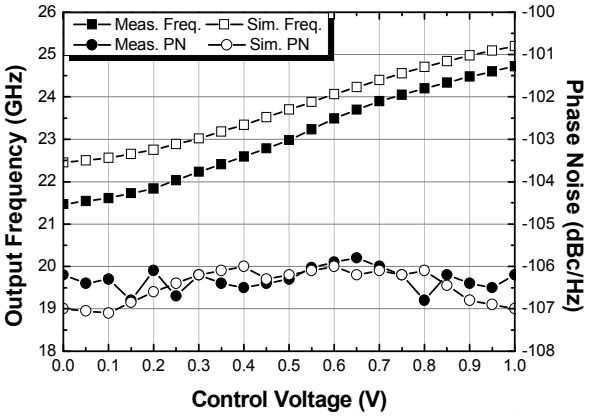

Fig. 9. Simulated and measured output frequencies and phase noise versus tuning voltage.

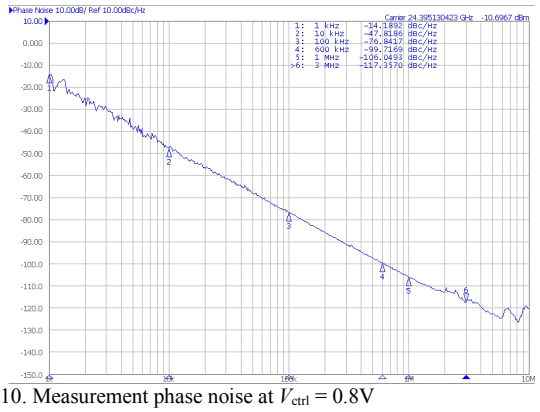

Fig. 10. Measurement phase noise at V_{ctrl} = 0.8V

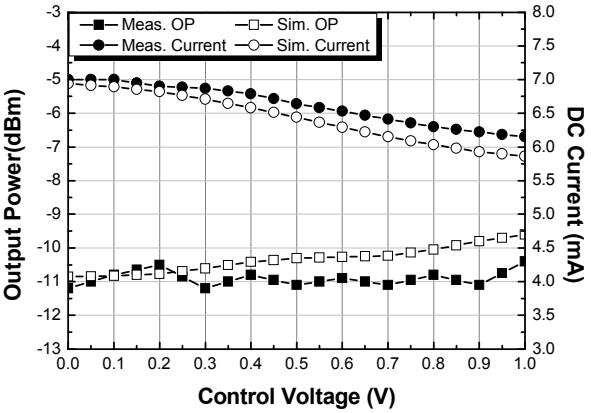

Fig. 11. Simulated and measured output power and DC current versus tuning voltage.

TABLE I
SUMMARY OF THE PHASE AND AMPLITUDE ERRORS

Ports	I+/Q+	I+/Q-	I+/I-	Q+/Q-	Q+/I-	Q-/I-
Phase Error (degree)	1.02	3.85	3.5	2.8	2.4	0.8
Amplitude Error (dB)	0.04	0.08	0.48	0.53	0.45	0.61

TABLE II
COMPARISONS OF THE PREVIOUSLY REPORTED QVCOS AND THIS WORK

Ref	CMOS Process	Freq. (GHz)	Phase Noise @ 1MHz (dBc/Hz)	Tuning Range (%)	Amplitude/ Phase Error	V_{DD}/I_{DD} (V/mA)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Area (mm^2)	Topology
[4]	180nm	16.2	-110	17.28	N.A./1.4°	1/10	188.0	192	0.37[(a)]	Transformer coupling
[6]	90nm	20.9	-117.2	3.1	0.6dB/4°	1.7/3.71	195.6	185.4	0.77	Current-Reuse TF coupling
[10]	130nm	20.17	-102.41	10.2	N.A.	1.2/26.67[(b)]	179.4	179.7	0.72	Parallel coupling
[11]	90nm	23.8	-105	7.1	0.6dB/4°	1.2/18	179.2	176.2	0.47	Super-Harmonic coupling
This work	90nm	24.39	-106.05	13.4	0.61dB/3.9°	1/6.2	185.8	188.2	0.377 0.18[(a)]	PMOS Source-Follower coupling

[(a)]: only core area.
[(b)]: Total dc power consumption includes VCO core and buffer amplifier.

III. EXPERIMENT RESULTS

The proposed PSFC-QVCO was fabricated in 90 nm CMOS technology with a chip size of 0.377 mm^2. Under a 1-V supply voltage, the DC power consumption of the core circuit and buffer are 6.2 mW and 8 mW, respectively. The output spectrum was measured by the Agilent E4407B spectrum analyzer, and phase noise was measured by using the Agilent E5052B signal source analyzer with an Agilent E5053A microwave down-converter. Fig. 8 shows the measured output power of -11.37dBm. Fig. 9 shows the simulated and measured frequencies and phase noise at 1MHz offset frequency versus tuning voltage, and the measured phase noise is better than -105.8dBc/Hz over the entire tuning range. The measured tuning range is about 3.22GHz. The measured phase noise at 24.39GHz is -106.05dBc/Hz at 1MHz offset frequency as shown in Fig. 10. Fig. 11 shows the simulated and measured output power and dc bias current. The output power is higher than -12dBm over the tuning range. The amplitude and phase errors were measured by using Agilent N5247A PNA-X network analyzer operated in the receiver mode [9]. The measured amplitude and phase errors are summarized in Table I with the minimum and maximum phase errors of 0.2°and 3.85°, respectively. The measured performance and comparison with previous works are summarized in Table II. The proposed PSFC-QVCO shows an FOM_T [6] among the best with the smallest chip area, compared with previously reported QVCOs.

IV. CONCLUSION

A PSFC-QVCO using a commercial standard bulk 90-nm 1P9M CMOS process has been successfully demonstrated. With a compact chip area (core area only 0.18mm^2), the presented design achieved a low phase noise of -106.04dBc/Hz, low phase error of 3.85° (worst case), and an excellent FOM_T of 188.2dBc/Hz under low power consumption of 6.2mW. The proposed PSFC-QVCO is suitable for the application in high performance frequency synthesizers.

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