A Low Power CMOS Driver Integrated With Mach-Zehnder Modulator for PAM4 Optical Transmissions

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***Abstract* — In this paper, we design a wideband driver in 65nm CMOS and integrate with the MZM (Mach-Zehnder Modulator) and bias network to demonstrate high speed electrical-optical (EO) conversion. The driver uses DA (distributed amplifier) topology with stacked-FET cell to achieve more than 23 GHz bandwidth. The issue of breakdown tolerance and bandwidth is much improved by introducing the LPN (low pass network) with stack-FET. Also, the proposed driver adopts a different bias scheme to improve the power efficiency of traditional DA. A transmission efficiency of 15.96 pJ/bit is achieved with a total 734 mW power consumption. The NRZ and PAM4 signals can reach 32 Gb/s and 25 Gbaud/s with more than 5V and 3.8V differential amplitudes respectively by electrical measurements. With integration of MZM, the proposed design demonstrates operating speed of 25Gb/s with 5.41dB extinction ratio (ER) and 23 Gbaud/s with 3.78 ER for NRZ and PAM4 signals, respectively.**

***Keywords* — CMOS Modulator driver, Mach-Zehnder Modulator, Electro-Optic integrate, PAM4.**

I. Introduction

Optical data communication systems operating at multi-Gb/s rates across metro or long-haul spans rely upon external modulators to encode the transmitted optical carrier at a high extinction ratio (ER) and with minimal frequency chirp. The Mach-Zehnder Modulator (MZM) is often used for this purpose, however, the electronic circuits required to drive the interferometer remain one of the most challenging blocks in the optical transceiver. A large voltage swing must be developed across a load at data rates up to 40 Gb/s (i.e., from 2 to 10 V, depending upon MZM design and length [1]).

Fig. 1 shows an optical transmission front-end system. The digital signal is synthesized into a high-speed signal through the MUX and then amplified by the Modulator Driver. The amplified signal will control the absorption rate of the MZM to generate the optical modulation signal [2]. Modulator drivers for optical communication are often designed using the distributed amplifier (DA) topology due to its superior broad bandwidth, a flat gain response, and controlled output return loss [8]. However, it often suffers shortcomings such as large power consumption and insufficient breakdown voltage requirement for MZM drivers. To solve this problem, we use modified DA with the stacked-FET cell to enhance breakdown voltage by RC LPN (low pass network). Also, a different bias scheme is used from the conventional DA design. As a result, the power consumption is reduced by more than 50%.

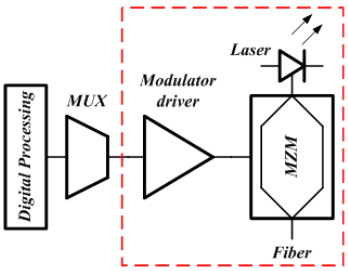


Fig. 1. Optical transmission front-end system.

II. Proposed Design

A. Proposed circuit topology

Fig. 2 shows the proposed driver topology in 65nm CMOS. It mainly consists of three parts including the stack-FET cell, input/output inductive network and the LPN. With the inherent transmission–line like configuration, the parasitic gate and drain capacitances in each FET can be absorbed to achieve wideband performance. As the input signal is fed into the DA, it can be sequentially amplified in phase. Although DA is a good candidate for broadband applications, the breakdown and power consumption are critical issues. In order to address these shortcomings, next section will describe how to optimize the stack-FET design and also the bias technique to reduce power.

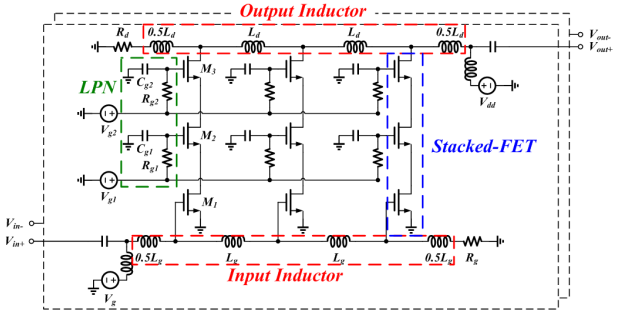


Fig. 2. Proposed MZM driver topology in 65nm CMOS.

B. Optimization of breakdown and bandwidth in the Stacked-FET

Fig. 3 shows the circuit schematics of stacked-FET and traditional cascode-FET. Both types of amplifiers consist of CS (common-source) and CG (common-gate) amplifiers. The reason why the cascode-FET suffers potential breakdown issue is the AC ground on gate terminal of the CG stage. With a large output swing appearing at the drain terminal of CG, V_{dg} of CG is equal to the output swing. Therefore, in high output swing applications such as the MZM driver, using cascode-FET will severely suffer breakdown issue. To ease the breakdown issue, the stacked-FET topology can be used to introduce the capacitor voltage divider on the gate terminal of CG [3]. With the given output swing, V_{dg} voltage drop becomes only a part of the entire output voltage swing. However, although the breakdown can be enhanced by stacked-FET, the bandwidth is still an issue [4].

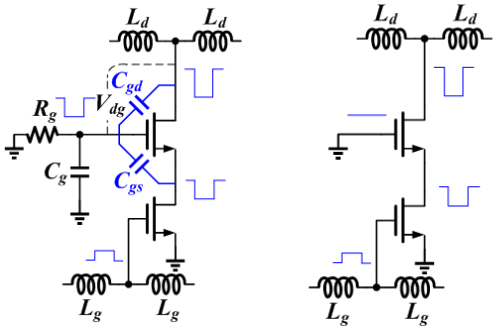


Fig. 3. (a) Stacked-FET; (b) Cascode-FET.

$$V_{dg} = V_{ds} \times \frac{2C_g + C_{gs}}{C_{gs} + C_g + C_{gd}} \quad (1)$$

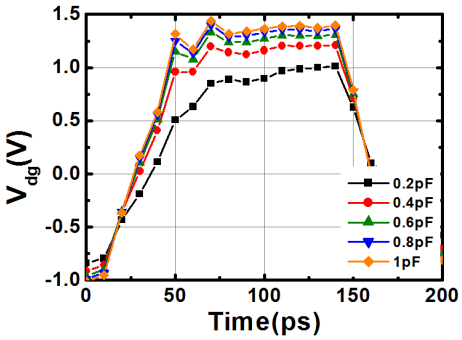


Fig. 4. V_{dg} time domain waveform of different C_g (R_g = 1kOhm).

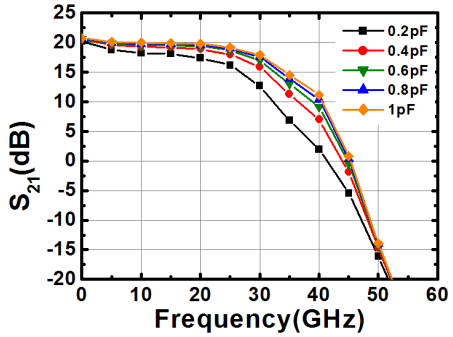


Fig. 5. S_{21} simulated result of different C_g (R_g = 1kOhm).

Equation (1) shows the drain-gate voltage of the CG stage in the stacked-FET design with an external shunt gate capacitor C_g. Fig. 4 and Fig. 5 illustrate the simulated time domain V_{dg} waveforms and S_{21} of the modulator driver based on the stacked-FET topology under a fixed R_g. Improved breakdown headroom can be obtained by using smaller C_g which is corresponding to small V_{dg}. However, using smaller C_g also decrease the bandwidth, as can be seen in Fig. 5. To relax the tradeoff between breakdown and bandwidth limitation, design of the LPN (low-pass network) at the gate terminal of CG is critical. Based on the simulated results without optimization, 20 dB gain and 2.25 V V_{dg} can be achieved with C_g = 0.6 pF and R_g =1 kOhm as shown in Fig. 4. A further improvement can be obtained by optimizing R_g to obtain more breakdown headroom (100 mV increasing) as shown in Fig. 6. As can be seen, we can achieve optimum design with R_g of 1.5 kΩ to increase the breakdown margin with nearly a same bandwidth performance.

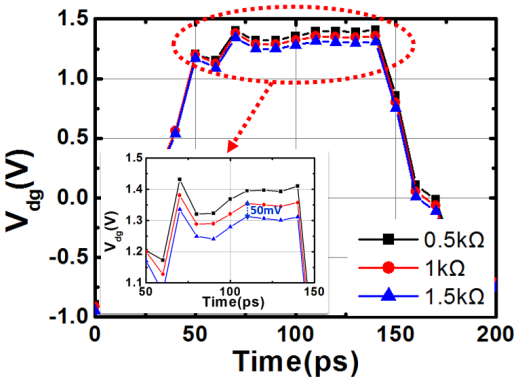


Fig. 6. V_{dg} time domain waveforms of different R_g.

C. Bias design for improved power efficiency

To prevent reflected wave from impedance mismatch, the terminal resistances for both gate and drain lines are inevitable. Fig. 7(a) shows a typical way for bias applied in a DA. The DC supply is fed in the left-hand side, and all the current in each stage flows into the termination resistor (R_d) [5], which consumes a huge additional power. To maintain sufficient output swing, a high supply voltage V_d is necessary to keep transistor operating in the saturation region.

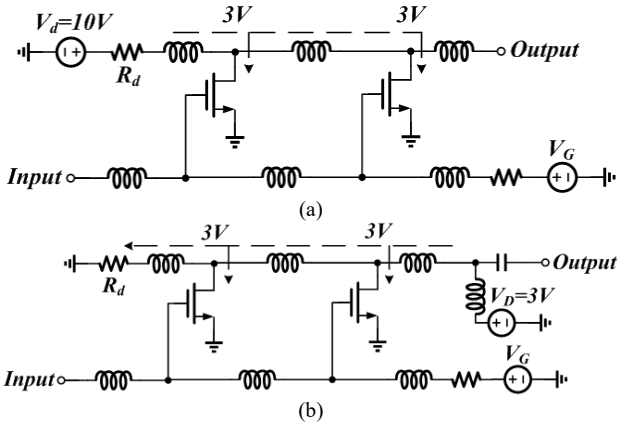


Fig. 7. Distributed amplifier bias approaches: (a) traditional bias scheme (b) proposed bias scheme.

In Fig. 7(b), the bias for V_d is applied at the output terminal with an external bias-tee network including the DC block and RF choke. With the proposed bias scheme, a substantial improvement of power consumption can be achieved. Table I shows comparison of power consumption. As the drain voltage of each stages keep approximately same as 3V, a much higher supply voltage of 10V is needed with the conventional design. The proposed bias scheme can reduce power consumption by over 50% due to a much lowered V_d.

Table 1. Power Consumption Comparison

	V_d(V)	I_d(mA)	P_{dc}(W)
Conventional design	10	121	1.21
Proposed bias scheme	3	173	0.52

III. Experimental Results

The proposed photonic MZM transmitter is composed of a bulk CMOS driver and an in-house developed SOI CMOS modulator. The driver is fabricated by a standard TSMC 65 nm 1P9M CMOS process, occupying a 0.13 mm^2 chip area, as shown in Fig. 8. Measurements are performed in the driver along first, and followed by the integration with the MZM modulator on board.

A. Electrical measurements

The driver was first tested using a vector network analyser (VNA) to characterize its gain and terminal impedance. Keysight N5247A network analyser is used for 4-port differential S-parameters measurements. As shown in Fig. 9, the 3-dB bandwidth is 23 GHz and the small-signal gain S_{21} of the circuit is 18 dB within the bandwidth.

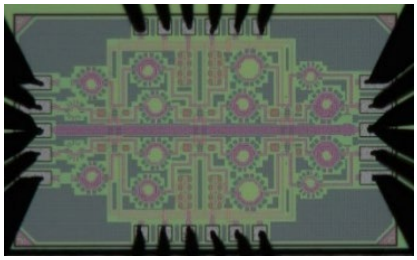


Fig. 8. Chip photo of the MZM modulator driver in 65nm CMOS.

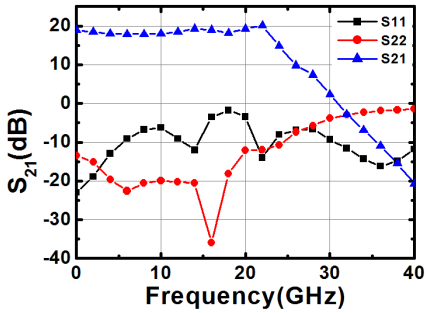
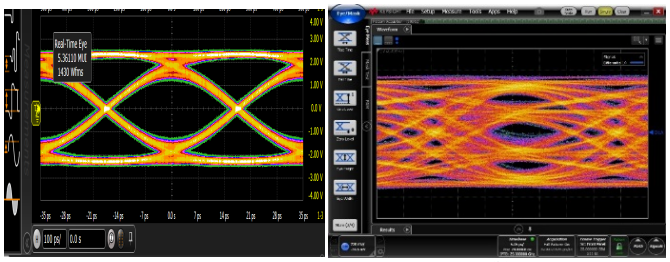


Fig. 9. Measured differential S-parameters.

For the transient signal testing, differential PRBS-31 signals (Antritsu MP1800A pattern generator) are fed into the driver. The output signal is captured by Keysight DSOZ504A Infiniium real time oscilloscope. The NRZ eye diagram measurement result is shown in Fig. 10(a). The transmission speed operated in NRZ will reach 30 Gb/s with a differential amplitude up to 5Vpp. In the PAM4 eye signal test, measurement result is shown in Fig. 10(b). The PAM4 signal can approach 25 Gbaud/s with a differential amplitude of 3.8Vpp.

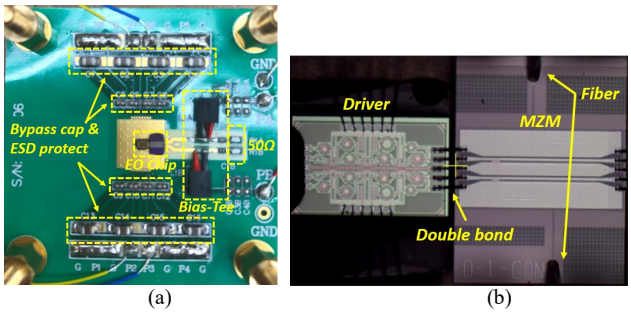


(a) (b)

Fig. 10. Measured electrical output eye diagrams: (a)NRZ at 30Gb/s (b) PAM4 at 25 Gbaud/s.

B. EO integration with optical measurements

Fig.11(a) shows integrated electrical circuit and optical components which includes the wire bonded driver and MZM, wideband bias-tee network and ESD protection capacitor. To reduce the parasitic inductance, the MZM driver is directly bonded to the modulator using two parallel bond wires as shown in Fig. 11(b). To apply the bias for driver, we design a wide bandwidth bias-tee on the PCB. Since the operating frequency of the circuit covers from DC to 23GHz, the choice of inductor choke and decouple capacitor are critical in this wideband applications. The American Technical Ceramics 506WLSN10R7KT150T inductor (self-resonant frequency > 40 GHz) and Passive Plus Inc. 0201BB104KW160 capacitor (self-resonant frequency > 65 GHz) are selected, and the results demonstrate that the output signals are not distorted. Also, in order to prevent ESD damage, a 1-μF capacitor is used as ESD protection and bypass the power supply noise.



(a) (b)

Fig. 11. Integrated driver and MZM: (a) PCB view (b) Chip microscope view.

The EO measurement setup is shown in Fig. 12. The MZM driver input signal is applied with an electrical high speed modulation signal from Antritsu MP1800A pattern generator. The Santec TSL550 and PCU-100 provide tuneable laser source and polarization adjustment before the signal is applied to MZM. The MZM output modulated optical signal is transmitted through Agilent O-band optical filter and GIP Optical Amplifier then directly fed into the Tektronix DSA8300 Sampling Oscilloscope for optical eye diagrams measurements.

Table 2. Comparison of Published Modulator Drivers

Ref.	Technology	Data-Rate (NRZ)	Data-Rate (PAM4)	ER(dB)	Driver output swing(Vpp)	Power(mW)	Efficiency(pJ/bit)
[6]	0.25 µm SiGe BiCMOS	N/A	20 Gbaud/s	N/A	4	1100	27.5
[7]	65 nm CMOS	32 Gb/s	N/A	4.53	4	201	6.28
[8]	28 nm CMOS	22 Gb/s	N/A	4.83	N/A	62.7	2.85
[9]	40 nm CMOS	28 Gb/s	N/A	N/A	4	585	20.89
This Work	65 nm CMOS	25 Gb/s	23 Gbaud/s	5.41/3.78[#]	5/3.8[*]	734	15.96

[#]NRZ 25Gb/s and PAM4 25Gbaud/s; [*]NRZ 30Gb/s and PAM4 25Gbaud/s

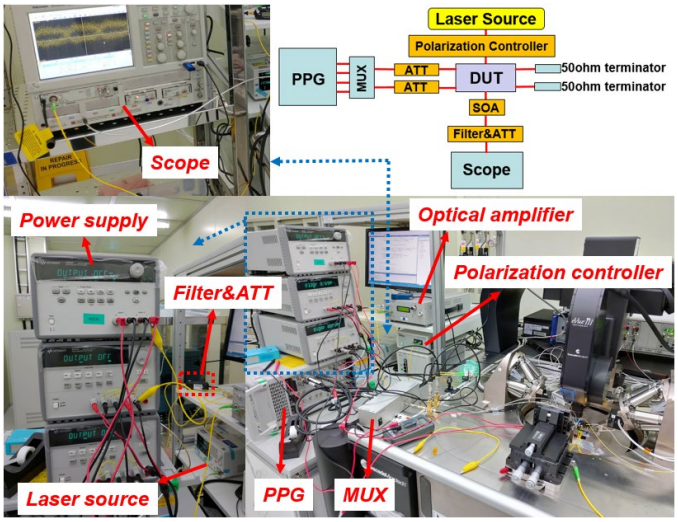
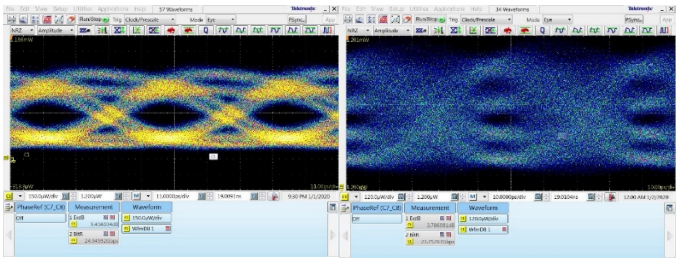


Fig. 12. Electrical-Optical measurement setup.

The NRZ 25Gb/s and PAM4 23Gbaud/s optical-electrical eye diagram are shown in Fig. 13. The achieved extinction ratios are 5.41dB and 3.78dB respectively, and the equivalent data transmission efficiency is 15.96 pJ/bit.



(a) (b)

Fig. 13. Measured optical output eye diagrams: (a)NRZ 25Gb/s (b) PAM4 23 Gbaud/s.

The performance of proposed design are summarized and compared with recently published MZM drivers in Table I. It can be seen that most of the CMOS-based designs did not demonstrate the PAM4 modulation performance. In this paper, we successfully realized a wideband MZM driver which can operate at high speed for both NRZ and PAM4 signal formats. The data rate can reach up to 25 Gb/s and 23 GBaud/s for NRZ and PAM4 with an extinction ratio of 5.41 dB and 3.78 dB, respectively. In addition, the proposed MZM driver can achieve a high transmission efficiency of 15.96pJ/bit.

IV. Conclusion

In this work, a wideband MZM driver was demonstrated using low cost CMOS technology together with the integrated optical modulator and bias network. The optimal design for the tradeoff between breakdown and bandwidth was discussed in the stacked-FET cell in the modulator driver. A different bias scheme was used to achieve significant power efficiency improvement. We integrated CMOS driver, SOI MZM and bias-tee network on the PCB for electrical- optical transmission validation. The measured results showed that a data rate of 25Gb/s with an extinction ratio 5.41 dB can be achieved in the NRZ signal format, while the data rate was up to 23 Gbaud/s with an extinction ratio of 3.78 dB for PAM4 data transmission.

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