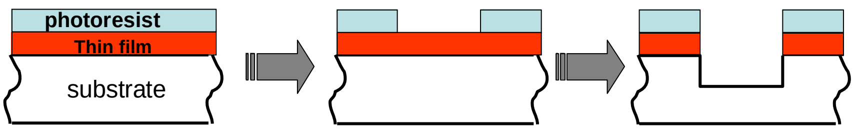
Lecture 2: Micromachining Processes

- Deposition (Additive techniques)
- Pattern Transfer : Optical Lithography
- Etching (Subtractive techniques)
  - » Bulk and Surface Micromachining
  - » Dry and Wet Etching

The Toolbox: Processes for Micromachining

- Some are inherited from IC fabrication (e.g., optical lithography), and some are unique for MEMS only (e.g., wet etching, wafer bonding, deep reactive ion etching (DRIE), etc)



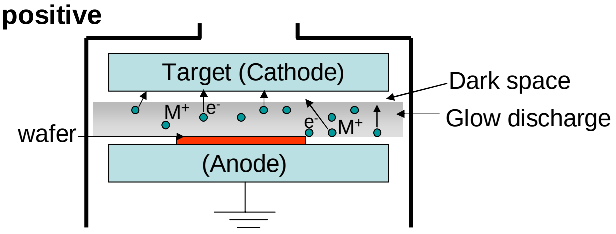
Deposition (additive)
Sputtering
Evaporation
CVD/LPCVD/PECVD
Epitaxy
Oxidation
Spin-on
Plating

Patterning
Optical lithography

Etching (subtractive)
Wet etching
Plasma (dry) etching:
{ Chemical
RIE
DRIE }
Lift-off*

Physical Vapor Deposition (PVD): Sputtering

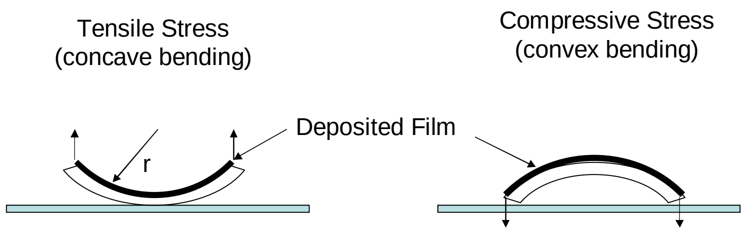
- Physical bombardment of inert ions (Ar, He) into target to "knock out" atoms
  - » Ions accelerated by E field of the dark space
- DC plasma or Radio-Frequency plasma (f = 13.56 MHz)
- Almost any thin films: metal films (Al, Ti, Pt, etc.), amorphous Si, insulators (glass and piezoelectrical ceramics PZT, ZnO)
- Equal # of electrons and ions ⇒ plasma potential is constant, and always most positive



Sputter Step Coverage

- Dependent on temperature, pressure, and DC bias
- Better step coverage and better adhesion to the substrate than Evaporation

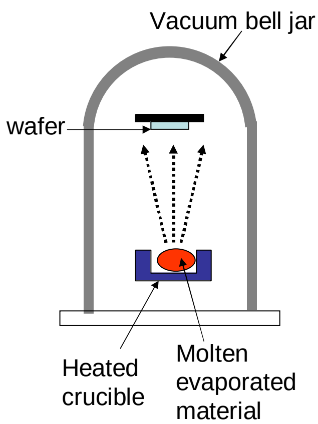
Understand Film Stresses



- Stresses can be extracted from measured radius of curvature (Stoney's equation)
- Undesirable mechanical features
  - » Compressive stress results in "BUCKLING" for clamped-clamped mechanical structures
  - » Stress gradient results in structural CURLING

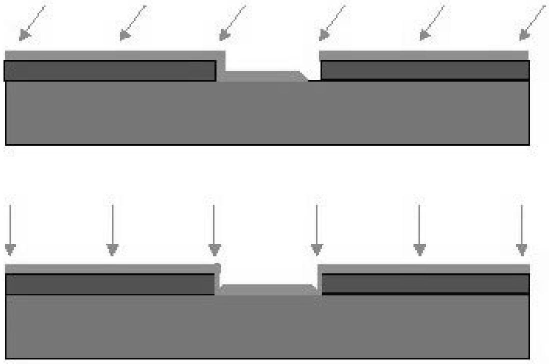
PVD: Evaporation

- Local heating of target material to generate vapor, followed by condensation
- For deposition of nearly any material, including refractory metals
- Techniques
  - » Resistive Heating
    - – Needs good vacuum (10^{-7} to 10^{-6} Torr) to avoid contamination
  - » Electron Beam
    - – Accelerated electrons strikes and melt materials
    - – Better film quality
    - – X-rays produced during strikes (crystal and electronics damages)



Evaporation Film Thickness

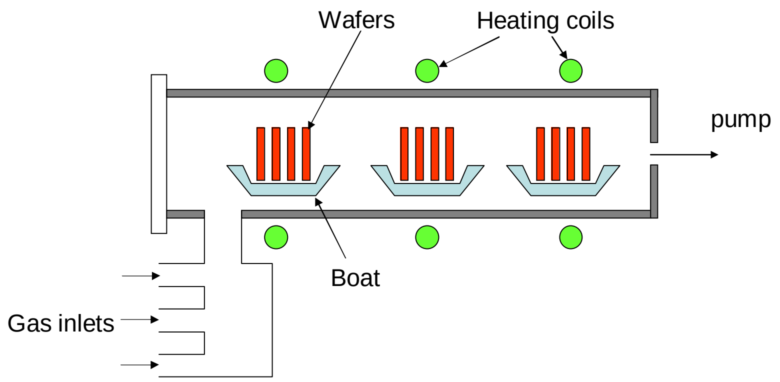
- **Line of sight deposition – POOR STEP COVERAGE**
  - » **Need to rotate substrate to achieve uniform thickness**



Deposition: Chemical Vapor Deposition (CVD)

- **Produces high-quality metal and dielectric films for IC fabrication**
  - » **Polycrystalline film: Polysilicon, tungsten, titanium, copper**
  - » **Amorphous films: silicon oxides and nitrides, low-k dielectrics**
  - » **Chemical reaction**
    - – **Requires heat and mass transfer modeling**
  - » **Relative HIGH temp. (> 300 °C)**
  - » **Types**
    - – **CVD (APCVD): Atmosphere Pressure, 500 – 800 °C**
    - – **LPCVD: Low Pressure, 500 – 800 °C**
      - – **Pyrolytic reaction: thermal breakdown of gases**
    - – **PECVD: Plasma Enhanced deposition rate, ~ 300 °C**
      - – **Compatible with IC metallization**
- **Requires post-deposition anneals to “densify” the CVD films to remove voids**

LPCVD Furnace Tube



CVD Silicon Dioxide

- **Most commonly used dielectric film, can be grown *in situ* (e.g., thermally grown gate oxide) or deposited**
- **Types**
  - » **Phosphorus-doped SiO2 (PSG): good passivation layer**
  - » **Boron-doped SiO2 (BSG)**
  - » **BPSG (Low-Temp. Oxide, LTO): excellent reflow property at low temperature for planarization**
- **Reactions**
  - » **Silane + O_2: $SiH_4 + O_2 \rightarrow \underline{SiO_2} + 2H_2$**
  - » **Tetraethoxysilane (TEOS) decomposition: $Si(OC_2H_5)_4 \rightarrow \underline{SiO_2}$ + by-products**
    - – **Excellent uniformity and step coverage (@650 – 750 °C)**
  - » **$SiCl_2H_2 + 2N_2O \rightarrow \underline{SiO_2} + 2N_2 + 2\ HCl$**
    - – **Less used. Excellent uniformity and step coverage (@~900 °C)**

Oxide Color Chart

- Interference causes colorization of light reflected from thin films; color is dependent on film thickness

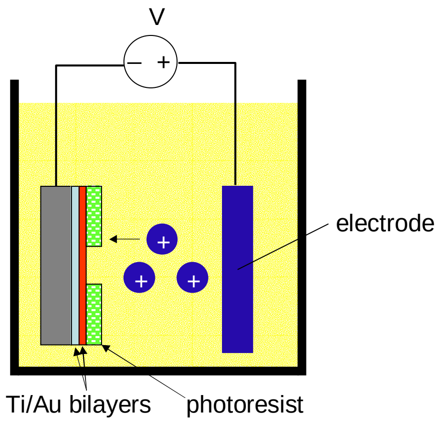
t_{ox} (um)	color	t_{ox} (um)	color
0.05	tan	0.54	yellow green
0.12	royal blue	0.60	pink
0.20	light gold	0.80	orange
0.25	orange	0.89	blue
0.31	blue	1.00	pink
0.34	green	1.10	green
0.39	yellow	1.19	red violet
0.47	violet	1.28	yellow
0.49	blue	1.40	orange
0.52	green	1.50	blue

CVD Polysilicon

- Polysilicon is a popular MEMS structural material, MOSFET gate material, high-value resistor, and conductor (with silicide film)
- Pyrolytic reaction: $SiH_4 \rightarrow Si + 2H_2$
- LPCVD polysilicon (600 – 700 °C) exhibits a crystalline grain structure. PECVD polysilicon is completely amorphous
- Requires annealing @900 °C or above to reduce stress (~50 MPa) for MEMS application

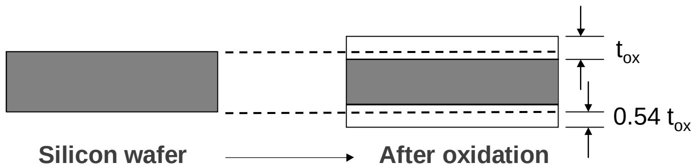
Deposition by Plating

- **Metal ions in solution deposit on conductive surface at negative potential**



Thermal Oxidation of Silicon

- **Highest-quality SiO_2 (e.g., 10 nm gate oxide) is obtained by oxidizing Si in dry O_2**
  - » **Reaction: $Si + O_2 \rightarrow SiO_2$**
- **Wet oxidation is used to make thicker oxides (up to ~1.5 um)**
  - » **Film thickness characterized by Deal-Grove model**
  - » **Reaction: $Si + H_2O \rightarrow SiO_2 + H_2$**
- **46% of grown oxide is below original Si surface**
- **Short times: reaction-rate limited; linear rate**
- **Long times: diffusion limited; parabolic rate**



Deal-Grove Model

- **The final oxide thickness x_f is given by:**

$$x_f = 0.5A_{DG}\left[\sqrt{1+\frac{4B_{DG}}{A_{DG}^{2}}(t+\tau_{DG})}-1\right]$$

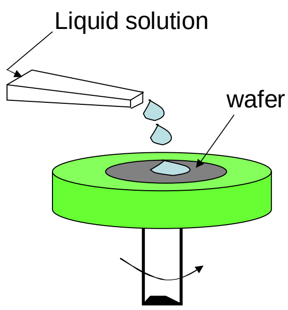
$$\tau_{DG} = \frac{x_i^{2}}{B_{DG}} + \frac{x_i}{\left(B_{DG}/A_{DG}\right)}$$

- **Deal-Grove rate constants for dry oxidation**

Temperature (°C)	A_{DG} (um)	B_{DG} (um/hr)	τ_{DG} (hr)
920	0.235	0.0049	1.4
1000	0.165	0.0117	0.37
1100	0.090	0.0270	0.067

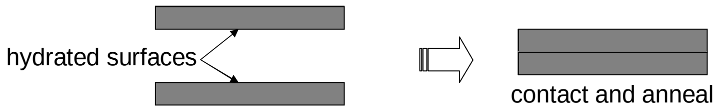
Spin-on Deposition

- **"Spin" and "spread"**
- **Material types**
  - » **Dielectric insulators**
    - – **spin-on glass (SOG) : interlayer dielectric for IC**
  - » **Organic materials**
    - – **Photoresist (PR)**
    - – **Polyimides**
    - – **SU-8 (special thick PR, ~ 100 um)**
    - – **Organic polymer**

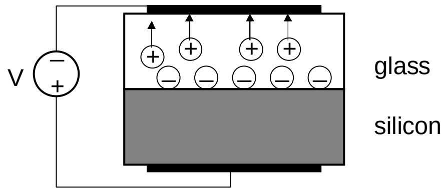


Wafer Bonding

- Silicon Fusion Bonding achieves direct Si-to-Si wafer bonding or with an intermediate oxide layer; hydrated surfaces annealed at 800 to 1000 °C



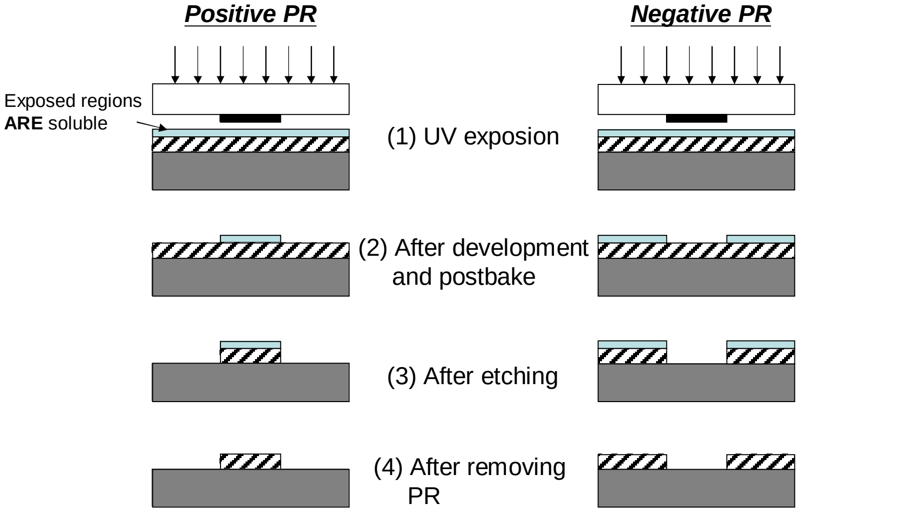
- Anodic Bonding joins together a silicon wafer and sodium-containing glass substrate by electrostatic force



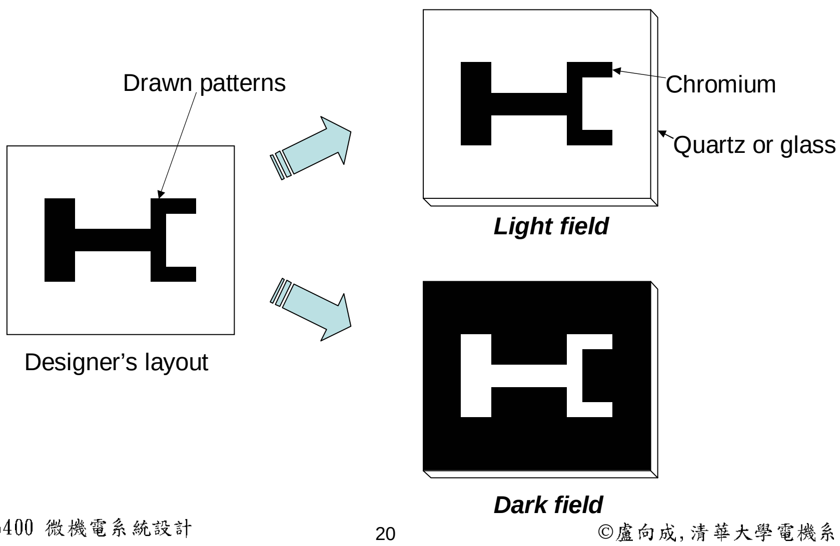
Pattern Transfer: Lithography

- Three major sequential steps:
  - » Application of photoresist (photosensitive material) by spin coating
  - » Optical exposure to print mask image onto the resist
  - » Immersion in an aqueous developer solution to dissolve exposed resist and render desired image
- Light source
  - » Deep UV: λ = 150 to 300 nm
  - » Near UV: g-line λ = 436 nm; i-line λ = 365 nm

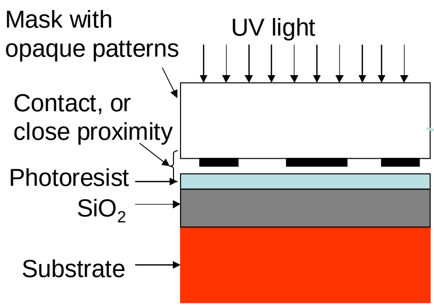
Positive and Negative Photoresists



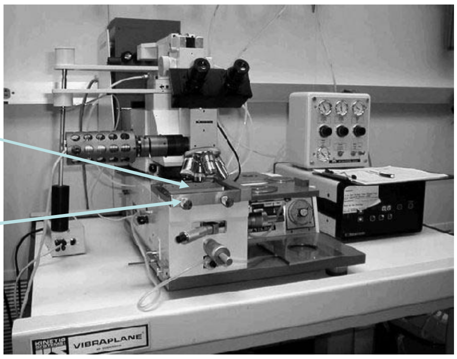
Light-Field and Dark-Field Masks



Contact/Proximity Photolithography



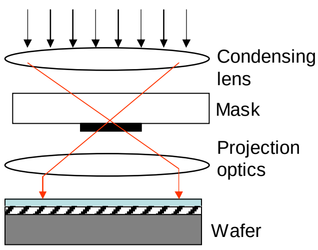
- Mask susceptible to damage and contamination during alignment



Contact aligner

Projection Photolithography

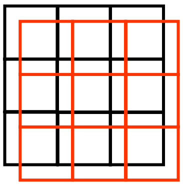
- Mask patterns imaged onto wafers with reduction (5:1 or 10:1)
- Step and repeat pattern
- No mask degradation
- Large mask patterns are easier to make reliably



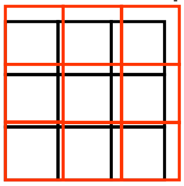
Canon Stepper

Misregistration

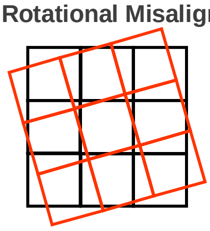
- Translational Misalignment



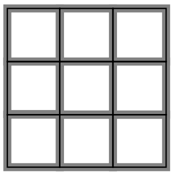
- Mask or wafer expansion



- Rotational Misalignment

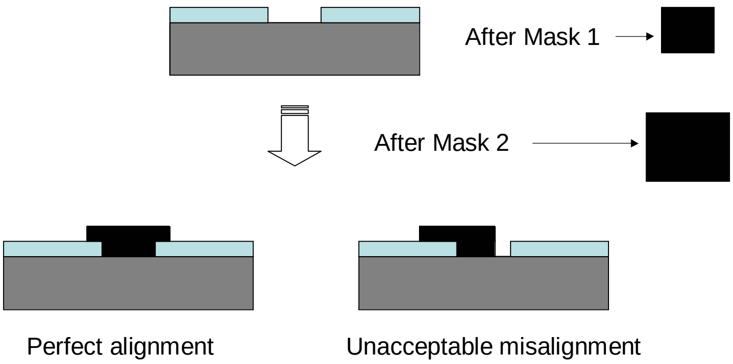


- Etch shift and bloat



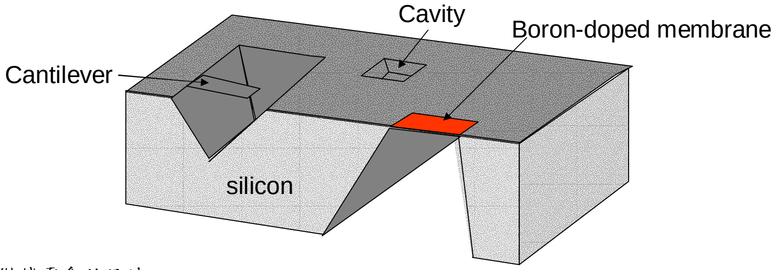
Example: Translational Misalignment

- **Design rules are required to make working devices**



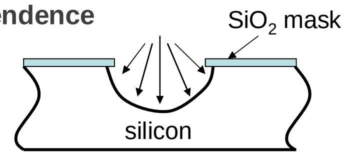
Bulk Silicon Micromachining

- Dates back to a piezo-resistive silicon pressure sensor (Tufte et al., Honeywell, 1962)
- Structures made by etching substrate material (usually Si or glass wafer)
- Membranes for pressure sensors, microphones
- Nozzles for ink-jet printing, drug delivery
- Cantilevers for thermomechanical sensing
- Cavities for microfluidic chambers

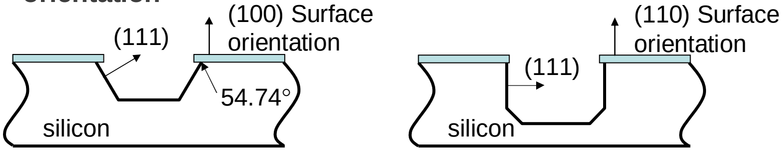


Isotropy of Bulk Silicon Micromachining

- Isotropic etch
  - » No etch dependence

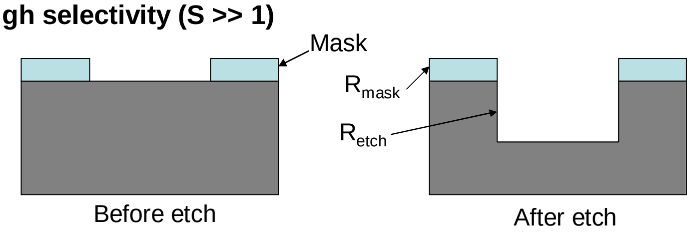


- Anisotropic etch
  - » Etch rate and profile changes with wafer or crystal orientation

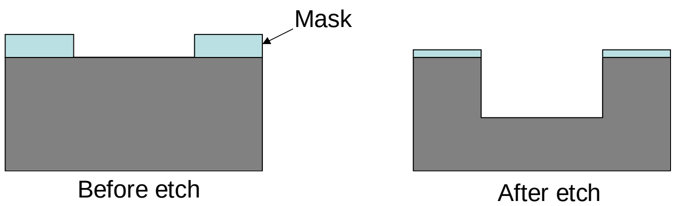


Selectivity

- **Ratio of etch rates: $S = R_{etch}/R_{mask}$**
- **High selectivity ($S >> 1$)**

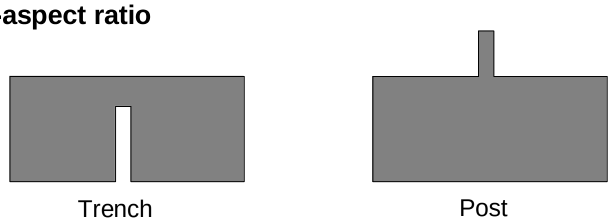


- **Low selectivity**

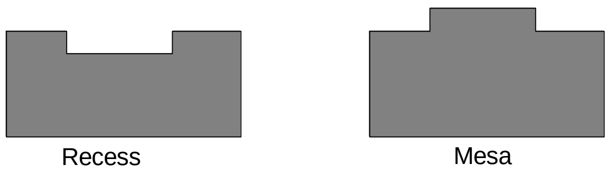


Aspect Ratio

- **High-aspect ratio**

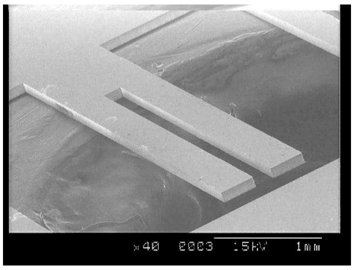


- **Low-aspect ratio (< 1:1)**

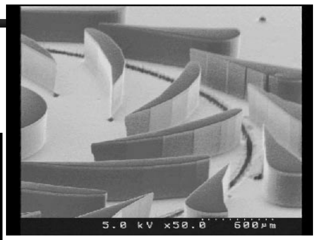


Bulk Micromachining

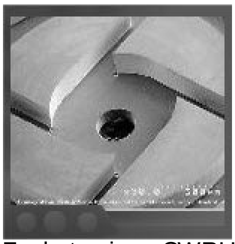
Trenches, STS



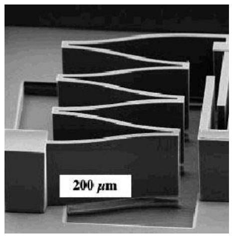
Suspended beam, Tohoku U.



Micro-turbine, Tohoku U.



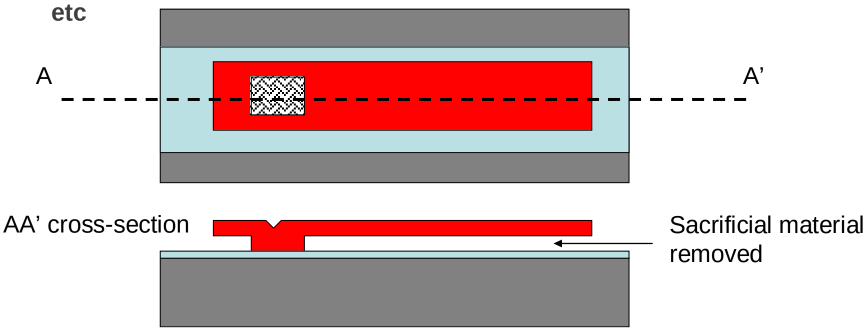
Fuel atomiser, CWRU



spring, Klassen et al., 1995

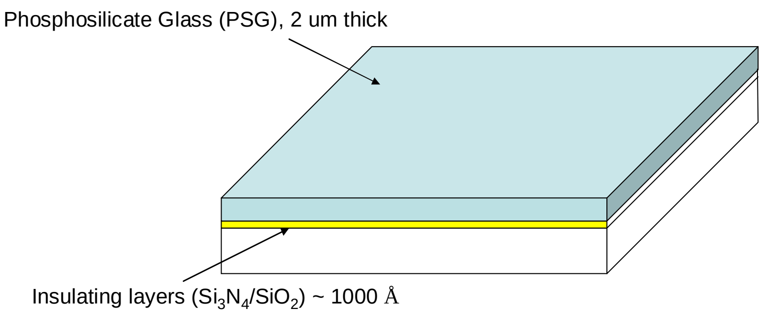
Surface Micromachining

- **Structures are made by a sequence of deposition and patterning of thin films (usually < 10 um), followed by removing the SACRIFICIAL material for structural release**
  - » **More commonly used in IC fabrication than bulk micromachining**
  - » **Key issues: deposition temperature, intrinsic stress, step coverage, etc**



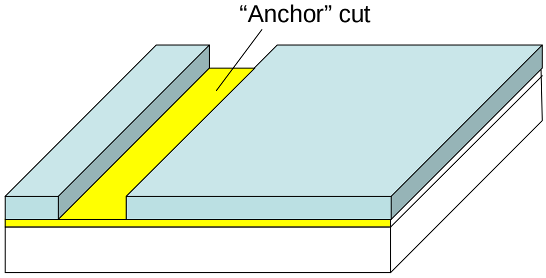
Surface Micromachining

- Many processes; common one used produces polysilicon microstructures
- Starts with deposition of insulating layers and sacrificial material



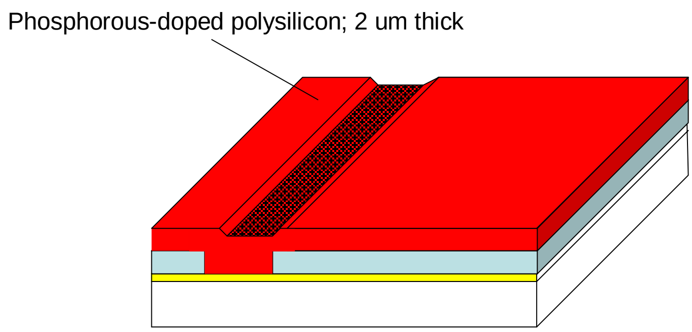
Surface Micromachining

- Selected regions of sacrificial material are patterned and removed (etched)
- Regions serve as anchor areas for succeeding structural material deposition



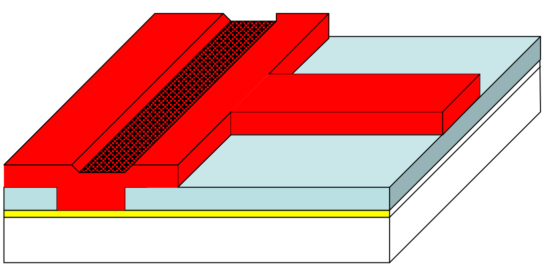
Surface Micromachining

- Deposition of structural material



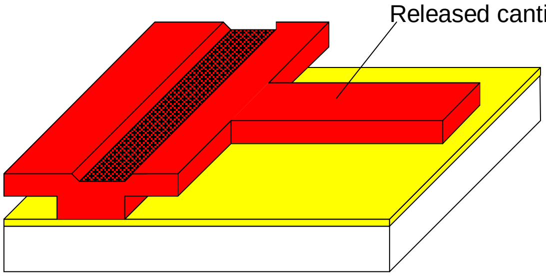
Surface Micromachining

- Structural material is patterned and etched to create desired microstructures
- Underlying sacrificial layer is exposed



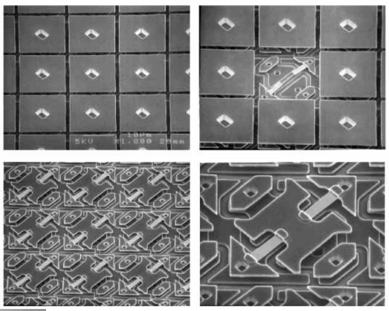
Surface Micromachining

- **Buffered hydrofluoric (HF) acid etches sacrificial material, releasing microstructure**

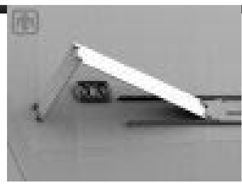


Surface Micromachining

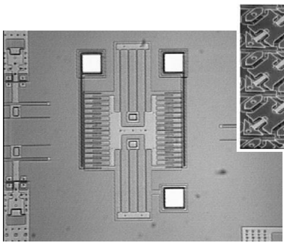
Gear (Sandia Lab)



Micro-mirrors for projection display (Texas Instrument)



3D mirror (Sandia Lab)



Micro-resonator

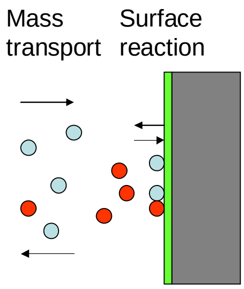
Optical mirror switch (Lucent)

Material Removal

- Wet chemical etching
- Dry etching
  - » Chemical etching
  - » Ion milling
  - » Plasma etching
  - » Reactive-ion etching
- Lift off

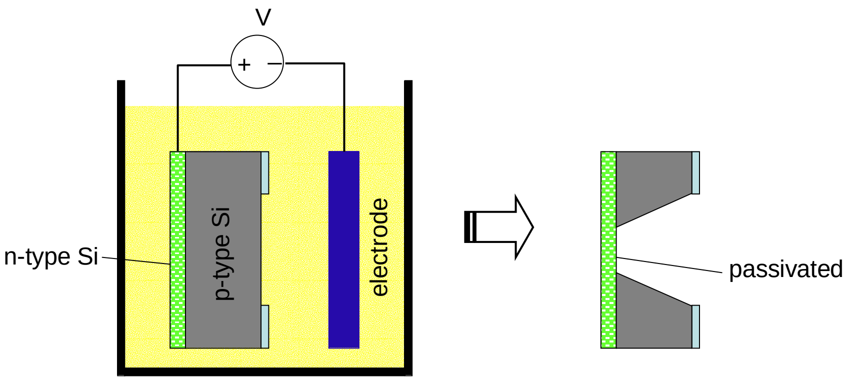
Wet etching

- Etching mechanism
  - » Reactant transport from etchant solution to surface
  - » Surface reaction
  - » Transport of etch products from surface into solution
- Reaction rate limits:
  - » Mass transport is diffusion limited ⇒ etch rate increased by agitation
  - » Surface reaction is rate limited ⇒ etch rate increased by increasing temperature



Etch Stop

- To achieve uniform and controlled depths for bulk silicon wet etching
- Electrochemical technique: wet etch stops on a passivated n-type epitaxial layer when exposed



Other Etch Stop Techniques

- Dielectric Etch Stop
  - » The Si etching stops on a dielectric layer (e.g., silicon nitride) to produce a dielectric diaphragm
- P^+ Etch Stop with a heavily boron doped layer
  - » Selectivity not as high as for passivating oxides
  - » Residual stress due to doped layer
  - » Not likely to diffuse piezo-resistors into heavily-doped p+ silicon

Dry Etching

- **Chemical Etching**
  - » **Chemical reaction**

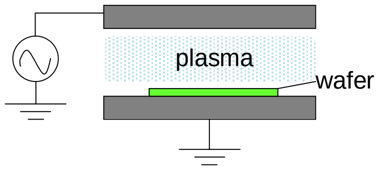
- **Plasma-Assisted Etching**
  - » **Ion milling: physical sputtering**
  - » **Plasma etching: energetic chemical reaction**
  - » **Reactive-ion etching (RIE): physically assisted chemical reaction**
  - » **Deep RIE**

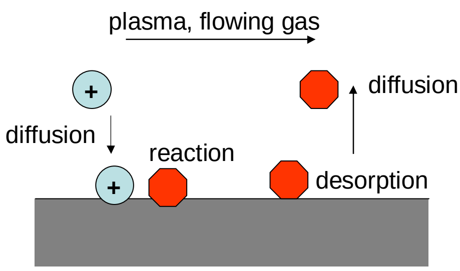
Dry XeF_2 Chemical Etching

- **Vapor phase XeF_2 (Xenon difluoride) etch of Si:**
  - » **$2XeF_2 + Si \rightarrow 2Xe + SiF_4$**
- **Isotropic**
- **Excellent selectivity over photoresist, oxide, aluminum, and nitride**
- **Can make CMOS-integrated MEMS devices with aluminum as mask to undercut silicon**
- **Ideal for dry release of surface micromachined devices if polysilicon is the sacrificial material**

Plasma Etching

- **Disassociated gas radicals in the plasma are responsible for etching**
- **Wafer on grounded electrode**
- **Reacted material is pumped out of the chamber**
- **O_2 plasma + photoresist → CO_2 + H_2O (called "Ashing")**
- **0.1 to 10 torr operating pressure**



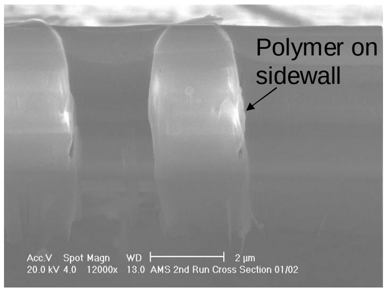


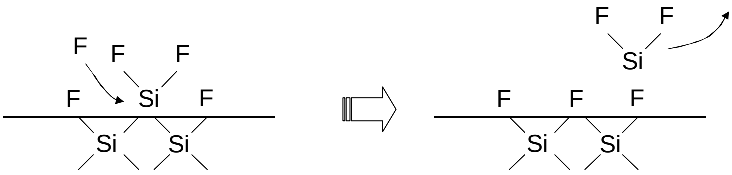
Plasma Etch Chemistry

- **Silicon**
  - » $CF_4 + O_2$, $SF_6 + O_2$, CCl_4 (for polysilicon)
- **Silicon dioxide**
  - » $CF_4 + H_2$, CHF_3
- **Silicon nitride**
  - » $CF_4 + O_2$, CHF_3 , SF_6
- **Aluminum**
  - » BCl_3, CCl_4
- **Organics**
  - » O_2, $O_2 + CF_4$, $O_2 + SF_6$

Reactive-Ion Etch

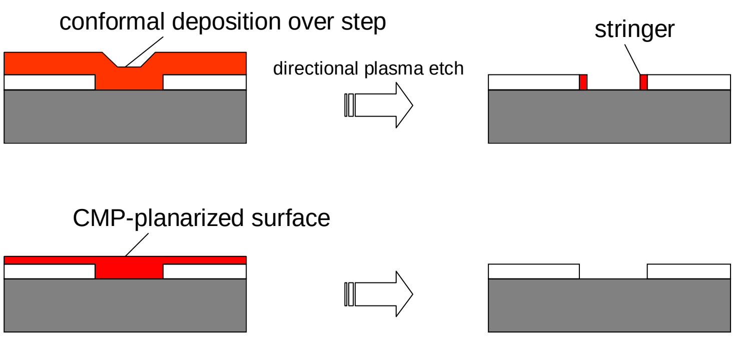
- Good directionality is achieved by operating at low pressure (10^{-3} to 10^{-1} torr) to generate relatively higher energy ions perpendicular to wafer
- Creates polymeric species by chemical cross-linking
- Wafer on powered electrode
- Fluorocarbon etching of Si: gas phase products formed





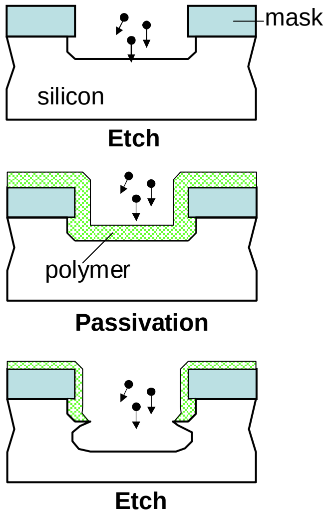
Unwanted Etched Feature: Stringer

- Can be removed by planarization of uneven topography using
  - » Chemomechanical Polishing (CMP)
  - » Resist Etchback
  - » Planarization with Polymers (e.g., polyimides, SU-8)



Deep Reactive Ion Etch

- Inspired from polymer produced in RIE
- Patent 4455017, 4784720 by Robert Bosch GmbH, of Stuttgart, Germany
- Rapid cycling between ETCH and PASSIVATION and high-density plasma to achieve very high aspect ratio microstructures
  - » ETCH: $SF_6 + O_2$ plasma
  - » PASSIVATION: C_4H_8 to produce a fluorocarbon polymer for sidewall protection
- Sidewall scalloping: less than 50 nm roughness can be achieved



Wet versus Dry Etching

- Wet Etching
  - » Excellent selectivity
  - » Etching isotropic or can stop at crystal planes
  - » Inexpensive
  - » Fast
  - » Poor dimension control
  - » Hard to make repeatable
  - » Surface tension upon removal of sacrificial material can cause sticking
- Dry Etching
  - » Can etch directionally
  - » Expensive equipment
  - » Relatively slow
  - » Excellent dimension control
  - » Repeatable
  - » No rinsing or drying steps

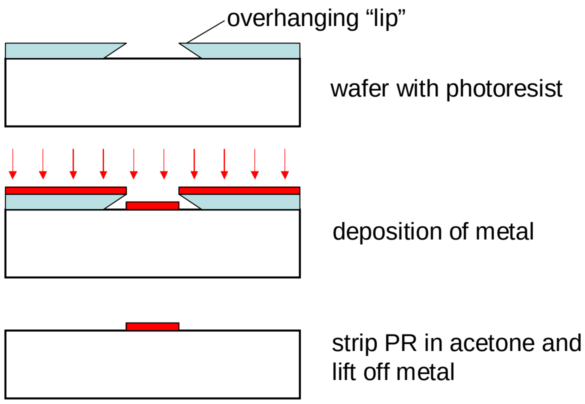
Comparison of Silicon Etchants*

	HNA (HF + HNO3 + acetic acid	Alkali-OH	EDP (ethylene diamine pyrochatechol	TMAH (tetramethyla mmonium hydroxide	XeF_2	SF_6 plasma	DRIE
Type	Wet	Wet	Wet	Wet	Dry	Dry	Dry
Anisotropic	No	Yes	Yes	Yes	No	Varies	Yes
Si etch rate (μm/min)	1 to 3	1 to 2	1 to 30	~ 1	1 to 3	~ 1	> 1
Oxide mask (nm/min)	10 to 30	1 to 10	1 to 80	~ 1	Low	Low	low
P^{++} etch stop?	No	Yes	Yes	Yes	No	No	No
CMOS compatible?	No	No	Yes	Yes	Yes	Yes	Yes
Si roughness	Low	Low	Low	Varies	High	Varies	low

***William and Muller, "Etch rate for micromachining processes", J. MEMS, 1996**

Lift Off

- **Used with metals that are difficult to etch with plasmas**
- **Typically photoresist is soaked in chlorobenzene to form an overhanging "lip" to form discontinuous metal layer**



Spindt Process

- **A modified lift-off process to create sharp tips for data storage and field-emission display**