A CMOS Micromachined Capacitive Tactile Sensor With High-Frequency Output

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***Abstract*—This paper describes the design and characterization of a CMOS-micromachined tactile sensing device that can be utilized for fingerprint recognition. The complete post micromachining steps are performed at die level without resorting to a wafer-level process, providing a low-cost solution for production. The micromechanical structure has an area of 200 μm by 200 μm and an initial sensing capacitance of 153 fF. An oscillator circuit is used to convert the pressure induced capacitance change to a shift in output frequency. The circuit has a measured initial frequency at 49.5 MHz under no applied force. The total frequency shift is 14 MHz with a corresponding mechanical displacement of 0.56 μm and a capacitance change of 63 fF, averaging a capacitive sensitivity of 222 kHz/fF. The measured spring constant is 923 N/m, producing a force sensitivity of 27.1 $\mathrm{kHz}/\mu\mathrm{N}$. [1694]**

***Index Terms*—Astable oscillator, capacitive sensor, complementary–metal–oxide semiconductor (CMOS) microelectromechanical systems (MEMS).**

I. Introduction

FINGERPRINT recognition has many possible applications, such as access control for buildings and computers, among others. A typical fingerprint sensor uses an optical measurement as its basis, where the finger surface is illuminated by visible light and photographed, and the image then stored for subsequent identification [1], [2]. However, optical sensing may be affected by stained fingers, and an optical sensor may not be sufficiently sensitive to differences between a printed image of a fingerprint and a true live fingerprint. In addition, optical sensors may be bulky and susceptible to malfunction under shock and vibration.

In the past few years, semiconductor-type fingerprint sensors have provided a low-cost solution for miniaturization and have shown a better immunity against vibration, making them suitable for mobile applications. For example, the thermal sensing technology developed by ATMEL [3] measures the temperature difference between areas on the sensor in which skin contact is achieved (a ridge) and areas in which it is not (a valley). The chip is made of a silicon die covered by a pyroelectric material, which transforms the temperature difference (not the absolute temperature) into electric charges. The CMOS micromachined fingerprint sensor, reported on by Charlot [4], consists of an array of micro cantilevers with a polysilicon layer inserted for piezoresistive sensing. An anisotropic silicon etch was performed by TMAH at chip level for structural release. However, piezoresistive coefficients of polysilicon are sensitive to operating temperature, and their dependency on doping concentration and crystal orientation can produce varying results between runs.

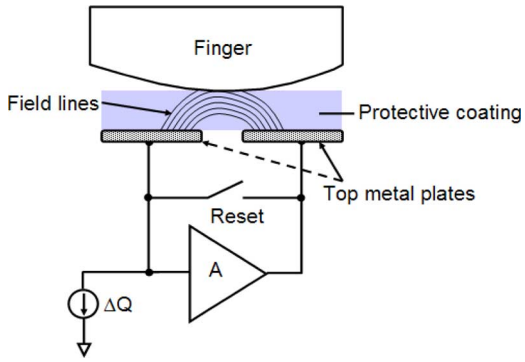

Fig. 1. Schematic of one pixel cell of the capacitive fingerprint sensor by STMicroelectronics [8].

Many other integrated solid-state fingerprint sensors adopt the capacitive sensing mechanism [5]–[14], for which two main approaches have been proposed. The first approach [5]–[10] requires only a few additional steps following the conventional integrated circuit fabrication, such as the addition of a protective coating for finger contact. Sensing capacitances are formed between the fingerprint and the closely spaced electrodes beneath the protective layer. In some cases, the detection process is sensitive to finger surface conditions, such as electric charges accumulating on a dry finger. The schematic in Fig. 1 illustrates the working principle of the fingerprint sensor by STMicroelectronics, Inc. [8]. Each sensor pixel contains a capacitive feedback circuit whose effective feedback capacitance is modulated by the presence of the live skin close to the surface of the sensor. When live skin is brought in close proximity to the two metal sensing plates, the skin interferes with field lines between the two plates and reduces the effective capacitance between them, resulting in a minimized capacitance for a fingerprint ridge and a maximized capacitance for a fingerprint valley.

The fingerprint sensor patented by Philips [9] includes an array of sensing electrodes, and active addressing of the electrodes is achieved by a switching device (e.g., a thin film transistor) associated with each electrode. A sensing capacitor is formed by each electrode in combination with the covering dielectric material and the overlying finger surface which is set

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at ground potential. By applying a potential to an addressed electrode, the charging characteristic of a sensing capacitor can be measured by a sensing circuit. One concern associated with driving the array of closely spaced electrodes is the capacitive crosstalk from adjacent electrodes. To effectively reduce the crosstalk, AuthenTec, Inc., developed a z-axis anisotropic dielectric layer to focus the electric field at each of the sensing electrodes [10]. Small radio-frequency (RF) excitation signals are applied by the RF electronics imaging mechanism to the live, highly conductive layer of skin that lies beneath the skin's dry outer surface layer. This mechanism is claimed to be capable of acquiring fingerprints under most surface conditions.

The second approach [11]–[14] uses the mechanical displacement between the movable and fixed electrodes for capacitive detection, resulting in a better immunity against charges on a finger than the first method. Monolithic integration of micromechanical structures with sensing circuits is necessary to promote the signal-to-noise ratio, which is otherwise negatively impacted by parasitic capacitances in a two-chip solution. For example, Sato [11] performed successive micromachining steps on a 0.5-μm 3-metal CMOS wafer to achieve a pressure-sensing membrane.

To avoid the high investment cost associated with accessing a whole CMOS wafer, we provide in this paper a convenient micromachining process that can be performed at die level [14]. The materials that make up the micromechanical structure can directly utilize those already available in a conventional CMOS process. The design and characterization of a capacitive sensing pixel will be presented to demonstrate the capabilities of this approach in making integrated fingerprint sensors.

The rest of the paper is organized as follows. The post CMOS micromachining process is introduced in Section II, followed by the design of the capacitive sensor in Section III. Experimental results are presented in Section IV, followed by discussions and conclusions in Section V.

II. Device Fabrication

The TSMC 0.35-μm two-polysilicon four-metal (2P4M) CMOS process is used for sensor fabrication. The post micromachining steps are performed on a CMOS die. The process flow in Fig. 2 shows the development of a released microstructure in cross section. After completion of the CMOS foundry process, most of the die area, including the bond pads, is covered by the top passivation layer except for the openings beside the structure that are intended for subsequent etching. As shown in Fig. 2(b), we perform a sacrificial wet etch of stacked metal (aluminum) and via (tungsten) layers through the openings by using a mixed H_2SO_4/H_2O_2 (2:1) etchant, with the dielectric layers for etch protection. The solution is constantly heated at 85°C, while H_2O_2 is replenished every 20 minutes to maintain the etching rate. The top and bottom electrodes for capacitive sensing are formed afterwards when the sacrificial metal-3 layer is removed. To avoid stiction due to liquid remaining between the movable and fixed electrodes, the die is immersed in isopropyl alcohol (IPA) for 30 min, followed by a hotplate bake at 90 °C for five minutes. To remove the passivation remaining on bond pads, a reactive ion etch using the CHF_3/O_2 plasma (100 sccm: 5 sccm) is performed as shown in Fig. 2(c). An overhanging thin Teflon tape (durable up to 260 °C) is used to cover the sensor area.

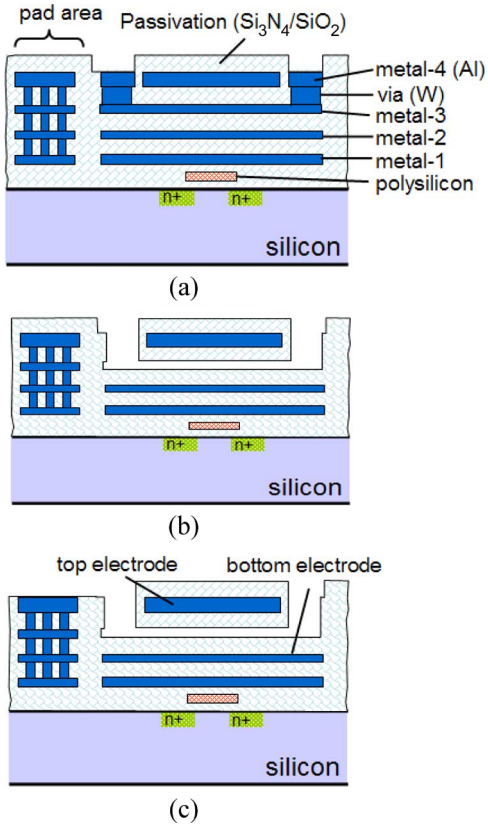

Fig. 2. Post-CMOS micromachining steps: (a) after completion of CMOS, (b) sacrificial metal etch for structural release, and (c) removal of passivation on top of bond pads.

According to the processing steps, the shape of the suspended microstructure is defined by the passivation openings. The use of large-size vias for the sacrificial metal etch is against foundry design rules but acceptable for fabrication. The separation between the suspended plate and the bottom is about 0.64 μm of the metal-3. The passivation on top of CMOS becomes part of the suspended plate. It consists of Si_3N_4 and SiO_2 with a total thickness of about 1.4 μm. These dielectric layers are to remain on top for protection and electrical isolation during finger contact.

To characterize the sacrificial metal etching process shown in Fig. 2(b), we have measured different sacrificial metal layers and opening sizes through a series of test keys. One set of the channel structures after etch is shown in Fig. 3. The results indicate that the etching rates of tungsten via and aluminum layer are around 0.04 μm/min and 1.5 μm/min, respectively.

III. Capacitive Sensor Design

A. Mechanical Design

The released microstructure shown in Fig. 4 is doubly clamped with four support beams connected to anchors. The 150-μm-diameter circular plate consists of multiple dielectric and metal layers, giving a total thickness of about 3.3 μm. Most of the support beams are made up of the passivation (Si_3N_4/SiO_2) and the dielectric layer between the metal-4 and metal-3, except for one beam that must have a metal-4 line running through to connect the top electrode to the sensing circuit. The all-dielectric composition in the support beams is

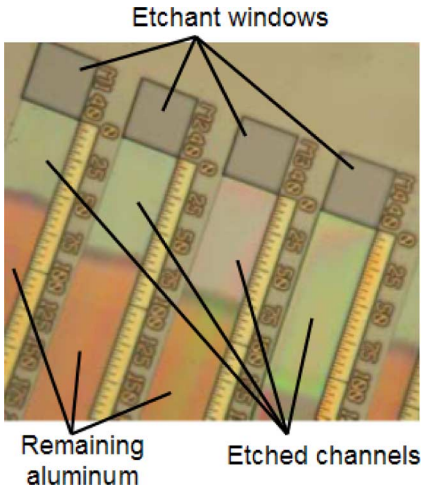

Fig. 3. Micrograph of etched test structures using different sacrificial metal layers. From left to right: metal-1, metal-2, metal-3, and metal-4.

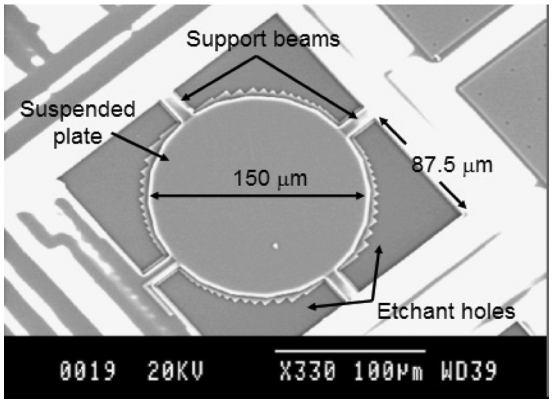

Fig. 4. SEM of the fabricated tactile sensor.

meant to have a more uniform stress distribution in the beam cross section.

The doubly clamped structure is preferred over the cantilever structure in achieving a uniform gap between the two opposing sensing electrodes when producing a sensor array. A large curl variation is expected for cantilever structures since the residual stress and stress gradient vary between locations on a die [15]. The drawback of a doubly clamped structure is that the stiffness can still be affected by residual stress, just as tensile stress tends to increase the stiffness, for instance [16]. The compressive dielectric films that make up most of the structure are expected to reduce the stiffness, as will be demonstrated through experimental characterization. In order to avoid the out-of-plane buckling caused by the compressive stress and to ensure a proper structural release, short support beams of 25 μm by 10 μm are used in the design.

The out-of-plane spring constant of the suspended structure is an important parameter in calculating the measured sensitivity in terms of the applied force. Since the mechanical structure can not be represented analytically through a partial differential equation as that for a square membrane [17], we resort to finite-element simulation [18] to calculate the spring constant. The Young's modulus of aluminum, silicon dioxide, and silicon nitride are set to values of 70, 75, and 210 GPa in simulation,

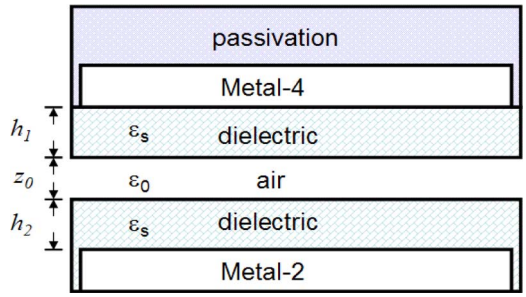

Fig. 5. Sideview of the sensing capacitance.

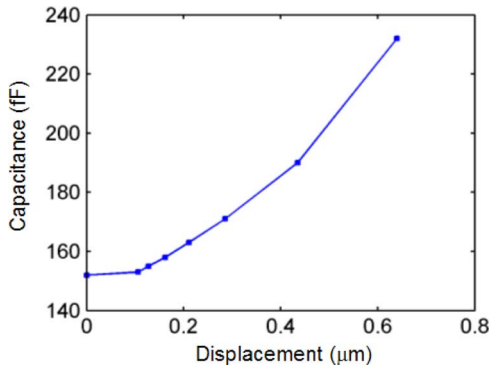

Fig. 6. Relationship of the sensing capacitance with respect to the plate displacement at center.

respectively. The film stresses are set to zero due to the lack of data from the CMOS foundry. The spring constant from simulation is 1876 N/m, obtained as the ratio of an applied pointed force at the center of the plate over the associated displacement. A concentrated load is used instead of a uniform pressure because the force-displacement relationship is to be verified by a nano-indenter experiment, in which the pointed load is applied by a controlled tip with a radius of less than 0.1 μm.

The top and bottom sensing electrodes shown in Fig. 5 are the metal-4 and metal-2 layers in the 2P4M CMOS process. The capacitor consists of an air gap and two dielectric layers on the electrodes. The latter provides electrical insulation when the two electrodes touch each other. The initial sensing capacitance is expressed as

$$C_0 = \frac{\varepsilon_0 A}{(h_1 + h_2)\frac{\varepsilon_0}{\varepsilon_s} + z_0} \tag{1}$$

where ε_0 is the permittivity of air, ε_s is the permittivity of silicon dioxide, A is the electrode area, h_i is the dielectric thickness ($h_1 = h_2 = 1\,\mu$m), and z_0 is the initial gap separation. The total sensing capacitance under a load can be obtained by performing a two-dimensional integration when the displacements associated with each point on the movable electrode are known. The relationship between the capacitance and the plate displacement at center in Fig. 6 is obtained by finite-element simulation [19]. The capacitance increases from an initial from 153 to 232 fF for a displacement of 0.64 μm.

By using a 2P4M CMOS process, the metal layers selected for sensing can be determined by requirements for maximizing the sensitivity or the measurable range. For the former, the design can follow the case in Fig. 2 to produce a minimum gap; for the latter, the metal-4 and the polysilicon layers can be used as the

top and bottom electrodes, with the sacrificial etch removing the thick stacked layers formed from the metal-3 down to the metal-1. The air gap created in this case is close to 3.9 μm. The associated drawback is that the sensing circuit can not be placed below the mechanical structure because no metal layer is left for routing. It is thus conceivable that a CMOS process with more metallization layers can provide more design options.

B. Capacitive Sensing Circuit

The design of circuit topology for capacitive detection can choose among commonly used schemes, including continuous-time voltage sensing [20], continuous-time current sensing [21], switched-capacitor circuit [22], and capacitance-to-frequency conversion using oscillators [23]–[26]. The capacitance-to-frequency conversion is used to allow a simple circuit design occupying a small area; in addition, by taking advantage of the fast electronics provided by the advanced CMOS process, an oscillator can be outfitted with a high frequency output, which is beneficial in enhancing the capacitive sensitivity of the sensor.

An astable oscillator [27], as shown schematically in Fig. 7(a), is used to detect the capacitance change with respect to the plate displacement by observing the shift in its output frequency. The circuit, as shown, consists of four inverters, one resistor, and the sensing capacitor. The oscillation is produced through self excitation and without any added external signals, aside from the power supply. To illustrate this point, the ideal waveforms of the oscillator at important nodes are depicted in Fig. 7(b) and explained as follows: for $0 \leq t \leq T_1$ when v_a and v_c are logic high and v_b is logic low, v_a is discharged at an exponential rate from the high to the low logic level, according to a time constant determined by the resistor and the capacitor. The high and low logic levels of v_a depend on the transistor sizes in the circuit, and can be designed close to V_{DD} and zero, respectively, as shown in Fig. 7(b). The waveform of v_a can be expressed through the relation

$$v_a(t) = V_{DD} e^{-t/RC}. \tag{2}$$

Logic switches of v_b and v_c occur when the voltage v_a drops to the threshold voltage V_{th}. Then the transient response of v_c from its high to low level causes the voltage v_a to be pulled down to its low level, with an instantaneous current source provided by the inverter on the left. This instantaneous current is ac-coupled between the gate and source of the transistor in the inverter, and flows through the source-substrate diode. By neglecting the transient of v_a from V_{th} to its low logic level, the time T_1 shown in Fig. 7(b) is calculated as

$$T_1 = RC \cdot ln\left(\frac{V_{DD}}{V_{th}}\right). \tag{3}$$

Similarly in the next half cycle for $T_1 \leq t \leq T_2$, when v_a and v_c are logic low and v_b is logic high, v_a rises exponentially from the low to the high logic level by the same time constant as expressed by

$$v_a(t) = V_{DD}(1 - e^{-t/RC}). \tag{4}$$

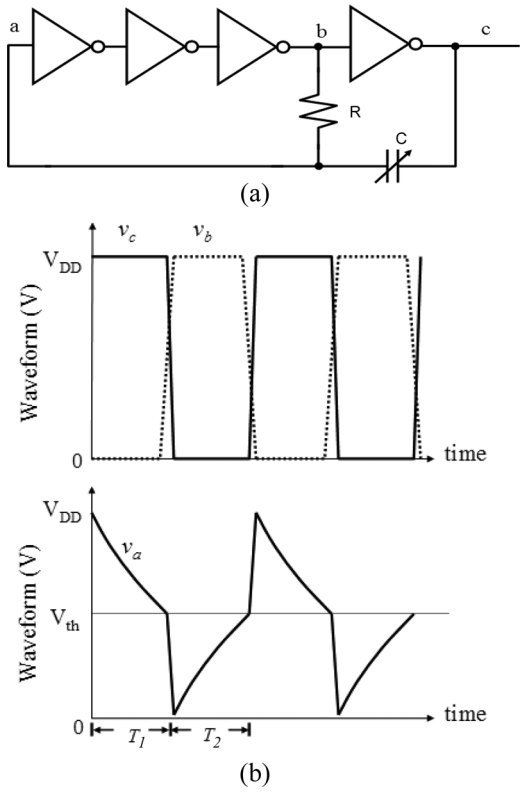

Fig. 7. (a) Schematic of the astable circuit with the sensing capacitance C. (b) Ideal waveforms at points a, b, and c.

The time T_2 required for v_a to reach V_{th} is calculated as

$$T_2 = RC \cdot ln\left(\frac{V_{DD}}{V_{DD} - V_{th}}\right). \tag{5}$$

The total period of the oscillation is the sum of T_1 and T_2 given by

$$T = T_1 + T_2 = RC \cdot ln\left[\frac{V_{DD}^2}{V_{th}(V_{DD} - V_{th})}\right]. \tag{6}$$

The complete circuit schematic shown in Fig. 8 includes two more inverters in the output stage. The first inverter should have a smaller input capacitance to lessen the capacitive loading at the original circuit output. The HSPICE simulation shows that the astable circuit with the predicted sensing capacitance does not produce oscillations for resistor values less than 10 kΩ. We therefore pick a resistor value of 30 kΩ, which is produced by the polysilicon resistor (50 Ω/sq,) provided by the process. The output frequency of the oscillator with a capacitance of 153 fF is 59.2 MHz by HSPICE simulation. The sensing circuit has a total area of 130 μm by 40 μm.

IV. Experiment

The out-of-plane spring constant of the suspended plate was measured after release using a MTS Nanoindenter, in which a controlled diamond tip applied a continuous load to the center of the microstructure. The relationship between the force and the

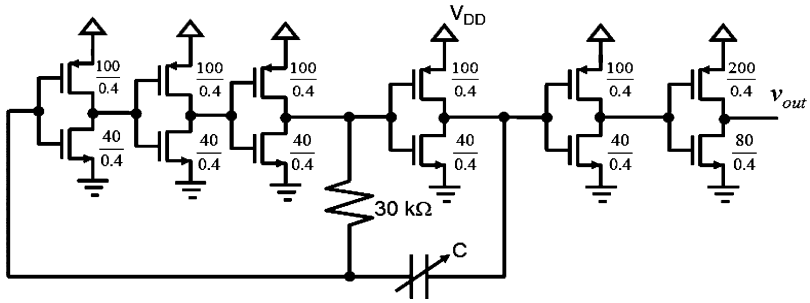

Fig. 8. Complete CMOS circuit design with labeled transistor sizes (unit $= \mu$m).

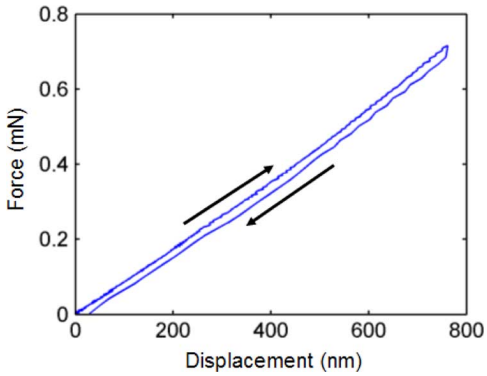

Fig. 9. The measured force-displacement curve by a MTS Nanoindenter.

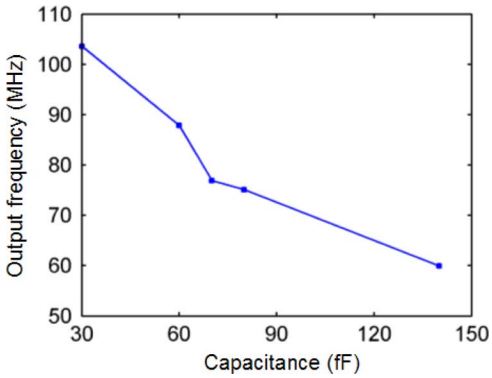

Fig. 11. Relationship of the measured output frequency with respect to the capacitance values in the test circuits.

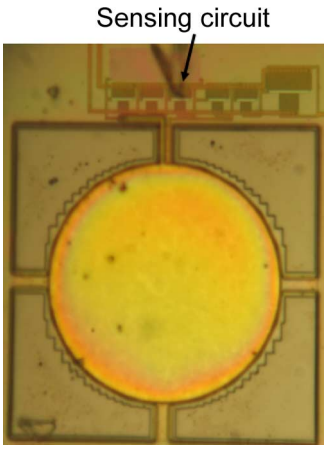

Fig. 10. Micrograph of the suspended plate and the associated sensing circuit.

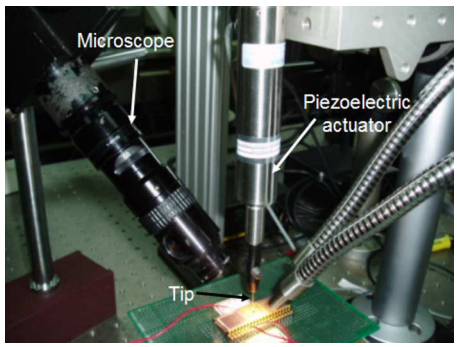

Fig. 12. Test setup for measuring the oscillator waveform with respect to the plate displacement. A tip is moved by a piezoelectric actuator to produce the desired displacement.

associated displacement is plotted in Fig. 9, which shows a measured spring constant of 923 N/m in the elastic operation range. The small hysteresis is due to the plastic deformation caused by penetration of the measuring tip into the suspended plate as it touches the bottom. The measured spring constant in this region is therefore higher than the value in the elastic region. The measured value is smaller than the value acquired through finite element simulation. This discrepancy can be attributed to the variation in film thickness, as well as the residual stresses that are not considered in the simulation due to lack of information.

The micrograph of the sensing device in Fig. 10 shows that the sensing circuit is placed beside the microstructure. It can be placed beneath the microstructure using the metal-1 and polysilicon layers for routing purposes in the design. A series of measurements on output frequency was performed on five test circuits which have different fixed capacitances ranging from 30 to 140 fF, produced by the double polysilicon layers provided by the process. The resistor value in the test circuits is 30 kΩ, same as the value used in the sensor. The measured frequencies with respect to the capacitance values in Fig. 11 show that the highest and lowest frequencies are 103.6 and 60 MHz, respectively. Since our sensor design has a sensing capacitance of 153 fF, which is greater than those used in test circuits, the result indicates the possibility that a mechanical design of smaller size can also function properly.

The experimental setup for measuring the circuit output of the sensor with respect to the applied load is shown in Fig. 12, where a sharp tip was moved by a piezoelectric actuator to give a desired displacement. The measured output response under no applied load is shown in Fig. 13(a). Its corresponding spectrum measurement in Fig. 13(b) indicates the resonant peak occurs at

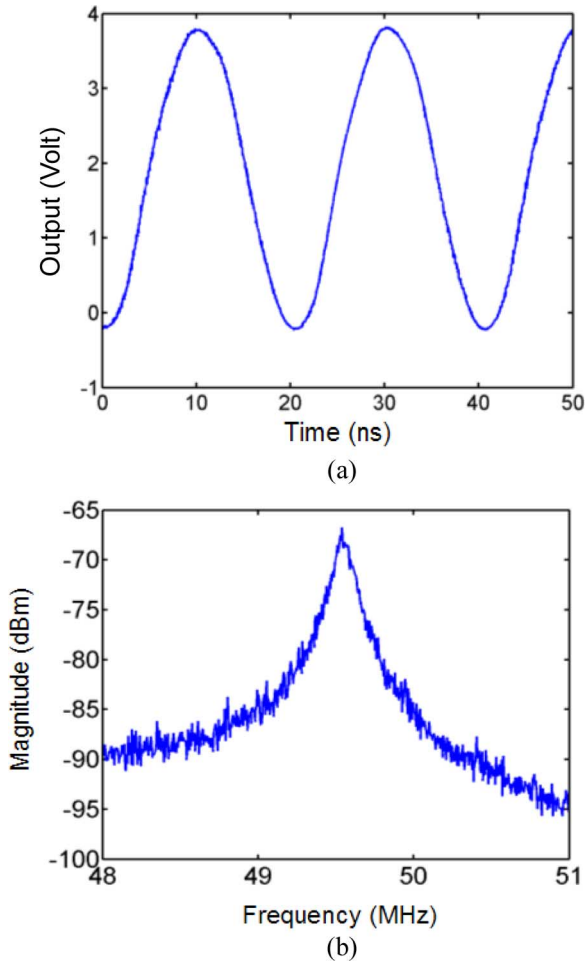

Fig. 13. Measured transient response (a) and spectral output (b) from the oscillator circuit with no applied load.

49.5 MHz, which is less than the simulated value of 59.2 MHz. Fig. 13(a) shows that the waveform, after reaching the steady-state logic values, produces overshoots that exceed the supplied voltages (3.3 and 0 V). This phenomenon can be attributed to the underdamped poles produced by the load impedance in combination with the MOS transistor. In analyzing the production of these poles, it is possible to use the high-frequency, small-signal MOS model that considers all the mutual capacitances between the gate, source, and drain [28]. To verify this external loading effect, we have also performed measurements on other sensors designed for higher oscillation frequencies (e.g., 82 MHz). Due to reduced driving capability at higher frequencies, the measured output amplitudes are smaller with no observed overshoot.

The center of the suspended plate was gradually pressed down by the tip, and the output frequency of the oscillator decreased as a result of the increasing sensing capacitance. Fig. 14 shows the relationship of the output frequency with respect to the displacement. The total frequency shift is 14 MHz with a corresponding displacement of 0.56 μm and a capacitance change from 153 fF to 216 fF. The capacitive sensitivity in terms of the frequency shift is 222 kHz/fF. The maximum applied force is 517 μN, which is calculated using the product of the measured spring constant and the maximum tip displacement. Thus the sensitivity with respect to the applied force is shown to be 27.1 kHz/μN.

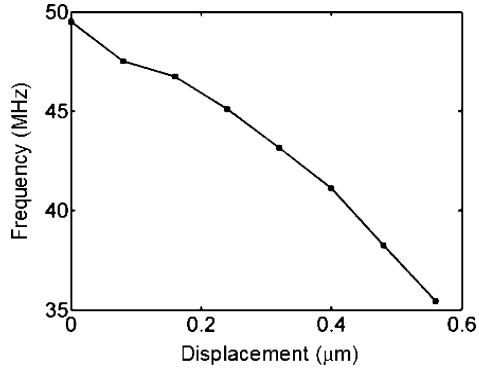

Fig. 14. Relationship of the measured frequency with respect to the plate displacement.

V. Discussion and Conclusion

In this paper, we have outlined a convenient CMOS micromachining process for making fingerprint sensors at die level, in contrast with most CMOS-compatible fingerprint sensors that are fabricated at wafer level. The suspended microstructure with a high stiffness in the out-of-plane direction can be successfully released without stiction during the wet etch. The sensing circuit works properly without being affected by the dielectric reactive ion etch for depassivation. For mass production, this die-level fabrication method has to be modified into a wafer-level process. It would be favorable for the passivation on bond pads to be replaced by a polymeric material capable of being lithographically patterned for etch protection of hydrogen peroxide in the etchant and able to provide the benefit of easy removal after etch. However, there is no such a material available to the best of our knowledge. By following the die-level approach, one of the options to remove the passivation on bond pads in a wafer process would be to place a dry film photoresist on wafer after the wet etch, followed by a lithographic step to open up the pad areas for the dielectric etch.

The sensor development takes advantage of the multiple metal layers and the fast electronics provided by an advanced sub-μm CMOS process. The former allows convenient signal routing beneath the suspended structure, and the latter enhances the sensor performance by producing a high output frequency from the oscillator. Monolithic integration prevents the oscillation frequency from being negatively impacted by parasitic capacitances as occurred in the two-chip solution. The measured sensitivity of 222 kHz/fF is nearly four orders of magnitude greater than recently reported data from a capacitive pressure sensor [23] using a 0.8-μm CMOS process in a hybrid implementation. The result is also two orders of magnitude greater than the value reported in [25].

Deviation of the measured spring constant with respect to the simulated value is attributed to the joint effect of the compressive residual stress and the variation in structural thickness. By separately adding a stress of -37 MPa and a thickness reduction of 10% in simulations, we observe corresponding reductions of 40% and 22% from the original simulated spring constant. With a combined stress of -37 MPa and a thickness reduction of 10%, the reduction is about 50%, close to the measured difference.

A test circuit with a fixed capacitance of 30 fF has shown a measured oscillation frequency at 103.6 MHz, higher than the 49.5 MHz of the reported sensor. The result implies that the same capacitive sensing is feasible with a circular plate of 66 μm in diameter, as compared to the current design of 150 μm. With the sensing circuit placed beneath each sensor, there is great potential in producing a fingerprint sensor by making a dense array through this approach. The maximum mechanical displacement is about 0.32% of the sensor's size, which is within the elastic range of the structural materials. There is no appreciable change in the output frequency after repeated loading, implying that the suspended plate can be restored to its initial position without permanent deformation.

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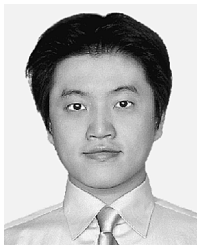

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