五、論文著述：

Publications and Conference Presentations

1. Chi-Fu Chang, Yarsun Hsu, “A System Exploration Platform for Network-on-Chip”, IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA), Sept., 2010
2. Tzer-Ta Tseng, Yarsun Hsu, “A flexible and cost-effective file-wise reliability scheme for storage systems”, IEEE High Performance Computing and Communications, Melbourne, Australia, Sept., 2010
3. Yi-Chiun Fang, Chien-Kai Tseng, Yarsun Hsu,” Emulation of Object-Based Storage Devices by a Virtual Machine”, C.-H. Hsu et al. (Eds.): Part II , LNCS 6082, pp. 176--187. ISBN 978-3-642-13135-6 , Springer, Heidelberg (2010). Paper was also presented at International Symposium on Frontiers of Parallel and Distributed Computing (FPDC 2010), Busan, Korea, May, 2010
4. Wei-Yu Tsai, Ching-Te Chiu, Jen-Ming Wu, Shuo-Hung Hsu, Yar-Sun Hsu, “A Novel MUX-FF Circuit for Low Power and High Speed Serial Link Interfaces”, IEEE International Symposium on Circuits and Systems, Paris, France, May, 2010
5. Chi-Fu Chang, Yarsun Hsu, “Nocsep: NOC-centric System Exploration Platform”, DATICS-FutureTech’10, Busan, Korea, May, 2010
6. Cheng-Chia Wang, Yarsun Hsu, “WOFS: a distributed network file system supporting fast data insertion and truncation”, SNAPI2010, Lake Tahoe, Ca., USA, May, 2010
7. Cheng-Chia Wang, Chien-Kai Tseng, Yarsun Hsu, “WOFS: a distributed network file system supporting fast data insertion and truncation”, National Computer Symposium, November 27-28, 2009
8. Chung-Wen Huang, Wei-Kuan Shih, Yarsun Hsu, and Jenq Kuen Lee, “Configurable SIDbased Multi-core Simulators for Embedded System Education”, WESE09, ESWEEK, Grenoble, France, October 15, 2009
9. Chih-Hao Lu, Chien-Ching Lin, Shau-Wei Yen, Chih-Lung Chen, Hsie-Chia Chang, Chen-Yi Lee, Yar-Sun Hsu, and Shyh-Jye Jou, “Design of a Multiple QC-LDPC Decoder Based on Shift-Routing Network”, IEEE Transcations on Circuits and Systems –II, Vol. 56, No. 9, September, 2009 (NSC 97-2221-E-009-166-MY3) (SCI)
10. Yu-Hao Hsu, Ming-Hao Lu, Ping-Lin Yang, Fan-Ta Chen, You-Hung Li, Min-Sheng Kao, Chih-Hsing Lin, Ching-Te Chiu, Jen-Ming Wu, Shuo-Hung Hsu, YarSun Hsu, “A Quarter-Rate 2.56/3.2Gbps 16/20:1 SERDES Interface in 0.18um CMOS Technology”, International Journal of Electrical Engineering, V.16 #1, Feb., 2009

(NSC-96-2752-E-007-002-PAE)

11. Changkuo Yeh, Tse-Ta Tseng, Yarsun Hsu, “An Improved Metadata Server Cluster”, High Performance Computing Asia (HPC-Asia), March 2-5, 2009 (NSC 96-2221-E-007-131-MY3)

12. Changkuo Yeh, Tse-Ta Tseng, Yarsun Hsu, “A Reliable DHT-Based Metadata Server Cluster”, 2008 International Computer Symposium, Nov. 13-15, 2008 (NSC 96-2221-E-007-131-MY3)

13. Jwo-An Lin, Yung-Chou Tsai, Tai-Jyi Lin, Yarsun Hsu, “Cycle Stealing Buffers and Channel Management for On-chip Networks”, IEEE High Performance Computing and Communications, September, 2008 (NSC-96-2220-E-007-032)

14. Y-H Hsu, M-H Lu, P-L Yang, F-T Chen, Y-H Li, M-S Kao, C-H Lin, C-T Chiu, J-M Wu, S-H Hsu, Y-S Hsu, “A Scalable Folded Load Balanced Switch with SerDes Interface in 0.13um CMOS Technology”, submitted to IEEE Trans. on Circuit and System I (Invited) 2008 (SCI)

15. Y-H Hsu, M-H Lu, P-L Yang, F-T Chen, Y-H Li, M-S Kao, C-H Lin, C-T Chiu, J-M Wu, S-H Hsu, Y-S Hsu, “A 28 Gbps 4x4 Switch with Low Jitter SerDes Using Area-saving RF Model in 0.13um CMOS Technology”, IEEE ISCAS, 2008

16. Chih-Hao Liu, Chien-Ching Lin, Hsie-Chia Chang, Chen-Yi Lee, Yar-Sun Hsu, “Multi-Mode Message Passing Switch Networks Applied for QC-LDPC Decoder”, IEEE International Symposium on Circuits and Systems 18-21 May 2008, Seattle, Washington, USA

17. Chih-Hao Lu, Shau-Wei Yen, Chih-Lung Chen, Hsie-Chia Chang, Chen-Yi Lee, Yar-Sun Hsu, and Shyh-Jye Jou, “An LDPC Decoder Chip Based on Self-Routing Network for IEEE 802.16e Applications”, IEEE Journal of Solid-State Circuits, Vol. 43, No. 3, March 2008 (SCI)

18. Jwo-An Lin, Yung-Chou Tsai, Tai-Jyi Lin, Yarsun Hsu, “Cycle Stealing Buffers and Physical Channel Management Scheme for Wormhole Based On-chip Networks”, National Computer Symposium, December, 2007

19. Lungpin Yeh, Juei-Ting Sun, Sheng-Kai Hung, Yarsun Hsu, “A Windows-Based Parallel File System”, High Performance Computation Conference, Houston, Texas, September, 2007 (NSC95-2221-E-007-022, NSC96-2752-E-007-004-PAE)

20. Po-Chun Liu, Sheng-Kai Hong, Yarsun Hsu, “Security Enhancement and Performance Evaluation of an Object-Based Storage System”, High Performance Computation Conference, Houston, Texas, September, 2007 (NSC95-2221-E-007-022, NSC96-2752-E-007-004-PAE)

21. Hsiang-Ju Hsu, Ching-Te Chiu, Yarsun Hsu, “Design of Ultra Low Power CML Muxs and Latches with Forward Body Bias”, 2007 IEEE SoC Conference, September, 2007 (EI)

22. Ching-Te Chiu, Jen-Ming Wu, Shuo-Hung Hsu, Yarsun Hsu, Ming-Hao Lu, Ping-Lin Yang, Fan-Ta Chen, You-Hung Li, Yu-Hao Hsu, Min-Sheng Kao, " A Quarter-Rate 2.56/3.2 Gbps 16/20:1 SERDES Interface in 0.18um CMOS Technology", 18th VLSI Design/CAD Symposium, August, 2007 (EI)

23. Ching-Te Chiu, Yu-Hao Hsu, Min-Sheng Kao, Hou-Cheng Tzeng, Ming-Chang Du, Ping-Ling Yang, Ming-Hao Lu, Fanta Chen, Hung-Yu Lin, Jen-Ming Wu, Shuo-Hung Hsu, Yar-Sun Hsu, "A Scalable Load Balanced Birkhoff-Von Neumann Symmetric TDM Switch IC for High-Speed Networking Applications", IEEE International Symposium on Circuits and Systems, New Orleans, USA, May 27-30, 2007. (NSC93-2752-E-007-002-PAE) (EI)

24. Sheng-Kai Hung, Yarsun Hsu*: " Reliable Parallel File System with Parity Cache Table Support". IEICE Transactions on Information and Systems, Special Section on Parallel/Distributed Processing and Systems, Vol. E90-D, #1, January, 2007 (NSC 92-2213-E-007-052) (SCI)

25. Sheng-Kai Hung, Yarsun Hsu* " DPCT: Distributed Parity Cache Table for Redundant Parallel File System". High Performance Computing and Communications, Sept., 2006, LNCS, 4208, Springer, P.320-329. (NSC 92-2213-E-007-052) (SCI)

26. Sheng-Kai Hung, Yarsun Hsu*: "Striping Cache: A Global Cache for Striped Network File System". Computer Systems Architecture, Sept., 2006, LNCS, 4186, Springer, P.387-393 (NSC 92-2213-E-007-052) (SCI)

27. C.H. Chao, M.S. Kao, C.H. Jen, Y.H. Hsu, P.L. Yang, C.T. Chiu, J.M. Wu, S.H. Hsu, Y.S. Hsu, "A 3.2 Gbits/S CML Transmitter with 20:1 Multiplexer in 0.18 CMOS Technology", IEEE International Conference Mixed Design of Integrated Circuits and Systems, Gdynia, June 22-24, 2006 (NSC 92-2213-E-007-052)

28. Sheng-Kai Hung, Yarsun Hsu*, "Modularized Redundant Parallel Virtual File System", 10th Asia-Pacific Computer Systems Architecture Conference, Singapore, Oct. 24-26, 2005. Also appears in Advances in Computer Systems Architecture, LNCS 3740, Springer, 2005. p.186-199 (NSC 92-2213-E-007-052) (SCI)

29. Ching-Te Chiu, Jen-Ming Wu, YarSun Hsu, Shuo-Hung Hsu, Min-Sheng Kao, Chih-Hsien Jen, "A 10 Gb/s Wide-Band Current-Mode Logic I/O Interface for High-Speed Interconnect in 0.18μm CMOS Technology", IEEE SOCC September 25-28, 2005, Washington DC, USA (NSC 93-2752-E-007-002-PAE) (EI)

30. Lungpin Yeh, Juei-Ting Sun, Sheng-Kai Hung, Yarsun Hsu*, "A Parallel File System for Windows", National Computer Symposium. Dec. 15-16, 2005 (NSC 92-2213-E-007-052)

31. Shen-Wei Chen, Wei-Chi Ting, Hung-Min Sun, Yarsun Hsu, "Modified AES for Wireless Sensor Networks", National Computer Symposium. Dec. 15-16, 2005 (NSC93-2213-E-007-103) (Received Best Paper Award)

32. Ching-Te Chiu, Jen-Ming Wu, Shuo-Hung Hsu, Cheng-Hsiang Hsiao, Chih-Hsien Jen, Yu-Hao Hsu, Min-Sheng Kao, Yarsun Hsu, “A 3.2 Gb/s 20:1 CML Transmitter in 0.18um CMOS Technology”, VLSI 2005 Design/CAD, August 8-11, 2005, Taiwan (NSC 93-2752-E-007-002-PAE) (EI)

33. Sheng-Kai Hung, Yarsun Hsu*, “Reliable Parallel File System”, 2004 International Computer Symposium, Dec 15-17, 2004. (NSC 92-2213-E-007-052) (Received best paper award)

34. MingShen Lin, Yarsun Hsu*, “Grid Enabled MPI: PACX-MPI Optimization”, 2004 International Computer Symposium, Dec 15-17, 2004 (NSC 92-2213-E-007-052)

35. Yarsun Hsu, “Design Consideration for Low Power Distributed Sensor Network”, Workshop for International Collaboration in SoC and Embedded System Technologies, April 22-24, 2004, Seoul, Korea (Invited speaker)

36. Yarsun Hsu “High Performance Server Architecture”, The Bioinformatics and BioGrid 2002 Workshop on BioGrid Technology and Applications, November 8, 2002, Tainan, Taiwan

37. Yarsun Hsu*, Jinsoo Kim, “Object characteristics and memory behavior of Java Programs”, The 11th Annual Wireless and Optical Communication Conference, New Jersey, April, 2002 (EI)

38. C. H. Lee, S.K. Hung, C.T. King, Y.Hsu, “A Reliable Multicast Protocol over Virtual Interface Architecture”, The 8th Workshop on Compiler Techniques for High Performance Computing, March 14-15, 2002 Taiwan (NSC 90-2213-E-007-076)

39. Jinsoo Kim, Yarsun Hsu “Memory system behavior of Java programs: methodology and Analysis”, ACM SIGMETRICS 2000 (ACM International Conference on Measurement and Modeling of Computer Systems), Santa Clara, California, USA, June 17-21, 2000 (Received best paper award) (EI)

40. Eric Wu, Yarsun Hsu, Yew-Huey Liu, ”Stack Simulation”, Encyclopedia of Electrical and Electronics Engineering, Editor: John Webster (U. of Wisconsin), John Wiley & Sons, Feb., 1999

41. Jinsoo Kim, Yarsun Hsu “Analyzing Memory Reference Traces of Java programs”, IEEE 2nd Annual Workshop on Workload Characterization, Austin, Texas, October 9, 1999

42. Yarsun Hsu, “Java Workload Characterization”, Java Server Performance Workshop, Hawthorne, New York, May 1999

43. Jinsoo Kim, Xiaohan Qin, Yarsun Hsu “Memory Characterization of a Parallel Data Mining Workload”, Proceedings of Workshop on Workload Characterization, ACM/IEEE Micro-31, Nov., 1998

44. Yarsun Hsu, “Parallel Systems and Modern Parallel IO Technology”, International Conf. on

Parallel and Distributed System, December, Seoul, Korea, 1997 (Invited tutorial) (EI)

45. Yarsun Hsu, “Overview of Scalable Shared Memory Systems”, 3rd Workshop on Compiler Techniques for High Performance Computing, March 20-21, 1997 (Invited tutorial)

46. Eric Wu, Yarsun Hsu, Yew-Huey Liu, “Efficient Stack Simulation for Set-Associative Virtual Address with Real tags”, IEEE transaction on Computer (p.719-723), May 1995 (SCI) (EI)

47. P. Corbett, D. Feitelson, J. Prost, G. Almasi, S. Baylor, A. Bolmarcich, Y. Hsu, J. Satran, M. Snir, R. Calo, B. HerrJ. Kavaky, T. Morgan, A. Zlotek, “Parallel file systems for IBM SP computers”, IBM System Journal (9.222-248), Vol. 34, #2, 1995 (SCI) (EI)

48. D. Feitelson, P. Corbett, S. Baylor, Y. Hsu, “Parallel I/o Subsystem in Massively Parallel Supercomputers”, IEEE Parallel and Distributed Technology (p.33-47), Vol. 3, #3, 1995 (SCI) (EI)

49. C. Benveniste, D. Pruett, Y. Hsu, “PPDT-A Parallel Program Development Tool Kit”, Summer Computer Simulation Conference, Ottawa, Canada, July, 1995

50. S. Baylor, C. Benveniste, Y. Hsu “Performance Evaluation of a Parallel I/O Architecture”, International Conference on Supercomputing, Spain, 1995 (EI)

51. P. Corbett, D. Feitelson, S. Fineberg, Y. Hsu, B. Nitzberg, J-P Prost, M. Snir, B. Traversat, P. Wong, “Overview of the MPI-IO Parallel I/O Interface”, third annual workshop on Input/Output in Parallel and Distributed Systems, 1995 International Parallel Processing Symposium (IEEE, ACM), April, 1995 (EI)

52. Eric Wu, Yarsun Hsu, Yew-Huey Liu, “Timestamp Consistency and Trace Driven Analysis for Distributed Parallel System”, 1995 Int. Parallel Processing Symposium (IEEE, ACM), April, 1995 (EI)

53. Yarsun Hsu, “Multiprocessor Systems and Parallel I/O Technology”, High Performance Computer System Workshop, July, 1995 (Invited tutorial)

54. E. Kalns, Y. Hsu, “Video on Demand using the Vesta Parallel File System”, 3rd Workshop on Input/Output in parallel and Distributed Systems, 1995 International Parallel Processing Symposium (IEEE, ACM), April, 1995 (EI)

55. J-P Prost, M. Snir, P. Corbett, D. Feitelson, Y. Hsu, “Collective I/O with Vesta Parallel File System”, Supercomputing Conference, 1994 (EI)

56. C. Benveniste, Y, Hsu, “Performance Evaluation of Central Queue Arbitration Policies for the Vulcan Parallel System”, 1994 Summer Computer Simulation Conference, July 1994.

57. Peter Corbett, Dror Feitelson, Yarsun Hsu, Jean-pierre Prost, Marc Snir, Sam fineberg, Bill Nitzberg, Bernard Traversat, Parkson Wang, “MPI-IO: A parallel file I/O interface”, Research report 19841, 1994

58. S. Baylor, C. Benveniste, Y. Hsu, “Performance Evaluation of a Massively Parallel I/O Subsystem”, 2nd Workshop on Input/Output in Parallel and Distributed Systems, 8th Int’l parallel Processing Symposium (IEEE, ACM), April, 1994 (EI)

59. S. Baylor, C. Benveniste, Y. Hsu, “Performance Evaluation of a Massively Parallel I/O Subsystem”, Special issue on Input/Output in Parallel Computer System, Computer Architecture News (ACM), Vol. 22, No. 4, Sept., 1994

60. Eric Wu, Yarsun Hsu, Yew Huey Liu, “A Quantitative Evaluation of Cache Types for High Performance Computer Systems”, IEEE Tran. On Computers (p.1154-1162), V.42, No. 10, October, 1993 (SCI)

61. Ching-Farn Eric Wu, Yarsun Hsu, Yew-Huey Liu, “Efficient Stack Simulation for Shared Memory Set-Associative Multiprocessor Caches”, International Conference on Parallel Processing (ICPP), 1993 (EI)

62. E. Wu, Y. Hsu, Y. Liu, “A Quantitative Evaluation of Cache Types”, Proceedings of (IEEE, ACM) 26th Hawaii Int. Conference on System Science, Jan., 1993 (EI)

63. E. Wu, Y. Hsu, Y. Liu, “One pass simulation for set-associative shared memory MP caches”, 1992 Int. Conf. On Parallel and Distributed Systems, Dec., 1992 (EI)

64. E. Wu, Y. Hsu, Y. Liu, “Stack simulation for set-associative V/R type cache”, IEEE Computer Software and Application Conference., Sep., 1992 Chicago, Illinois (EI)

65. S. Baylor, Y. Hsu, “The effect of network delays on the performance of MIN-based cache coherency protocols”, 1991 Int. Conf. On Parallel Processing, Aug., 1991 (EI)

66. S. Wang, Y. Hsu, “On integrating control algorithms for buffer management and concurrency for parallel transaction processing”, Int. Conf. On VLSI and Systems, May, 1991

67. S. Min, Y. Hsu, H. Kim, “A design of performance optimized control-based synchronization”, Joint Conf. On Vector and Parallel Processing (VAPP/CONPAR 90) pp.312-323, Sept., 1990 Switzerland

68. C. Benveniste, Y. Hsu, “A Trace-Driven Analysis of the Wrap-Around Network”, IEEE Int. Conf. On Computer Design, Sept., 1990 (EI)

69. Y. Hsu, C. Benveniste, J. Ruedinger, C. Tan, “Design of VLSI Switch for Highly Parallel Multiprocessor Systems”, IEEE Custom Integrated Circuit Conference, May 1990, Boston (EI)

70. S. Wang, Y. Hsu, “A novel message switch for highly parallel systems”, IEEE Int. Conf. On Computer Design, Oct.2-4, 1989 (EI)

71. Y. Hsu, C. Benveniste, J.Ruedinger, C. Tan, “Large interconnection network for highly parallel systems”, Int. Conf. On Circuit and System, pp.256-261, July, 1989 (EI)

72. Y. Hsu, C. Tan, W. Kleinfelder,"Design of Combining Switch for RP3", Int. Sym. On VLSI Technology and System Application, pp.349-353, 1987 (EI)

Patents

1. Chen-Yi Lee, Chih-Hao Liu, Chien-Ching Lin, Hsie-Chia Chang, Yar-Sun Hsu, "Method and apparatus for switching data in communication system", US patent 7,724,772, May, 2010
2. Chen-Yi Lee, Jr-Hau Lu, Chien-Ching Lin, Hsie-Chia Chang, Yar-Sun Hsu, "Method and apparatus for switching data in communication system", US patent 7,724,770, May, 2010
3. Chih-Hao Liu, Chien-Ching Lin, Chen-Yi Lee, Hsie-Chia Chang, Yarsun Hsu, "Multi-mode multi-parallelism data exchange method and device thereof", US patent 7,719,442, May 18, 2010
4. "物件導向之單晶片網路模型", Patent pending, 2009 (With Chi-Fu Chang)
5. "單晶片網路之系統探索平台以及使用於該探所平台之平行應用程式通訊機制描述格式", Patent pending, 2009 (With Chi-Fu Chang)
6. "Multi-mode multi-parallelism data exchange method and device", US Patent Application **#:** 20090146849 (with Chih-Hao LIU, Chien-Ching Lin, Chen-Yi Lee, Hsie-Chia Chang) 2008
7. "Operating method applied to low density parity check (ldpc) decoder and circuit", US Patent Applicaton **#:** 20090037799 (with Chih-Hao LIU, Yen-Chin Liao, Chen-Yi Lee, Hsie-Chia Chang) 2008
8. "Method for Providing Virtual Atomicity in Multi Processor Environment Having Access to Multilevel Caches", US Patent 6,175,899, Jan., 2001 (with Sandra Baylor) (EI)
9. "Hierarchical Bus Simple COMA Architecture for Shared Memory Multiprocessors Having A Bus Directly Interconnecting Caches Between Nodes", US Patent 6,148,375, Nov. 14, 2000 (with Sandra Baylor) (EI)
10. "Cache coherency for lazy entry consistency in lockup-free caches", US Patent 6,094,709, July, 2000 (with Sandra Baylor, Anthony Bolmarcich, and Ching-Farn Wu) (EI)
11. "A cache coherency protocol for reducing the effects of false sharing in non-bus-based shared memory multiprocessors", US patent 5,822,763, Oct., 1998 (with Sandra Baylor) (EI)
12. "An invalidation bus optimization for multiprocessors using directory based cache coherency protocols", US Patent 5,778,437, July, 1998 (with Sandra Baylor) (EI)

13. “New switch queue structure for one-network parallel processor systems”, US patent 5,313,649, May, 1994 (with Roy Jackson) (EI)
14. “Network Rearrangement Method and System”, US patent 5,287,491 Feb., 1994 (EI)
15. “Single FIFO High Speed Combining Switch”, U.S. Patent 5,946,000, Sept., 1991 (EI)
16. “Programmable vatiable cycle clock circuit for skew tolerant array processor architecture”, U.S. Patent 4,851,995, July 25, 1989 (with H-W Li) (EI)

Book Chapters

1. Dror Feitelson, Peter Corbett, Sandra Baylor, Yarsun Hsu, “Parallel I/O Subsystems in Massively Parallel Supercomputer”, Book Chapter 24, edited by Toni Cortes, Hai Jin, and Rajkumar Buyya, IEEE and Wiley Interscience, 2002, ISBN: 0-471-20809-4
2. P. Corbett, D. Feitelson, S. Fineberg, Y. Hsu, W. Nitzberg, J. Prost, M. Snir, W. Traverset, P. Wong, “Overview of the MPI-IO Parallel IO Interface”, Book Chapter 27, edited by Toni Cortes, Hai Jin, and Rajkumar Buyya, IEEE and Wiley Interscience, 2002, ISBN:0-471-20809-4
3. Jin-soo Kim, Yarsun Hsu, “Analyzing memory reference traces of Java programs”, Chapter 2, isbn 0-7923-7777-x, Book edited by Lizy Kurian John and Ann Maarie Grizzaffi Maynard, Kluwer Academic Publishers, 2000
4. D. Feitelson, J-P Prost, P. Corbett, Y. Hsu, “Parallel IO Systems and Interfaces for Parallel Computers”, Book chapter appeared in Multiprocessor Systems-Design and Integration, Editor: C-L Wu, World Scientific Publication Company, August, 1996(35 pages). ISBN: 9810222181
5. Eric Wu, Yarsun Hsu, Yew-Huey Liu, “One-pass simulation methodology for Cache Performance Analysis”, Book chapter appeared in Multiprocessor System-Design and Integration, World Scientific Publication Company, August, 1996 (47 pages). ISBN: 9810222181
6. P. Corbett, D. Feitelson, S. Fineberg, Y. Hsu, B. Nitzberg, J-P Prost, M. Snir, B. Traversat, P. Wong, “Overview of The MPI-IO Parallel IO Interface”, Chapter 5, INOUT/OUTPUT IN PARALLEL AND DISTRIBUTED COMPUTER SYSTEMS, edited by Ravi Jain, et al, Kluwer Academic Publishers, June, 1996. ISBN: 0792397355
7. E. Kalns, Y. Hsu, “Video On Demand Using The Vesta Parallel File System”, Chapter 8, INOUT/OUTPUT IN PARALLEL AND DISTRIBUTED COMPUTER SYSTEMS, edited by Ravi Jain, et al, Kluwer Academic Publishers, June, 1996. ISBN: 0792397355
8. S. Baylor, C. Benveniste, Y. Hsu, “Performance Evaluation of A Massively Parallel I/O

Subsystem", Chapter 13, INOUT/OUTPUT IN PARALLEL AND DISTRIBUTED COMPUTER SYSTEMS, edited by Ravi Jain, et al, Kluwer Academic Publishers, June, 1996. ISBN: 0792397355

Awards

- 清華大學 **校傑出教學獎**, 2009
- 清華大學 **校傑出教學獎**, 2006
- 清華大學電資院 **院傑出教學獎**, 2005
- **Best Paper Award**, National Computer Symposium, December 2005
- **Best Paper Award**, International Computer Symposium, December, 2004
- IBM Supplemental **Invention Award**, 2001
- **Best Paper Award**, ACM SIGMETRICS 2000 (ACM International Conference on Measurement and Modeling of Computer Systems), Santa Clara, California, June, 2000
- IBM **Top 5% Patent Invention Award**, 1999
- IBM third **Invention Plateau Achievement Award**, 1997
- IBM Second **Invention Plateau Achievement Award**, 1995
- IBM Research Technical Award for the contribution to parallel I/O for the IBM SP2, 1995.
- IBM Research Technical Award for contribution to communication switching network of IBM SP power parallel System, 1994
- IBM first **Invention Plateau Achievement Award**, 1988