

Publications:

I. Referred Papers

1. S.-N. Tang, C.-H. Liao and T.-Y. Chang, "An Area- and Energy-Efficient Multimode FFT Processor for WPAN/WLAN/WMAN Systems," IEEE Journal of Solid-State Circuits, Vol. 47, No. 6, pp. 1419-1435, June 2012. (NSC 98-2221-E-007-095, CIC T18-99B-05a, SCI, EI)
2. Y.-H. Chen, and T.-Y. Chang, "A High Performance Video Transform Engine by Using Space-Time Scheduling Strategy," IEEE Trans. on VLSI Systems, Vol. 20, No. 4, pp. 655-664, April 2012. (NSC 99-2221-E-007-119, CIC T18-98C-12a, SCI, EI)
3. Y. H. Chen and T. Y. Chang, "A High-Accuracy Adaptive Conditional-Probability Estimator for Fixed-width Booth Multipliers," IEEE Trans. Circuits and Systems I, vol. 59, no. 3, pp. 594-603, Mar. 2012. (NSC 100-2221-E-007-092, SCI, EI)
4. C.-Y. Li, Y.-H. Chen, T.-Y. Chang, L.-Y. Deng and K. To "Period Extension and Randomness Enhancement Using High-Throughput Reseeding-Mixing PRNG," IEEE Trans. on VLSI Systems, Vol. 20, No. 2, pp. 385-389, Feb. 2012.(NSC 99-2221-E-007-119, SCI, EI)
5. Y.-H. Chen, C.-Y. Li, and T.-Y. Chang, "Area-Effective and Power-Efficient Fixed-Width Booth Multipliers Using Generalized Probabilistic Estimation Bias," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol. 1, No. 3, pp. 277-288, Sept. 2011. (NSC 100-2221-E-007-092, SCI, EI)
6. Y.-H. Chen, T.-Y. Chang, and C.-Y. Li, "High Throughput DA-based DCT with High Accuracy Error-compensated Adder Tree," IEEE Trans. on VLSI Systems, Vol. 19, No. 4, pp. 709-714, April 2011.(NSC 98-2221-E-007-095, SCI, EI).
7. C.-Y. Li, Y.-H. Chen, T.-Y. Chang, and J.-N. Chen, "A Probabilistic Estimation Bias Circuit for Fixed-width Booth Multiplier and Its DCT Applications," IEEE Trans. on Circuits and Systems II, Vol. 58, No. 4, pp. 215-219, April 2011.(NSC 99-2221-E-007-119, SCI, EI)
8. P.-L. Chen, Y.-C. Huang, T.-Y. Chang, "Fast Test Integration: Toward Plug-and-Play at-speed Testing of Multiple Clock Domains Based on IEEE Standard 1500," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 29, No. 11, pp. 1837-1842, Nov. 2010. (NSC 98-2221-E-007-095, CIC-T18-98A-02a, SCI, EI).
9. S.-N. Tang, J.-W. Tsai and T.-Y. Chang, "A 2.4-GS/s FFT Processor for OFDM Based WPAN Applications" IEEE Trans. on Circuits and Systems II, Vol. 57, No. 6, pp. 451-455, June 2010. (NSC 98-2221-E-007-095, CIC-UN90-98A-06a, SCI, EI).
10. P.-L. Chen, J.-W. Lin, and T.-Y. Chang, "IEEE Standard 1500 Compatible Delay Test Framework" IEEE Trans. on VLSI Systems, Vol. 17, No. 8, pp. 1152-1156, Aug. 2009. (CIC U18-94C-17a, NSC 96-2220-E007-027 and MoEA 96-EC-17-A-01-S1-002, SCI, EI.)
11. H.-C. Lin, H.-H. Wu, and T.-Y. Chang, "An Active-Frequency Compensation Scheme for CMOS Low-Dropout Regulators with Transient-Response Improvement," IEEE Trans. on Circuits and Systems II, Vol. 55, No. 9, pp. 853-857, Sept. 2008. (CIC D35-96B-13, NSC 96-2220-E007-027, SCI, EI.)

12. M.-J. Hsiao, J.-R. Huang, and T.-Y. Chang, "A Built-in Parametric Timing Measurement Unit", IEEE Design & Test of Computers," Vol. 21, No. 4, pp. 322-330, July-Aug. 2004. (NSC 90-2215-E007-044, NSC 91-2622-E007-026-CC3, NSC 92-2220-E007-003, SCI, EI)
13. S.-S. Yang, P.-L. Guo, T.-Y. Chang and J.-H. Hong, "A Low-Power TFT-LCD Column Driver Design for Dot-Inversion Method," IEICE Transaction on Fundamentals of Electronics, Communications and Computer Sciences, Vol. E87A, No. 2, pp. 364-369, Feb. 2004 (NSC 91-2215-E007-038, NSC 92-2220-E007-003, SCI, EI).
14. S.-S. Yang, H.-Y. Lo, T.-Y. Chang and T.L. Jong, "Design of the Earle Latch for High Performance Pipeline", IEE, Proc.- Computer and Digit. Tech., Vol. 149, No. 6, pp. 245-248, Nov. 2002. (NSC 90-2215-E007-044, NSC 91-2215-E007-038, CIC T06-89D-35e, and MoEA 91-EC-17-A-03-S1-0002.) (SCI, EI)
15. H.-Y. Lo, T.-Y. Chang, and M.-C. Lee, "Parallel Unidirectional Division Algorithms and Implementations," Journal of the Chinese Institute of Engineers, pp. 487-496, July 2001. (EI)
16. H.-Y. Lo, T.-Y. Chang, H.-F. Lin, C.H. Chen, J.S. Liu, C.-C. Liu, J. H. Lee, J.-S. Shie, S. S. Chen, P. C. Chang, W. M. Cho, J. H. Houn, M.-S. Shiau, and C.-H. Yang, "A Built-in Test Scheme for Pipelined Multipliers and Dividers," Journal of Hunan University, Natural Science, Vol. 27, No. 5, pp. 31-45, Sept. 2000.
17. C.-T. Huang, J.-R. Huang, C.-F. Wu, C.-W. Wu, and T.Y. Chang, "A Programmable BIST Core for Embedded DRAM," IEEE Design & Test, Vol. 16, No. 1, pp. 59-70, Jan. 1999. (SCI, EI)
18. T. Y. Chang and M.-J. Hsiao, "A Carry-Select Adder Using Single Ripple-Carry Adder," IEE Electronics Letters, Vol. 34, No. 22, pp. 2101-2103, 29th Oct. 1998. (NSC 87-2215-E007-019, NSC 88-2215-E007-031.) (SCI, EI)
19. Y.-C. Yu and T.Y. Chang, "A Testable On-the-fly Carry-save Multiplier by Alternating Input Data," IEE Proceedings, Computers and Digital Techniques, Vol. 143, No. 5, pp. 345-348, Sept. 1996. (NSC 85-2215-E007-015, NSC 85-2221-E007-040) (SCI, EI)
20. Chang, T.Y. and Y.S. Lin, " Design of Fault-Tolerant Systolic Array Multiplier with Time Redundancy," NSC Proc. Part A, Vol. 18, No. 5, pp. 514-522, Sept. 1994.
21. Chang, T.Y., C.C. Wang, and J.B. Hsu, "Two schemes for Detecting CMOS Analog Fault," IEEE Journal of Solid-State Circuits, Vol. SC-27, No. 2, pp. 229-233, Feb. 1992. (NSC 80-0404-E007-018) (SCI, EI)
22. Wey, C.L., T.Y. Chang, and J. Ding, "Design of Fault-Diagnosable and Repairable Folded PLA's for Yield Enhancement," IEEE Journal of Solid-State Circuits, Vol. SC-26, No. 1, pp. 54-57, Jan. 1991. (SCI, EI)
23. Wey, C.L. and T.Y. Chang, "Design of VLSI-based Parallel Multipliers" IEE Proc., Part E, Computers and Digital Techniques, Vol. 137, No. 4, pp. 328-336, July 1990. (SCI, EI)
24. Wey, C.L. and T.Y. Chang, "An Efficient Output Phase Assignment for PLA Minimization," IEEE Trans. on CAD of Integrated Circuits and Systems, Vol. 9, No. 1, pp. 1-7, Jan. 1990. (SCI, EI)
25. Chang, T.Y. and C.L. Wey, "Design of Fault Diagnosable and Repairable PLA's," IEEE Journal of Solid-State Circuits, Vol. SC-24, No. 5, pp. 1451-1454, Oct. 1989.(SCI,EI)

II. Conference Papers

1. Wey, C.L., T.Y. Chang, and M.K. Vai, "On the Design of Fault-Tolerant Programmable Logic Arrays," Proc. Int'l Computer Symposium Taiwan, pp. 398-404, Dec. 1986.
2. Wey, C.L., T.Y. Chang, and Y.F. Chen, "The Design of VLSI-based Parallel Multipliers, " Proc. of 30th Midwest Symposium on Circuits and Systems, pp. 97-104, Aug. 1987.
3. Wey, C.L. and T.Y. Chang, "Minimization of PLAs with Ground True Outputs," Proc. of 25th ACM/IEEE Design Automation Conference, Anaheim, CA., pp. 421-426, June 1988. (EI)
4. Chang, T.Y. and C.L. Wey, "The Design of Electrically Field-Repairable Programmable Logic Arrays (EFRPLAs)," Proc. of 31st Midwest Symposium on Circuits and Systems, St. Louis, MO., pp. 36-39, Aug. 1988.
5. Wey, C.L. and T.Y. Chang, "An Efficient Boolean Comparison Process for Logic Verification," Proc. of 31st Midwest Symposium on Circuits and Systems, St. Louis, MO., pp. 1175-1178, Aug. 1988.
6. Wey, C.L., J. Ding, and T.Y. Chang, "Design of Repairable and Fully and Fully Diagnosable Folded PLAs," Proc. of 27th ACM/IEEE Design Automation Conference, Orlando, FL, pp. 327-332, June 1990. (EI)
7. Wey, C. L. and T. Y. Chang, "On the Design of Concurrent Error Detectable Multiply and Divide Arrays," Proc. of Int'l Computer Symposium, pp. 564-570, Hsinchu, Taiwan, Dec 17-19, 1990.
8. Chang, T. Y., C. W. Wu, C. C. Wang, and J. B. Hsu, "On the Design of Fault-Tolerant Systolic Array Multiplier Using Time Redundancy," Proc. of Fourth Int'l Symposium on IC Design, Manufacture and Applications, pp. 497-502, Singapore, Sept. 11-13, 1991.
9. J.B. Hsu and T.Y. Chang, " Design of C-testable DCVS Binary Array Multipliers," Proc. of National Computer Symposium, pp. 111-116, Chungli, Taiwan, Dec. 18-19, 1991.
10. Chang, T.Y., J. B. Hsu, C. C. Wang, and Y. S. Lin, "A Design for Concurrent Error Detections in FPLAs," Proc. of 2nd Great Lakes Symposium on VLSI, pp. 9-15, Kalamazoo, Michigan, USA, Feb. 28-29, 1992.
11. Wang, C. C. and T. Y. Chang, "Concurrent Error Detections and Correction in Systolic Arrays," Informal digest of 3rd VLSI/CAD Symposium, pp. 53-62, Sun-Moon Lake, Taiwan, March 20-22, 1992.
12. Chang, T.Y., Y.S. Lin, "The Unsigned Multiplications Using Self-Dual Property," Proc. of Int'l Computer Symposium, pp. 385-391, Taichung, Taiwan, ROC, Dec. 13-15, 1992.

13. Wu, C. W., C. T. Chang, and T. Y. Chang, "On Testable Design of FFT Butterfly Networks," Proc. Int'l Conference Parallel and Distributed Systems, pp. 190-195, Hsinchu, Taiwan, Dec. 16-18, 1992.
14. Chang, T.Y. and J.H. Chen, "An IDDQ-Fault Free-Time Repairable CMOS SRAM Scheme," Informal digest of 4th VLSI Design/CAD Workshop, pp. 171-175, Nantou, Aug. 26-28, 1993.
15. Chang, T.Y., "On the Design of Full Adder Cells Using Reduced Transmission Gates and Probabilities," Proc. of 5th Int'l Symposium on IC Design, Manufacture and Applications, pp. 602-606 Singapore, Sept. 16-18, 1993.
16. Chang, T.Y., J.H. Chen, and J.B. Hsu, "A C-Testable DCVS GF(2^m) Multiplier," Proc. of 2nd Asian Test Symposium, Beijing, pp. 204-209, Nov. 16-18, 1993.
17. Chang, T.Y., Y.C. Wei, and J.H. Chen, "A C-Testable GF(2^m) Multiplier," Proc. of National Computer Symposium, pp. 539-546, Chia-Yi, Dec. 2-3, 1993.
18. Chang, T.Y., Y.C. Wei, and Y.C. Yu, "A C-Testable GF(2^m) Multiplier for Single Stuck-at Fault Model," Informal digest of 5th VLSI Design/CAD Symposium, pp. 187-192, Tainan, Aug. 25-27, 1994.
19. Chang, T.Y. and J.H. Chen, "A Fault-Tolerant DCVS Array Multiplier Using Alternative Logic Recomputations," Informal digest of 5th VLSI Design/CAD Symposium, pp. 137-142, Tainan, Aug. 25-27, 1994.
20. Chang, T.Y., Y.C. Wei, and Y.C. Yu, "A Synthesis of C-Testable DCVS GF(2^m) Multiplier," Proc. of Int'l Computer Symposium, pp. 606-611, Hsinchu, Dec. 12-15, 1994.
21. Yu, Y.C. and T.Y. Chang, "A Concurrent Error Detection and Correction Systolic Array Multiplier through Time Redundancy," Informal digest of 6th VLSI Design/CAD Symposium, pp. 81-84, Chia-i, Aug. 17-19, 1995.
22. Chang, T.Y. and, P.S. Wang "Two Implementations of nxn Carry-Save Multiplication without Final Addition," Informal digest of 6th VLSI Design/CAD Symposium, pp. 169-172, Chia-i, Aug. 17-19, 1995.
23. Chen, W.F. and, T.Y. Chang "A Low-Power Modulator Design," Informal digest of 7th VLSI Design/CAD Symposium, pp. 139-142, Shi-Mon, Aug. 15-17, 1996.
24. Chang, T.Y. and P.S. Wang, "Comparison and Analysis of Three Implementations of nxn On-the-fly Conversion," Informal digest of 7th VLSI Design/CAD Symposium, pp. 257-260, Shi-Mon, Aug. 15-17, 1996.
25. Chang, T.Y. and W.F. Chen, "An IDDQ-fault Location Scheme," Proc. of 39th Midwest Symposium on Circuits and Systems, pp. 291-294, Ames, Iowa, Aug. 19-21, 1996.
26. T.Y. Chang, M.C. Luo, "A 3V, Fast Lock-in PLL for High Speed Systems" Informal digest of 8th VLSI Design/CAD Symposium, pp. 193-196, Sun-Moon Lake, Aug. 21-23, 1997.

27. L.M. Tseng, T.Y. Chang, “High-Speed Multiplier/Divider Using Hybrid Number Representation” Informal digest of 8th VLSI Design/CAD Symposium, pp. 197-200, Sun-Moon Lake, Aug. 21-23, 1997.
28. 葉明杰, 張慶元, “低功率置換邏輯可測試 CMOS 陣列乘法器及類比估測器” Informal digest of 8th VLSI Design/CAD Symposium, pp. 377-340, Sun-Moon Lake, Aug. 21-23, 1997.
29. T.Y. Chang, J. R. Huang, and S.-S. Yang “Leading-Zero Anticipatory Logics for Fast Floating Addition with Carry Propagation Signal” Proc. of 40th Midwest Symposium on Circuits and Systems, pp. 385-388, Sacramento, CA, Aug. 4-6, 1997.
30. G.-S. Hwang and T.Y. Chang, “A Gate-Level C-Testable Design Method for GF(2^m) Power-Sum Circuit” Informal digest of 9th VLSI Design/CAD Symposium, pp. 137-140, Nantou, Aug. 19-22, 1998.
31. T.Y. Chang and C.Y. Li, “High Speed Parity Prediction for Binary Additions Using the Recursive Carry-Masking Method” Informal digest of 9th VLSI Design/CAD Symposium, pp. 227-230, Nantou, Aug. 19-22, 1998.
32. S.-S. Yang and T.Y. Chang, “Leading Zero Counter for Floating-Point Normalization” Informal digest of 9th VLSI Design/CAD Symposium, pp. 239-242, Nantou, Aug. 19-22, 1998.
33. C.-Y. Chen and T.Y. Chang, “Area-Efficient Two’s Complement Serial-Parallel Multiplier/Accumulator” Informal digest of 9th VLSI Design/CAD Symposium, pp. 397-400, Nantou, Aug. 19-22, 1998.
34. T.Y. Chang and S.-S. Yang, “The Implementation of Three-Level Leading Zero Counter with Small LZCs” Informal digest of 10th VLSI Design/CAD Symposium, pp. 69-72, Nantou, Aug. 18-21, 1999.
35. W.-C. Chiang, J.-R. Huang, and T.Y. Chang, “Orthogonal Frequency Division Multiplexing and Fast Fourier Transform” Proc. of 8th Int’l Symposium on IC Design, Manufacture and Applications, pp. 371-374, Singapore, Sept. 8-10, 1999.
36. J.-N. Ko, J.-R. Huang, and T.Y. Chang, “Inductive Fault Analysis and Fault Modeling of NOR Array Flash Memories” Proc. of 8th Int’l Symposium on IC Design, Manufacture and Applications, pp. 60-63, Singapore, Sept. 8-10, 1999.
37. J.-N. Ko, J.-R. Huang, and T.-Y. Chang, “March Test and On-Chip Test Circuit of Flash Memories,” Proc. of 43rd Midwest Symposium on Circuits and Systems, pp. 128-131, Lansing, MI, Aug. 8-11, 2000.
38. T.-Y. Chang, J.-R. Huang, H.-Y. Lo, P.-S. Wang, and K. Yang, “The On-the-fly Circuits That Can Be Applied to Array Multiplier and Fast Gray Code Adder,” Proc. of 43rd Midwest Symposium on Circuits and Systems, pp. 342 – 345, Lansing, MI, Aug. 8-11, 2000.

39. N.-S. Chang, M.-J. Hsiao, J.-R. Huang, and T.-Y. Chang, “A Low-Latency March-Based Memory Repair Analysis Architecture,” Informal digest of 11th VLSI Design/CAD Symposium, pp. 129-132, Aug. 16-19, 2000.
40. Y.-L. Horng, J.-R. Huang, and T.-Y. Chang, “A Realistic Fault Model for Flash Memories,” Proc. of Asian Test Symp., pp. 274-281, Taipei, Dec. 2000.
41. M.-J. Hsiao, J.-R. Huang, S.-S. Yang and T.-Y. Chang, “An Embedded Low-Cost CMOS Time Interval Measurement Core with 0.5ns Measurable Period for SoC Application” Proc. of ISCAS, Sydney, pp. 190-193, May 2001. (NSC 90-2215-E007-065) (EI)
42. M.-J. Hsiao, J.-R. Huang, S.-S. Yang and T.-Y. Chang, “A Built-in Timing Parametric Measurement Unit” Proc. of Int’l Test Conf., Baltimore, pp. 315-322, Oct. 2001. (NSC 90-2215-E007-011) (EI)
43. J.-H. Tsai, M.-J. Hsiao, and T.-Y. Chang, “A Built-In-Self-Test Approach for Digital to Analog Converters”, Proc. of Asian Test Symp., pp. 423-428, Japan, Nov. 2001. (NSC 90-2215-E007-065)
44. C.-W. Chou, J.-R. Huang and T.-Y. Chang, “A Hierarchical Test Access Mechanism for SOC and the Automatic Test Development Flow”, Proc. of MWSCAS, USA, 2002. (NSC 90-2215-E007-044)
45. H.-Y. Liao, S.-S. Yang, and T.-Y. Chang, “2.5Gbps Laser Diode Driver with Auto Power Control/Auto-Biasing”, Informal digest of VLSI/CAD Symposium, pp. 30-33, Taidong, Taiwan, 2002. (NSC 90-2215-E007-044)
46. M.-C. Lee, J.-R. Huang, C.-P. Su, T.-Y. Chang, C.-T. Huang, and C.-W. Wu, “A True Random Generator Design”, Informal digest of VLSI/CAD Symposium, pp. 137-140, Taidong, Taiwan, 2002. (NSC 90-2215-E007-044, MoEA 91-EC-17-A-03-S1-0002)
47. S.-H. Hsieh, M.-J. Hsiao and T.-Y. Chang, “An Embedded Built-In-Self-Test Approach for Analog-to-Digital Converters”, Proc. of Asian Test Symposium, pp. 266-271, Guam, USA, 2002. (NSC 90-2215-E007-044)
48. S.-R. Lee, M.-J. Hsiao and T.-Y. Chang, “An Access Timing Measurement Unit of Embedded Memory”, Proc. of Asian Test Symposium, pp. 104-109, Guam, USA, 2002. (NSC 90-2215-E007-044)
49. Shao-Sheng Yang, Pao-Lin Guo, Tsin-Yuan Chang, and Jin-Hua Hong, “A Multi-Phase Charge-Sharing Technique without External Capacitor for Low-Power TFT-LCD Column Drivers,” Proc. of ISCAS 2003, pp. 365-368, Bangkok. (NSC 91-2215-E007-038) (EI)
50. K.-C. Chen, M.-J. Hsiao, J.-R. Huang, and T.-Y. Chang, “An Effective Analysis Method for Worst-case Crosstalk Noise with Non-ideal Input Waveform,” Informal digest of VLSI/CAD

- Symposium, pp. 469-472, Hualien, Taiwan, Aug. 2003. also in Proc. Int'l Conference on Information Cybernetics and Systems (ICICS), pp. 325-330, Kaohsiung, Taiwan, Dec. 2003. (NSC 91-2215-E007-038, MoEA 91-EC-17-A03-S1- 0002)
51. K.-J. Mo, S.-S. Yang, and T.-Y. Chang, "Timing Measurement Unit with Multi-Stage TVC for Embedded Memories", in Proc. Asia and South Pacific Design Automation Conf. (ASP-DAC), pp. 565-566, Yokohama, Jan. 2004. (NSC 92-2220-E-007-003)
52. C.-C. Yu , M.-J. Hsiao and T.-Y. Chang, "Built-in Cell Current Measurement for Flash Memories," Informal digest of VLSI/CAD Symposium, P3-13, Kenting, Taiwan, Aug. 2004. (NSC 92-2220-E-007-003)
53. C.-F. Li, S.-S. Yang and T.-Y. Chang, "An Accumulated Jitter Measurement Unit for Phase-Locked Loops," Informal digest of VLSI/CAD Symposium, P3-17, Kenting, Taiwan, Aug. 2004. (NSC 92-2220-E-007-003)
54. J.-R. Huang, M.-J. Hsiao, P.-L. Chen , P.-S. Huang, and T.-Y. Chang, "Functional Path Delay Fault Test Flow for Processor and ASICs in SoC," Informal digest of WRTL'T'04, 5th Workshop on RTL and High Level Testing, pp. 97-102, Osaka, Japan, Nov., 2004. (MoEA 92-EC-17-A03-S1- 0002)
55. Y.-M. Sheng, M.-J. Hsiao, T.-Y. Chang, "A Measurement Unit for Input Signal Analysis of SRAM Sense Amplifier," Proc. of Asian Test Symposium, pp. 272-276, Kenting, Taiwan, Nov. 2004. (NSC 92-2220-E-007-003, NSC 93-2220-E-007-004)
56. H.-T. Yang, J.-R. Huang, and T.-Y. Chang, "A Chaos-Based Fully Digital 120 MHz Pseudo Random Number Generator," Proc. of IEEE Asia-Pacific Conf. on Circuits and System, pp.357-360, Tainan, Taiwan, Dec. 2004. (MoEA 92-EC-17-A-03-S1-0002, NSC 93-2220-E-007-029 and CIC U18-93B-07a)
57. C.-F. Li, S.-S. Yang and T.-Y. Chang, "On-Chip Accumulated Jitter Measurement for Phase-Locked Loops," Proc. of IEEE Asia South Pacific Design Automation Conf., pp.1184-1187, Shanghai, China, Jan. 2005. (NSC 93-2220-E-007-004 and NSC 93-2220-E-007-029)
58. J.-S. Chen, C.-Y. Li, and T.-Y. Chang, "The Reseeding Timing for a 32-bit Digital Chaos-Based Pseudo Random Number Generator" Informal digest of WRTL'T05, pp. 131-134, Harbin, China, July, 2005. (NSC 93-2220-E-007-029, MoEA 93-EC-17-A-03-S1-0002)
59. C.-H. Hsieh, S.-S. Yang, and T.-Y. Chang, "A PLL Fault Location Scheme" Informal digest of VLSI/CAD Symp., pp. P2-61, Hualien, Taiwan, Aug. 2005. (NSC 93-2220-E-007-004)
60. C.-C. Lee, S.-S. Yang, C.-Y. Li, and T.-Y. Chang, "Built-In Self-Measurement for SRAM Sense Amplifier Input Signal" Informal digest of VLSI/CAD Symp., pp. P1-11, Hualien, Taiwan, Aug. 2005. (NSC 93-2220-E-007-004)

61. H.-H. Chiu, P.-L. Chen,, C.-Y. Li, and T.-Y. Chang, “A Delay Test Wrapper Design on Core-Based System-on-Chip” Informal digest of VLSI/CAD Symp., pp. P2-62, Hualian, Taiwan, Aug. 2005. (MoEA 93-EC-17-A-03-S1-0002)
62. C.-Y. Li, J.-S. Chen, and T.-Y. Chang, “A Chaos-Based Pseudo Random Number Generator Using Timing-Based Reseeding Method,” Proc. of ISCAS 2006, pp. 3277-3280, Greece. (NSC 94-2220-E007-029, MoEA 93-EC-17-A-03-S1-0002) (EI)
63. C.-H. Lin, C.-Y. Li and T.-Y. Chang, “High Fault Coverage Built-In Self-Test for Phase-Locked Loops” Informal digest of VLSI/CAD Symp., pp. P22, Hualian, Taiwan, Aug. 2006. (NSC 94-2220-E007-004 and 94-2220-E007-029)
64. H.-Y. Hu, P.-L. Chen,, and T.-Y. Chang, “A Wireless Digital IC Test System” Informal digest of VLSI/CAD Symp., pp. P150, Hualian, Taiwan, Aug. 2006. (MoEA 94-EC-17-A-01-S1-002.)
65. Y.-C. Lai, P.-L. Chen and T.-Y. Chang, “A High Performance AWGN Generator” Informal digest of VLSI/CAD Symp., pp. P156, Hualian, Taiwan, Aug. 2006. (NSC 94-2220-E007-029.)
66. C.-Y. Li, C.-Y. Chou, and T.-Y. Chang, “A Self-Referred Clock Jitter Measurement Circuit in Wide Frequency Range,” Proc. of Asian Test Symposium, pp. 313-317, Fukouka, Japan, Nov. 2006. (NSC 94-2220-E-007-004, NSC 94-2220-E-007-029)
67. P.-L. Chen, H.-H. Chiu, and T.-Y. Chang, “A Delay Fault Testing Framework on Core-Based System-on-Chip,” Informal digest of Workshop on RTL and High-level Testing (WRTL06), pp. 33-40, Fukouka, Japan, Nov., 2006. (NSC 95-2220-E-007-011, MoEA 93-EC-17-A-03-S1-0002)
68. P.-L. Chen, H.-H. Chiu, J.-W. Lin, and Tsin-Yuan Chang, “A Smart Delay Testing Framework based-on IEEE 1500,” Informal digest of European Test Symposium, pp. 113-118, Freiburg, German, May 2007. (MoEA 95-EC-17-A-03-S1-0002)
69. T.-Y. Chang, C.-Y. Li, and M.-H. Hu, “An Robust Time-to-Voltage Converter for PLL Jitter Measurement,” Informal digest of 1st VLSI Test Technology Workshop, pp. P2.4, Hsinchu, Taiwan, July, 2007. (NSC 95-2220-E-007-011 and NSC 95-2220-E-007-039)
70. C.-Y. Li, C.-F. Chien, and T.-Y. Chang, “High Speed and Low Cost Implementations in Mix-Column/InvMix-Column,” Informal digest of VLSI/CAD Symp., pp. 620-623, Hualian Taiwan, Aug. 2007. (NSC 95-2220-E-007-011)
71. W.-C. Lee, H.-C. Lin, and T.-Y. Chang, “A Novel CMOS Smart Temperature Sensor for On-Line Thermal Monitoring,” Informal digest of VLSI/CAD Symp., pp. 664-667, Hualian Taiwan, Aug. 2007. (NSC 95-2220-E-007-039)
72. H. C. Lin and T.-Y. Chang, “Analysis and Design of a Sliding Mode Controller for Buck Converters Operating in DCM with Adaptive Hysteresis Band Control Scheme” Proc. IEEE Power Electronics and Drive Systems (PEDS) Conf, 2007, pp. 372-377, Bangkok, Thailand. (NSC 96-2220-E-007-027)

73. C.-Y. Li, C.-F. Chien, J.-H. Hong, and T.-Y. Chang, "An Efficient Area-Delay Product Design for MixColumns / InvMixColumns in AES", in Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2008, pp. 503-506, Montpellier, France. (NSC96-2220-E-007-027)
74. H.-C. Lin, B.-C. Fung, and T.-Y. Chang, "A Current Mode Adaptive On-Time Control Scheme for Fast Transient DC-DC Converters" Proc. of ISCAS 2008, pp. 2602-2605, Seattle, USA. (NSC96-2220-E-007-027, MoEA 96-EC-17-A-01-S1-002, EI)
75. P.-L. Chen, Y.-C. Huang, and T.-Y. Chang, "IEEE 1500-Based Test Framework for At-Speed Testing of Multiple Clock Domains," Informal digest of VLSI/CAD Symp., pp. S11-5, Kenting Taiwan, Aug. 2008. (NSC 96-2220-E-007-027)
76. Y.-Y. Chen, H.-C. Lin, Y.-P. Chen, and T.-Y. Chang, "A Fully Digital Interface, On-line Thermal/Power Monitoring System" Informal digest of VLSI/CAD Symp., pp. S15-6, Kenting Taiwan, Aug. 2008. (NSC 96-2220-E-007-027)
77. P.-L. Chen, T.-Y. Chang, and Y.-C. Huang, "IEEE 1500-Based Delay Test Framework for At-Speed Testing of Multiple Clock Domains," Informal digest of Workshop on RTL and High-level Testing (WRTL08), pp. 19-22, Sapporo, Japan, Nov., 2008. (NSC 97-2220-E-007-017, MoEA 96-EC-17-A-01-S1-0002)
78. P.-L. Chen, H.-C. Lin, C.-H. Wang, W.-T. Wang, and T.-Y. Chang, "Wafer Level Burn-in Cost Reduction Using the Heat Generated by Test Patterns," Informal digest of Workshop on RTL and High-level Testing (WRTL08), pp. 41-44, Sapporo, Japan, Nov., 2008. (NSC 97-2220-E-007-017, MoEA 96-EC-17-A-01-S1-0002)
79. Y.-H. Chen and T.-Y. Chang, "High Performance DA-Based DCT with Error Compensated Adder Tree" Informal digest of VLSI/CAD Symp., pp. S1-1, Hualian, Taiwan, Aug. 2009. (NSC 97-2220-E-007-017.)
80. C.-Y. Li, T.-Y. Chang, and C.-C. Huang, "A Nonlinear PRNG Using Digitized Logistic Map with Self-Reseeding Method," Proc. IEEE VLSI-DAT Conf., pp. 108-111, Hsinchu, Taiwan, April 2010. (NSC 98-2221-E-007-095)
81. Y. H. Chen, T. Y. Chang, and R. Y. Jou, "A Statistical Error-Compensated Booth Multiplier and Its DCT Applications," Proc. of IEEE TENCON, pp. 1146-1149, Fukuoka, Japan, Nov. 2010. (EI, NSC 99-2221-E-007-119)
82. C.-Y. Li and T.Y. Chang, "InvMixColumn Byte-level Decomposition using Greedy Algorithm and Design of AES," Proc. of Int'l Congress on Computer Applications and Computational Science, Singapore, Dec. 2010. (NSC 98-2221-E-007-095 and NSC 99-2221-E-007-119)

83. S.-N. Tang, J.-W. Tsai, T.-Y. Chang, "An Energy-Efficient MMAS FFT Processor for High-Rate WPAN Applications," Proc. of 15th IEEE International Symposium on Consumer Electronics (ISCE), pp. 446-449, Singapore, June 2011. (NSC 99-2221-E-007-119)
84. Y.-H Chen and T.-Y. Chang, "Low-Error Fixed-Width Two's-Complement Multipliers with Statistical Compensation Circuit" Informal digest of VLSI/CAD Symp., pp. S1-3, Yunlin, Taiwan, Aug. 2011. (NSC 99-2221-E-007-119)
85. H.-C. Chiang, Y.-H Chen and T.-Y. Chang, "A Low-Cost Architecture for High-Throughput Multi-Path Transform in Video Compression Applications" Informal digest of VLSI/CAD Symp., pp. S1-4, Yunlin, Taiwan, Aug. 2011. (NSC 99-2221-E-007-119)
86. R.-Y. Jou, Y.-H Chen, T.-Y. Kao, and T.-Y. Chang, "A High-Performance Video Transform Engine by Using Simultaneous Forward and Inverse DCT" Informal digest of VLSI/CAD Symp., pp. P-1, Yunlin, Taiwan, Aug. 2011. (NSC 99-2221-E-007-119)
87. Y. H. Chen, T. Y. Chang, and C. W. Lu, "A Low-Cost and High-Throughput Architecture for H.264/AVC Integer Transform by Using Four Computation Streams," in Proc. IEEE ISIC, , pp. 380-383, Singapore, 2011. (EI)

III. Technical Reports

1. Chang, T.Y., "The Design of Testable Programmable Logic Arrays," M.S. Thesis, Michigan State University, June 1987.
2. Chang, T.Y. and C.L. Wey, "The Design of Testable Programmable Logic Arrays," Technical Report, Division of Engineering Research, Michigan State University, 1987.
3. Wey, C.L. and T.Y. Chang, " Design of Programmable Logic Arrays for Diagnosability," Technical Report, Division of Engineering Research, Michigan State University, 1988.
4. Chang, T.Y., " Design of Fault-Tolerant Programmable Logic Arrays for Yield Enhancement, " Ph.D. dissertation, Michigan State University, Dec. 1989.
5. Chang, T.Y., "Concurrent Testable Design for Fault-Tolerant RAM-based PLAs," Research report for National Science Council, NSC 80-0404-E007-18, 1991.
6. Chang, T.Y., "Design of Fault-Tolerant Systolic Array Multiplier with Time Redundancy," Research report for National Science Council, NSC 81-0404-E007-108, 1992.
7. 張慶元, 王柏森, "靜態電流定址設計及良率分析", 暑期計劃, NSC 83-0115-C007-01-024E, 1993.

8. 張慶元, 楊文助, "利用機率及簡化邏輯閘設計全加器之分析", 暑期計劃, NSC 83-0115-C007-01-025E, 1993.
9. Chang, T.Y., "Schemes for Detecting CMOS Analog Fault," Research report for National Science Council, NSC 82-0404-E-007-121, 1993.
10. Chang, T.Y., "The Array Multipliers Using Self-Dual Property," Research report for National Science Council, NSC 82-0404-E007-311, 1994.
11. Chang, T.Y., "Design and Analysis of a Fault-Tolerant DCVS Multiplier," Research report for National Science Council, NSC 83-0404-E007-018, 1994.
12. 張慶元, 郭中仁, "有限場常數測試乘法器模擬與實作", 暑期計劃, NSC 84-0115-C007-052E, 1994.
13. 張慶元, 童建勳, "自我對偶性陣列乘法器之模擬驗證", 暑期計劃, NSC 84-0115-C007-053E, 1994.
14. Chang, T.Y., "On the Design of Two C-Testable $GF(2^m)$ Multipliers," Research report for National Science Council, NSC 83-0404-E007-072, NSC 84-0404-E007-017, NSC 84-0404-E007-028, July 1995.
15. Chang, T.Y., "Diagnosis System Design of the Hardware Emulator (I)," Research report for National Science Council, NSC 84-2215-E007-043, Aug. 1995.
16. 張慶元, 張銓淵, "TTL型轉置邏輯可測度陣列乘法器之低功率運算設計", 暑期計畫, NSC 86-2815-C007-005-E, 1996.
17. Chang, T.Y., "TTL型轉置邏輯可測度陣列乘法器之低功率運算設計 (II)", Research report, NSC 85-2215-E-007-015, Dec 1996.
18. Chang, T.Y., "3V Digital Modem Chip Design" Research report, NSC 85-2221-E-007-040, Dec 1996.
19. Chang, T.Y., "Low-Power Array Multiplier by Applying Alternative Logic" Research report, NSC 86-2215-E-007-012, Dec 1997.
20. Chang, T.Y., "JAVA Chip Design (I)" Research report, NSC 87-2215-E-007-019, Oct. 1998.
21. Chang, T.Y., "JAVA Chip Design (II)" Research report, NSC 88-2215-E-007-031, Oct. 1999.
22. Chang, T.Y., "DFT and Test Strategy of SOC" Research report, NSC89-2215-E007-023, May 2000.
23. Chang, T.Y., "DFT and Test Strategy of SOC(II)" Research report, NSC89-2218-E007-065,

May 2001.

24. S.-S. Yang, J.-R. Huang, M.-J. Hsiao, T.-Y. Chang, C.-W. Lu, “Laser Driver for 1.25G,” Mblock Inc., Oct. 2001.

25. Chang, T.Y., “DFT and Test Strategy of SOC(III)” Research report, NSC90-2215-E007-044, Oct 2002.

26. Chang, T.Y., “晶圓嵌入式參數量測單元,” Research report, NSC 91-2622-E-007-026-CC3, Aug. 2003.

27. Chang, T.Y., “R&D on Functional Testing ATPG Technologies of Network Security Processor System-“, Research report, 91-EC-17-A-03-S1-0002, Aug. 2003.

28. Chang, T.Y., “單晶片系統參數量測裝置及液晶顯示器驅動電路省電設計研究” Research report, NSC91-2215-E007-038, Oct. 2003.

29. Chang, T.Y., “SOC可生產性設計：基礎設施IP之研發；子計畫二：記憶體及鎖相回路參數量測IP之研發” Research report, NSC 92-2220-E-007-003, May 2004.

30. Chang, T.Y., “SOC可生產性設計：基礎設施IP之研發；子計畫二：記憶體及鎖相回路參數量測IP之研發” Research report, NSC 93-2220-E-007-004, May 2005.

31. Chang, T.Y., “低功率都會無線網路設計關鍵技術研發：總計畫(1/3)” Research report, NSC 93-2220-E-007-024, May 2005.

32. Chang, T.Y., “低功率都會無線網路設計關鍵技術研發：子計畫五：都會無線網路內嵌式時序量測電路及雜訊產生器(1/3)” Research report, NSC 93-2220-E-007-029, May 2005.

33. Chang, T.Y., “低功率都會無線網路設計關鍵技術研發：總計畫(2/3)” Research report, NSC 94-2220-E-007-024, May 2006.

34. Chang, T.Y., “低功率都會無線網路設計關鍵技術研發：子計畫五：都會無線網路內嵌式時序量測電路及雜訊產生器(2/3)” Research report, NSC 94-2220-E-007-029, May 2006.

35. Chang, T.Y., “SOC可生產性設計：基礎設施IP之研發；子計畫二：記憶體及鎖相回路參數量測IP之研發(3/3)” Research report, NSC 94-2220-E-007-004, Oct. 2006.

36. Chang, T.Y., “奈米級晶片之良率與可靠度提昇方法研究-可靠度嵌入式溫度量測系統(1/3)” Research report, NSC 95-2220-E-007-039, May 2007.

37. Chang, T.Y., “低功率都會無線網路設計關鍵技術研發：子計畫五：都會無線網路內嵌式時序量測電路及雜訊產生器(3/3)” Research report, NSC 95-2220-E-007-011, Oct. 2007.

38. Chang, T.Y., “低功率都會無線網路設計關鍵技術研發：總計畫(3/3)” Research report,

NSC 95-2220-E-007-006, Oct. 2007.

39. Chang, T.Y., “奈米級晶片之良率與可靠度提昇方法研究-可靠度嵌入式溫度量測系統 (2/3)” Research report, NSC 96-2220-E-007-027, May 2008.

40. Chang, T.Y., “奈米級晶片之良率與可靠度提昇方法研究-可靠度嵌入式溫度量測系統 (3/3)” Research report, NSC 97-2220-E-007-017, July 2009.

41. Chang, T.Y., “適用於多重通訊應用的高效能，低功率之整合型傅立葉轉換電路設計(I)” Research report, NSC 98-2221-E-007-095, Aug. 2010.

42. Chang, T.Y., “支援 MPEG/H.264/VC-1 多協定轉換運算單元 (I)” Research report, NSC 99-2221-E-007-119, Oct. 2011.

IV. Patents

1. 楊紹聖，張慶元，_“浮點正規化的前置零計數裝置” 新型第一六九三四三號，專利期限自中華民國九十年二月一日至中華民國九十九年九月十七日止。
2. 李仲益，張慶元，黃英叡 “高速二進位加法器之同位元產生裝置” 新型第一七七一〇〇號，專利期限自中華民國九十年六月二十三日至中華民國九十九年十月一日止。
3. 張慶元，蕭鳴鈞，楊紹聖，黃英叡 “使用單一漣漪進位加法器之進位選擇加法器眾裝置” 新型第195155號，專利期限自中華民國九十一年十月一日至中華民國一〇〇年三月二十五日止。(NSC88-2215-E007-031).
4. 張慶元，蕭鳴鈞，黃英叡 “嵌入式 CMOS 時間間距量測裝置及測試方法” 發明專利 182833號，專利期限自中華民國九十二年七月一日至中華民國一〇〇年十一月五日止。(NSC90-2215-E007-044)
5. 張慶元，蕭鳴鈞，蔡政宏 “數位至類比轉換器之嵌入式內建自我測試裝置及測試方法”，發明專利第一七九三七五號，專利期限自中華民國九十二年五月十一日至中華民國一一〇年十二月三日止。(NSC90-2215-E007-044)
6. 張慶元，蕭鳴鈞，李書榮 “嵌入式記憶體擷取時間量測方法及裝置”，發明專利I229343號，專利期限自2005年3月11日至2022年11月26日止. “Integrated circuit device with a built-in detecting circuit for detecting maximum memory access time of an embedded memory,” USA patent 6873557, March 29, 2005. (NSC90-2215-E007-044)
7. 張慶元，羅浩榮，楊紹聖，“改良Earle 門鎖設計” 發明專利I228349號，專利期限自2005年2月21日至2023年4月20日止. (NSC 91-2215-E-007-038 and MoEA 91-EC-17-A-03-S1-0002). “Feedback Latch Circuit and Method Therefor Cross-Reference to Related Application,” USA patent 6,791,387, Sept. 14, 2004.

8. 張慶元，蕭鳴鈞，黃英叡，“雙斜率積分器之控制方法及其裝置”(Method and Apparatus for Controlling a Dual-Slope Integrator Circuit to Eliminate Setting Time Effect Cross-Reference to Related Application) 發明專利204310號，專利期限自2004年6月11日至2023年7月27日止。(90-2215-E007-011, MoEA 91-EC-17-A-03-S1-0002), USA patent 6,914,471, July 5, 2005.
9. 張慶元，楊紹聖，莫凱圳，“一種定範圍待測時間轉換方法”發明專利 I227897 號，專利期限自2005年2月11日至2023年12月9日止。(NSC 92-2220-E-007-003)
10. 張慶元，楊興宗，黃英叡，“亂數產生方法及數位式亂數產生器”發明專利I246016號，專利期限自2005年12月21日至2024年10月27日止。(NSC 93-2220-E-007-029 and MoEA 92-EC-17-A-03-S1-0002)
11. 張慶元、陳柏霖、邱灝軒，“延遲錯誤測試裝置”發明專利I297825號，專利期限自2008年6月11日至2025年2月26日止。(NSC 95-2220-E-007-011, MoEA 93-EC-17-A-03-S1-0002)

.

V. Books

1. 翁通楹等94位，力學名詞辭典 (全二冊)，國立編譯館主編，俊傑書局股份有限公司印行，台北市 Dec. 2002.