

**Publication List of professor Hao-Yung Lo,
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Part A

- A1. ***Hao-Yung LO** and Yoshina O Aoki, "Generation of a Precise Binary Logarithm with Difference Grouping Programmable Logic Array". IEEE Transaction On Computers, vol. C-34, No. 8, August 1985, pp. (A1)1-10.

Part B

- B1. ***Hao-Yung LO**, Hsiu-Feng Lin, Chichyang Chen , Jenshiuh Liu and Chia-Cheng Liu . "Built-in Test with Modified-Booth High-Speed Pipelined Multipliers and Dividers", Journal of Electronic Testing : Theory and Applications 19, 2003. pp. (B1)1-25.
- B2. *S.-S. Yang, **H.-Y. LO**, T.-Y. Chang and T.-L. Jang , "Earle Latch Design For High Performance Pipeline" . IEE Proc. Comput. Digit. Tech. Vol. 149, No. 6, November 2002, pp. (B2)1-4.
- B3. ***Hao-Yung LO**, Tsin-Yuan Chang and Ming-Che Lee, "Parallel Unidirectional Division Algorithms and Implementations". Journal of the Chinese Institute of Engineers, Vol. 24, No. 4, 2001, pp. (B3)1-10.
- B4. ***Hao-Yung LO**. "A Uniform and Squared Direct Two's Complement Multiplier". Journal of Information Science and Engineering 13, (1997). pp. (B4)1-9.
- B5. ***Hao-Yung LO** and Jian-Da Chen, "A Routing Algorithm and Generalization for Cube-Connected Cycle Networks". IEICE TRANS. INF. & SYST. , Vol. E80-D, No. 9, September 1997. pp. (B5)1-8.
- B6. ***Hao-Yung LO**, Hsiu-Feng Lin and Yue-Yuan Ho, "Logarithmic Conversion by Four Partitioned Hybrid-ROMs". IEEE 1996, pp. (B6)1-4.
- B7. *Hsiu-Feng Lin, **Hao-Yung Lo** and Jung-Shiarn Shy, "A Novel Hybrid CORDIC Algorithm with A Variable Scalar Factor for Sine and Cosine Computation". IEEE July, 1997. pp. (B7)1-4.

- B8. *Hsiu-Feng Lin , **Hao-Yung Lo** and Jung-Shiarn Shy, "A High-speed of Self-Timing Carry-Completion for Direct Two's Complement Multipliers". 0-7803-5146-0/98/\$10.00, 1998 IEEE. pp. (B8)1-4.
- B9. ***Hao-Yung Lo**, Tsin-Yuan Chang, Yiwen Wang, "A Unidirectional Cordic Algorithm for Angle Computation and rotation", Journal of the Chinese Institute of Engineers, Vol. 20, No. 6, (1997). pp. (B9)1-7.
- B10. ***Hao-Yung LO** ,"An Implementation of The Conditional-Sum Scheme Embedded in A Signed Digital Adder". Journal of the Chinese Institute of Engineers, Vol. 19, No. 5, (1996). pp. (B10)1-10.
- B11. ***Hao-Yung LO** , and Lon-Ping Ju, "A New Design of A Balanced and Self-Purging Cascaded N-Module Redundancy (NMR)". Journal of the Chinese Institute of Engineers, Vol.18, No. 1, (1995). pp.(B11)1-24.
- B12. ***Hao-Yung Lo**, "An Optimal Matched and Parallel Mixed-Radix Converter". Journal of Information Science and Engineering 10, (April, 1994). pp. (B12)1-8.
- B13. ***Hao-Yung Lo**, Tsin-Yuan Chang, Hsiu-Feng Lin and Jen-Shiuh Liu ,"An Efficient Design with Structure in Parallel of Self-Checking Checker for Any m-out-of-n Codes". pp. (B13)1-36.
- B14. *Jing-Reng Huang, Tsin-Yuan Chang, Cheng-Hsun Liu and **Hao-Yung Lo**, "A Novel TSC checker for Berger Code". pp. (B14)1-22.
- B15. ***Hao-Yung Lo**, Tsin-Yuan Chang and Jen-Shiuh Liu, "Two High-speed Carry-Through Adders in Parallel Computation". pp. (B15)1-32.
- B16. ***Hao-Yung Lo** , Tsin-Yuan Chang , and Hsiu-Feng Lin , "Parallel Algorithms for Residue Scaling and Error Correction in Residue Arithmetic". pp. (B16)1-29.
- B17. ***Hao-Yung Lo**, Jen-hsiuh Liu, Hsiu-Feng Lin and Tsin-Yuan Chang, "Multi level and Multi thread algorithm for Markov Model – A New Algorithm for MTBF in NMR system". (July 23, 2003). pp. (B17)1-24.

- B18. *Shyi-Shiun Kuo, Hsiu-Feng Lin and **Hao-Yung Lo**, "Systolic Residue Number System Processing". Proceedings of National Computer Symposium 1991. pp.(B18)1-8.
- B19. *Chiang-Shiang Wan, Hsiu-Feng Lin and **Hao-Yung Lo**, "Hybrid ROMs Strategy (H-ROM) for Conversion Between Binary Numbers and Logarithms". Proceedings of National Computer Symposium 1991. pp. (B19)1-8.
- B20. *Chien-Chun Su and **Hao-Yung Lo**, "An Algorithm for Scaling and Single Residue Error Correction in Residue Number Systems". IEEE Transactions on Computers, Vol. 39, No. 8, August 1990. pp. (B20)1-12.
- B21. ***H-Y LO**, L-P JU, C-C SU, "General Version of reconfiguration N modular redundancy system". IEEE Proceedings Vol. 137. PT. G. No.1, February 1990. pp. (B21)1-4.
- B22. *Yen-Tseng Hsu, Chen-Fa Hsu, **Hao-Yung Lo** and Chien-Chung Su, "Novel high reliability bus level voted microcomputer system". INT. J. Electronics, 1990, Vol. 68, No. 4. pp. (B22)1-12.
- B23. ***Hao-Yung Lo**, "High-speed signed digital multipliers for VLSI". North-Holland Microprocessing and Microprogramming 29 (1990). pp. (B23)1-12.
- B24. *Chien-Chun Su, Lon-Ping Ju and **Hao-Yung Lo**, "Brief communication Priority switch design for hybrid redundancy system". INT. J. Electronics, 1989, Vol. 66, No. 6. pp. (B24)1-27.
- B25. ***Hao-Yung Lo** and Chien-Chun Su, "A distributive D-algorithm for generating the test pattern for faulty combinational circuit". INT. J. Electronics, 1989, Vol. 66, No. 1. pp. (B25)1-8.
- B26. ***Hao-Yung Lo** and Jau-ILng Chen, "Microstep of digital for step motor and its test using a laser interferometer measurement system". INT. J. Electronics, 1987, Vol. 62, No. 5. pp. (B26)1-20.

- B27. ***Hao-Yung Lo** and Fang Hsu, "A combinational word-parallel and bit-parallel associative processor". INT. J. Electronics, 1989, Vol. 62, NO. 4. pp. (B27)1-10.
- B28. ***Hao-Yung Lo**, Chien-Chun Su, and James. H.W. Tseng, "Double-Speed Quasi-serial Multiplier" Int. J. Electronics, 1989, Vol. 67, No. 4, (B28) 1-10.
- B29. ***H.Y. Lo**, J.H.Lu, Y.Aoki, "Programmable variable-rate up/down counter for generating binary logarithms". IEE Proceedings, Vol. 131, Pt. E, No. 4, July 1984. pp (B29)1-7.
- B30. ***Hao-Yung Lo** and Jau-Huei Lu, "An improved non-restoring array divider with carry-save and carry-look-ahead techniques". INT. J. Electronics, March 1987, Vol. 62. pp. (B30)1-8.
- B31. ***Hao-Yung Lo** and Jau-Ling Chen, "A Hardwired Generalized Algorithm for Generation the Logarithm Base-k Iteration". 0018-9340/87/1100-1363\$01.00, 1987 IEEE. pp. (B31)1-5.
- B32. ***Hao-Yung Lo** and Yoshinao Aoki, "Subtractions Used On Multiple- Valued Booth Algorithm for Quaternary Multiplication". 昭和 57 年電器四學會北海道支部連會大會. pp.(B32)1-2.
- B33. ***Hao-Yung Lo**, Der-Ling Tseng and Yoshinao Aoki, "A New Design of An Iterative Array for Multiplication of Signed Binary and Quaternary Digital Number Systems". Reprinted Proceedings of the Twelfth International Symposium Multiple-Valued Logic, May 1982. pp. (B33)1-8.
- B34. ***Hao-Yung Lo** and Yoshinao Aoki, "Microcomputer-Based Multichannel Counting System for Reducing Non-Paralysable Idle Time". 昭和 58 年度電子通信學會總會全國大會. 1983, pp. (B34).
- B35. ***Hao-Yung Lo**, "An Improvement of Nonrestoring Array Divider with Carry-Save and Carry Lookahead Techniques". pp. (B35)1-9.

- B36. *Der-Ling Tseng, **Hao-Yung Lo**, "An Extended Booth Algorithm for High Speed Multiplication Process". 電工雙月刊 July 1984. pp. (B36)1-6.
- B37. ***Hao-Yung Lo**, Ching-shen Su, "Design of Microcomputer-Based Data Acquisition System for the Time-of-Flight Ion Scattering Spectrometer". Nuclear Instruments and Methods 186(1981), North-Holland Company. pp. (B37)1-4.
- B38. ***Hao-Yung Lo**, Ching-sun Su, "Development of Analytical System for the Measurement of Energy and Intensity in Ion Scattering Spectrometer". 核子科學 第十八卷第二期, 中華民國七十六年六月. pp. (B38)1-5.
- B39. *羅浩榮, 徐正一, 汪維明, "座標旋轉法計算處理機之設計及速度之改進". 中國工程, January 1980, pp. (B39)1-9.
- B40. *陳康桐, 羅浩榮, "A Simplest Hardware System For Fixed Point Division", 中國工程 1980 年 9 月. pp (B40)1-5.
- B41. 楊覺民、羅浩榮, "自變電感器之設計", 電工季刊(B41), pp.1-3.
- B42. *Hao-Yung Lo, Ching-Shen Su, Teng-Yi Hsu, Lun Wang, "A Design Technique of Low Cost but High Quality Peak Stretcher", 核子科學十八卷一期中華民國七十年三月. pp (B42)1-6.
- B43. ***Hao-Yung Lo**, "Generalized Fault Detection for Multivalued Logic Systems". pp. (B43)1-9.
- B44. ***Hao-Yung Lo**, Jau-Huei Lu, "A Simple Design for a Digital Programmable Frequency Multiplier". INT. J. ELECTRONICS. 1979. vol. 46. NO. 5. 535-542. pp. (B44)1-8.
- B45. ***Hao-Yung Lo**, "Digital Display of Stepper Motor Rotation". Computer Design, April 1978. pp. (B45)1-4.
- B46. ***Hao-Yung Lo**, "A compromise Between Speed and Complexity in a BCD Adder". INT. J. ELECTRONICS. 1979. vol. 46. No. 1. pp. (B46)1-5.

- B47. ***Hao-Yung Lo**, "Up/Down Counter for Converting Binary-to-BCD and BCD-to-Binary". INT. J. ELECTRONICS. 1978. vol. 45. NO. 2. pp.(B47)1-7.
- B48. ***Hao-Yung Lo**, "Simple Circuit Generates Selected Number of Pluses". APPLIED IDEAS, Electronic Engineering, April 1976. pp. (B48)-1.
- B49. ***羅浩榮**, 盧朝輝, 李志浩, 莊長富, 張朝榮, 朱宏文, 楊士正, "精密步階式馬達運轉監視系統". 中國工程, 1978 年 5 月. pp. (B49)1-5.
- B50. ***Hao-Yung Lo**, "Binary Logarithms for Computing Integral and Non-Integral Roots and Powers". INT. J. ELECTRONICS. 1976. vol. 40. NO. 4. pp. (B50)1-8.
- B51. ***Hao-Yung Lo**, "A Method for Simplifying the Multi-Output Networks". 中國工程, 1975 年 7 月. pp. (B51)1-3.
- B52. ***Hao-Yung Lo**, "A Relay Tree Method for Simplifying Boolean Function". AEU Japan, 1975 年 1 月, pp10-13. pp. (B52)1-4.
- B53. ***羅浩榮**, "The Recognition and Identification of Symmetric Switching Functions With the Use Interchanging Map". 中正電機 1973 年 6 月. pp. (B53)1-13.
- B54. ***Hao-Yung Lo**, "To Solve the Equation With A Computer By Graffe's Root-Squaring Method". 無線電技術季刊, 1973 年 3 月. pp. (B54)1-7.
- B55. ***Hao-Yung Lo**, "應用於步階馬達加速/減速之數字式控制器". 電工雙月刊第二十一卷第三期. pp. (B55)1-10.

Part C. 最近五年著作(2002-2007)

- C1. **HAO-YUNG LO**, HSIU-FENG LIN, CHICHYANG CHEN, JENSHIUH LIU and CHIA-CHENG LIU, “Built-in Test with Modified-Booth High-Speed Pipelined Multipliers and Dividers”. Journal of Electronic Testing: Theory and Applications 19, 245-269, 2003.
- C2. S.-S. Yang, **H.-Y. Lo**, T.-Y. Chang and T.-L. Jong, “Earle latch design for high performance pipeline”, IEE Proc. Comput. Digit. Tech. Vol. 149, No. 6, November 2002, pp. (B2) 1-4.
- C3. **Hao-Yung Lo**, Hsiu-Feng Lin, Chichyang Chen, Jenshiuh Liu, Shao-Sheng Yang and Tsin-Yuan Chang, “A Novel High-speed Serial/Parallel Two’s Complement Multiplier/Divider”, submitted to IEEE Transaction on Computers.
- C4. **Hao-Yung Lo**, Hsiu-Feng Lin and Jian-Houng Lee, “New Algorithms for Residue Scaling and Error Correction”, submitted to IEEE Transaction on Computers.
- C5. **Hao-Yung Lo**, Tsin-Yuan Chang, Hsiu-Feng Liu, Jenshiuh Liu and Jia-Hong Chen, “An Efficient Design with Structure in Parallel of Self-Checking Checker for Any m-out-of-n Codes”, submitted to IEE Proc.-Comput. Digit. Tech.
- C6. **Hao-Yung Lo**, An Efficient Structure for Module $\langle 2^n+1 \rangle$ Multiplication, (unpublished, preliminary version.)
- C7. **Hao-Yung Lo**, $\langle 2^n+k \rangle$ Module Multiplication, (unpublished, preliminary version.)
- C8. **Hao-Yung Lo**, TSC NMR, (unpublished, preliminary version.)