JOURNAL PUBLICATIONS & SPECIAL HIGHLIGHTS:

1. Agashiwala K, Jiang J, Kumar, A, **Yeh, C.-H.**, Banerjee, K., Sustaining Moore's Law with graphene. ***Chip Scale Review***, November/December, 2021 (ChipScaleReview.com)

2. Parto, K., Pal, A., Chavan, T., Agashiwala, K., **Yeh, C.-H.**, Cao, W., Banerjee, K., One-Dimensional Edge Contacts to Two-Dimensional Transition-Metal Dichalcogenides: Uncovering the Role of Schottky-Barrier Anisotropy in Charge Transport across MoS_2/Metal Interfaces. ***Phys. Rev. Appl.***, 2021, 15, 064068. (IF=4.194, https://doi.org/10.1103/PhysRevApplied.15.064068)

3. *__Yeh, C.-H.__; *Zhang D. J.; Cao W.; Banerjee, K. 0.5T0.5R - Introducing an Ultra-Compact Memory Cell Enabled by Shared Graphene Edge Graphene Edge-Contact and h-BN Insulator. ***IEEE International Electron Devices Meeting***, 2020, 12.3.1–12.3.4. (*equal contribution) (10.1109/IEDM13553.2020.9371902)

4. *Zhang D. J.; *__Yeh, C.-H.__; Cao W.; Banerjee, K. 0.5T0.5R - An Ultra-Compact RRAM Cell Uniquely Enabled by van der Waals Heterostructures. ***IEEE Trans. Electron Devices***, 2020, 68, 2033-2040. (*equal contribution)
(IF=2.913, 10.1109/TED.2021.3057598)

   - **Highlighted** by ***Nature Electronics*** "Transistors and memory get together" (Vol. 4, 321, May 2021)
     nature.com/articles/s41928-021-00596-8

5. Agashiwala, K.; Jiang, K.; **Yeh, C.-H.**; Parto, K.; Zhang D. J.; Banerjee, K. Reliability and Performance of Multi-Level Subtractive Etched CMOS-compatible Graphene Interconnects. ***IEEE International Electron Devices Meeting***, 2020, 31.1.1-31.1.4. (10.1109/IEDM13553.2020.9371986)

6. Agashiwala, K.; Jiang, K.; Parto, K.; Zhang D. J.; **Yeh, C.-H.**; Banerjee, K. Demonstration of CMOS-Compatible Multi-Level Graphene Interconnects With Metal Vias. ***IEEE Trans. Electron Devices***, 2020, 68, 2083-2091. (IF=2.913, 10.1109/TED.2021.3061637)

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