National Tsing Hua University
Department of Electrical Engineering
EE4292 IC Design Laboratory (積體電路設計實驗)
Fall 2018

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Course Description

This course provides a basic but complete digital cell-based design flow with an advanced cell library. It is about how to implement your ideas into silicon through many abstraction layers (Idea → Hardware Description Language → Gate-level Netlist → Physical Layout) and also how to make sure the function and performance are met. Essential techniques and CAD tools will be taught, including Verilog HDL, logic synthesis, and physical placement and routing.

Prerequisites: Logic Design, Introduction to Integrated Circuits Design

Teaching Method

Lectures are given at DELTA 201R to introduce technical details, and hands-on labs at workstation classroom (EECS 407) are required for exercising. The connection between CAD tools is strong, so intense practice of each taught tool will be demanded. There will be **five** homework assignments and one term project. The weekly-based labs will teach you the basics of the tools; however, you have to keep practicing on the homework assignments and term project on your own. The Synopsys SAED 28nm cell library will be used throughout this course.

(***Note***: The library and tools are all very precious resources. Without CIC and the generous software providers, we will be unable to access them. So, please use them very carefully and only for this course.)

Evaluation

Lab (15%)
Homework (55%)
Term Project (30%)

Note:

1. For each lab, there will be checkpoints for examination.
2. One original work deserves only one credit. For example, if five students deliver the same (or very similar) results for homework or midterm, the grades will be averaged by five. If the

original work deserves 100 points, each one will get only 20 points. Rebuttal is allowed.

3. Five home assignments will be given. The grading equation for late delivery is

$$\text{New grade} = (\text{original grade}) \times 0.9^{(\text{delievery date} - \text{due date})}$$

4. Project: Build your own chip for some digital functions. Details will be disclosed on **11/22**. **No late delivery is allowed**.

Syllabus

Date	Week	Lecture (台達201)	Lab (資電407)	HW out	HW due
9/13	1	Overview: Syllabus and Introduction	Lab01: Workstation		
9/20	2	Verilog (I): Verilog Fundamentals (CVLM module 3~9)	Lab02: Verilog simulator (NC-Verilog)		
9/27	3	Verilog (II): Verilog for Verification (module 10~12, 20~22)	Lab03: Testbench debugging and writing (+CPU Intro)	1	
10/4	4	Verilog (III): Verilog for Synthesis (module 13~17)	Lab04: Debug platform (Verdi) + FSM exercise		
10/11	5	Verilog (IV): RTL Coding Guidelines	Lab05: RTL simulation and debugging	2	1
10/18	6	*No lecture*	Lab06: Line-based image processing example		
10/25	7	Synthesis (I): Synopsys Design Compiler	Lab07: Design Compiler	3	2
11/1	8	*No lecture*	Lab08: Coding for synthesis and optimization (I)	4	3
11/8	9	Synthesis (II): Optimization for Synthesis	Lab09: Coding for synthesis and optimization (II)		
11/15	10	Place & Route (I): Physical Design Flow	Lab10: ICC - Floorplan	5	4
11/22	11	Place & Route (II): Synopsys IC Compiler **Project Annoucement**	Lab11: ICC - Power plan, placement, CTS and routing		
11/29	12	Design Examples	Lab12: ICC - CTS, routing, verfication, power analysis		
12/6	13	*No lecture*	*No lab*		5
12/13	14	*No lecture* **Project Proposal**	*No lab*		
12/20	15	*No lecture*	*No lab*		
12/27	16	*No lecture*	*Project Consulting*		
1/3	17	**Project Presentation - Front-End Design**			
1/10	18	*No lecture*	*Project Consulting*		
1/17	19	**Project Presentation - Final Design**			

CVLM: Cadence Verilog Lecture Manual

Tool

HDL simulation: NC-Verilog
Synthesis: Design Compiler
P&R: IC Compiler
Debug/Verification: Verdi, nLint

Textbook

None.

References

Lecture notes will be provided and based on

- Cadence Lecture Manuals for Verilog (only in paper format)
- M. Keating and P. Bricaud, *Reuse Methodology Manual for System-on-a-Chip Designs*, Springer, 2007.
- CIC course lecture notes and labs

Note

The SAED library and Cadence lecture notes are only accessible and available for the students who are enrolled in this course. Any misuse of them is prohibited, including copy and redistribution.

Course Link

iLMS website

Teaching Assistant

TBD