Laboratory for Reliable Computing

Signal Sensing and Application Laboratory

Nano-Watt Ultra-Low-Voltage SAR ADC Design

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Outline

- nW SAR ADC Applications
- Optimal Supply Voltage and Design Challenges
- Low Power Design Techniques of SAR ADC
- Conclusions

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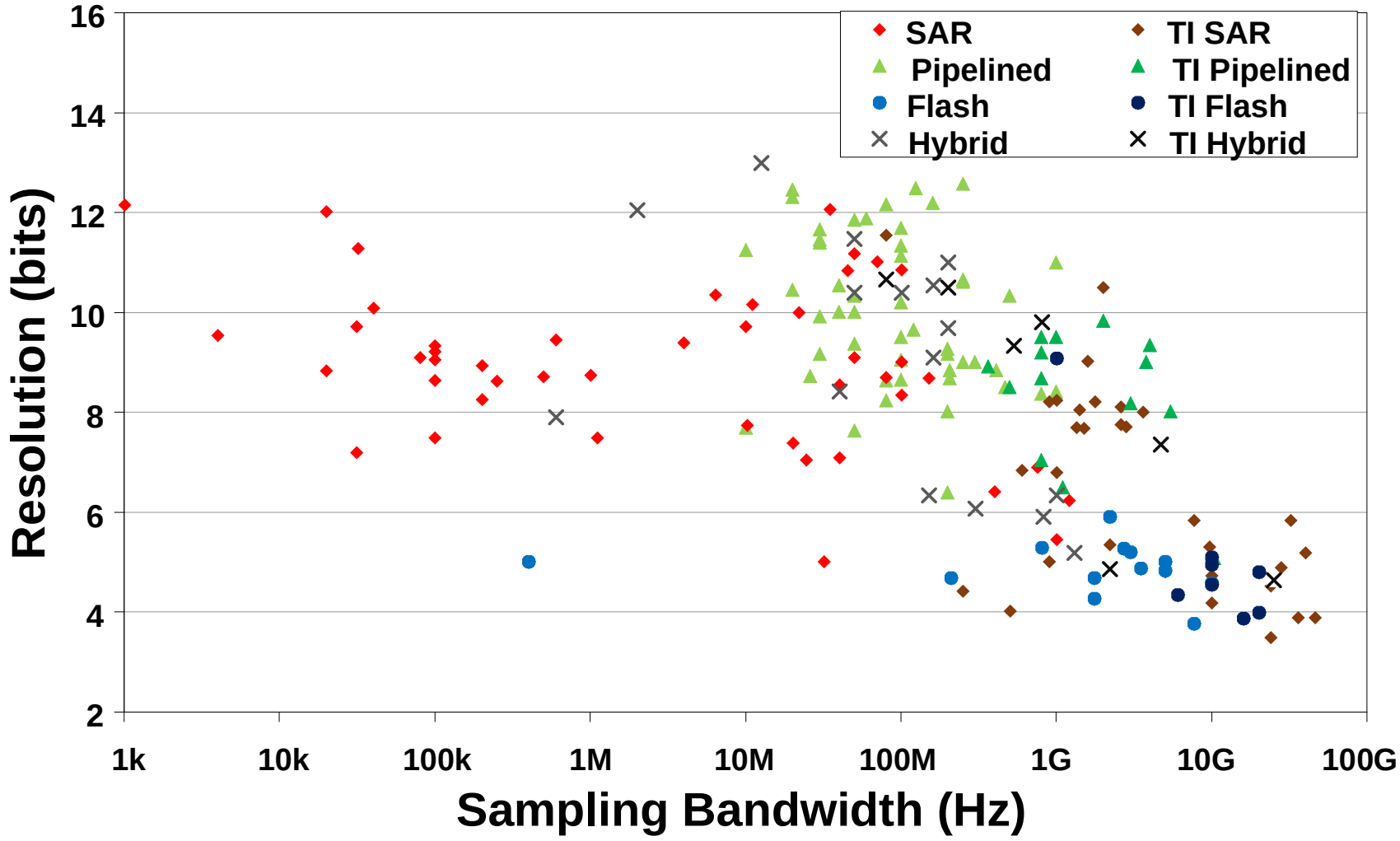
nW ADC Applications

- Battery-operated/always-on devices
  - Internet of things (IoT)
  - Wireless sensor network (WSN)
- Low power SoC
  - Low-voltage & efficient design
  - Digital design: speed and power tradeoff
  - Analog design: performance degradation
- ADC's requirements for IoT applications [1]
  - Ultra-low power ➔ ultra-low voltage operation (OpAmp not available)
  - Medium conversion rate : kS/s – MS/s
  - Medium resolution : 8b – 14b
  - Good efficiency (FoM)

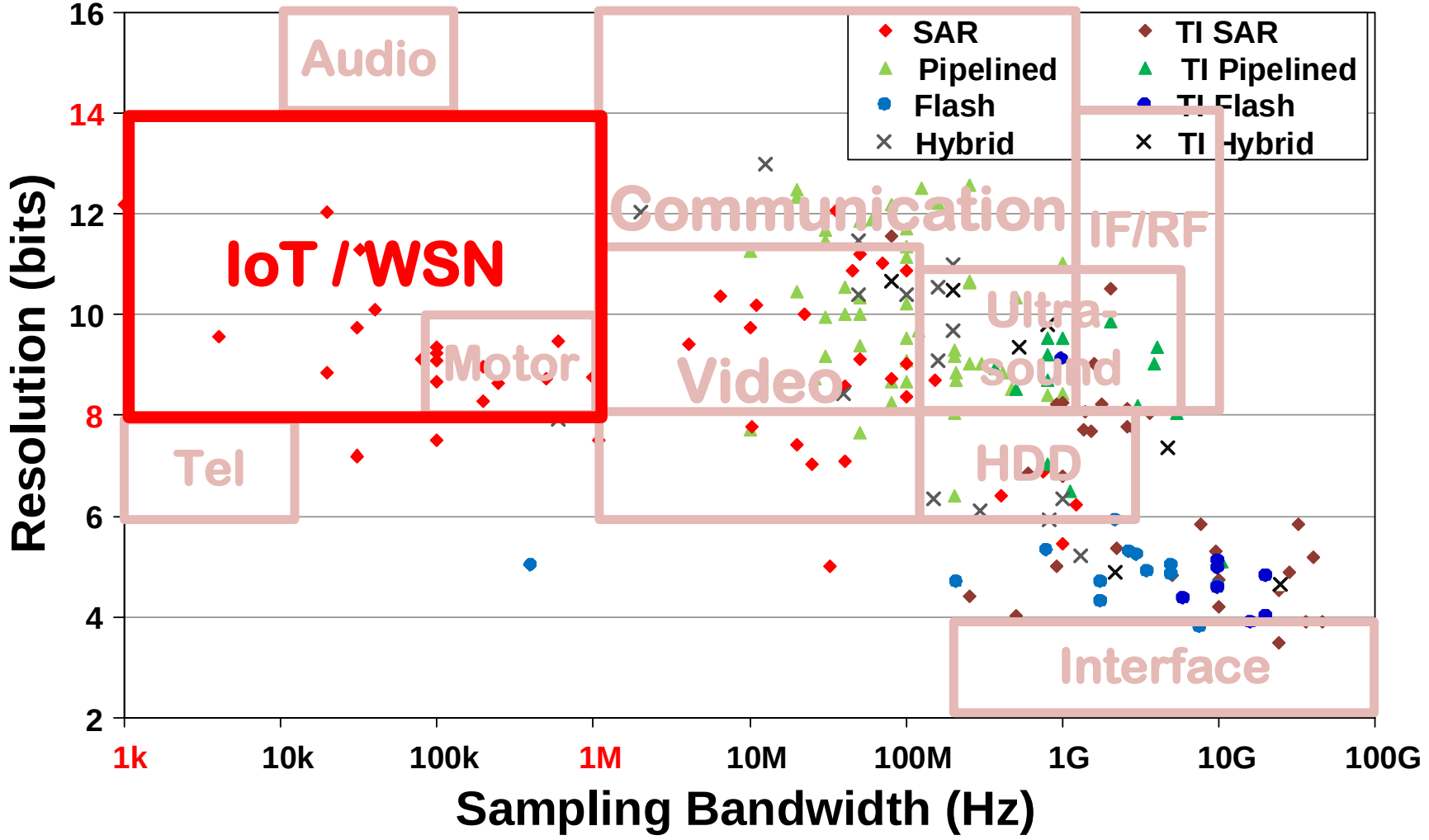
Nyquist ADCs (2006 – 2017)

[1]

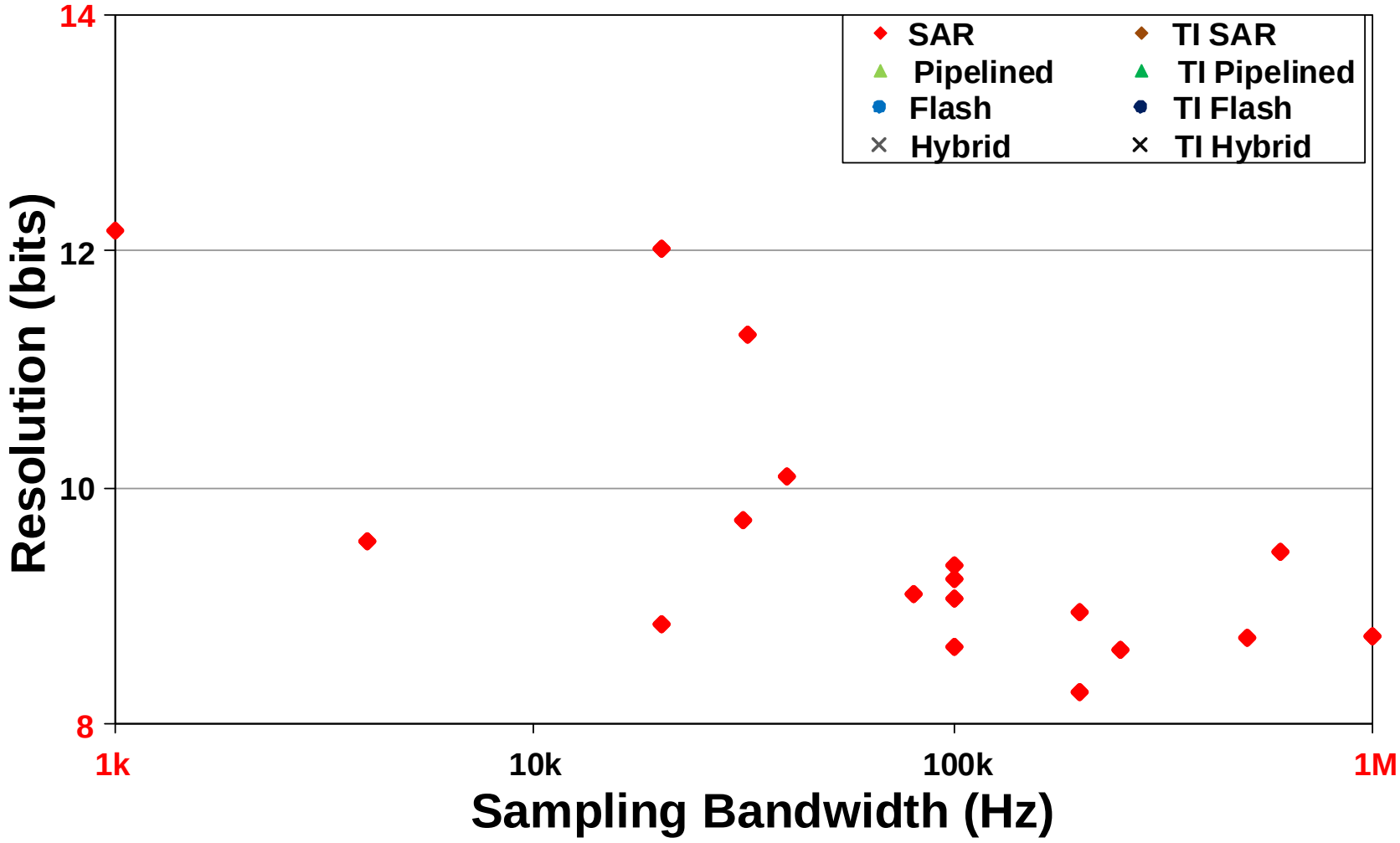


Nyquist ADCs (2006 – 2017)

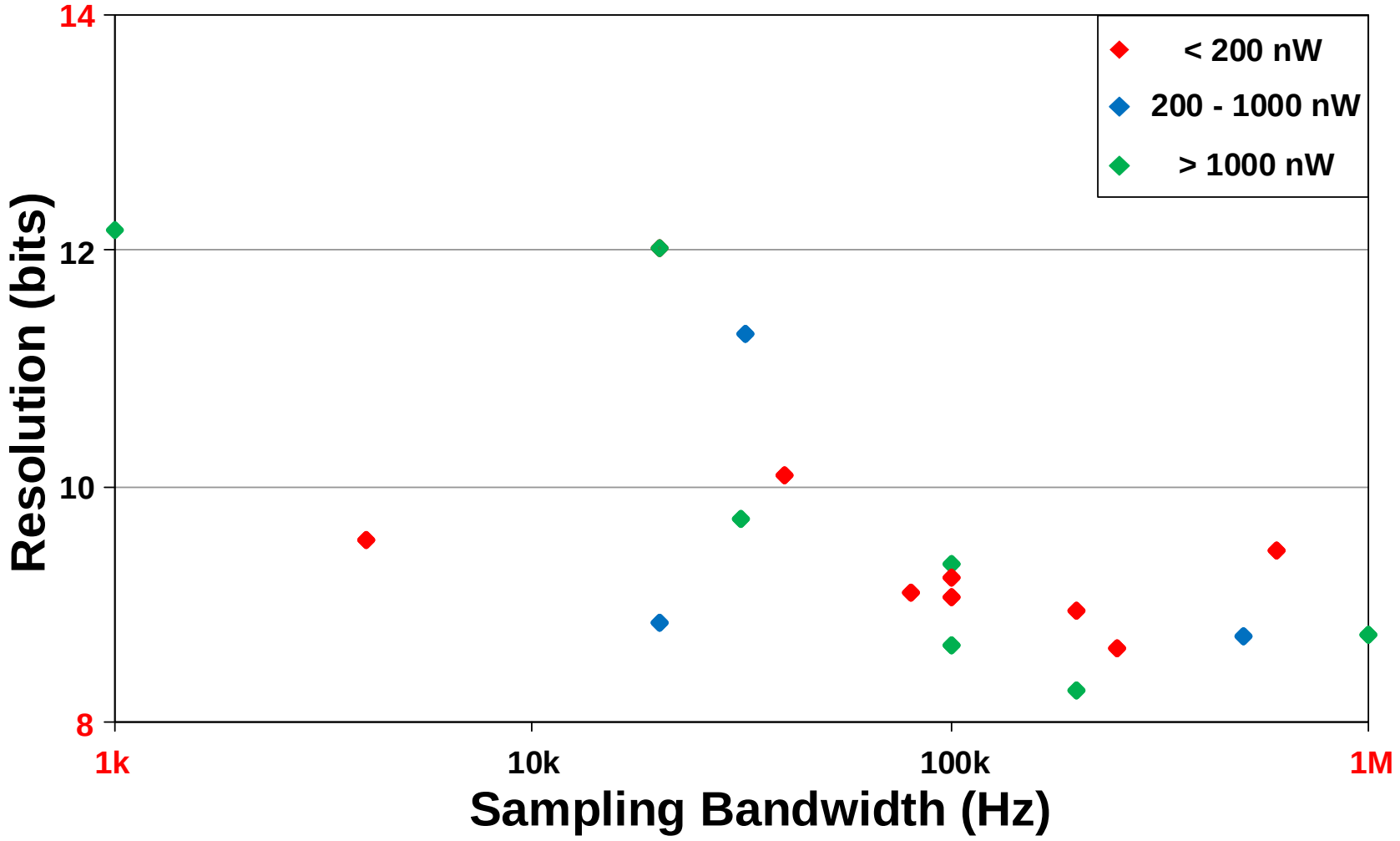
[2]



Best Candidate: SAR ADC (no OpAmp)



Demands of Nano-Watt ADC



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- Low Power Design Techniques of SAR ADC
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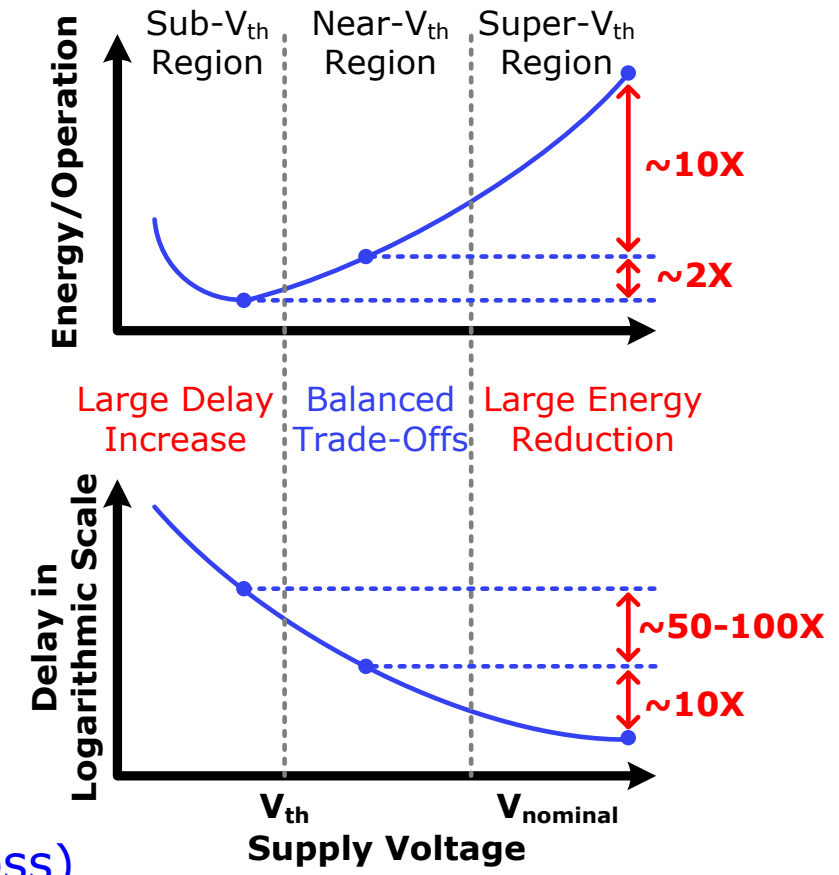
Optimal Supply Voltage

- Digital circuit
  - Dynamic power versus leakage
  - Optimal supply: 0.3~0.5V (90nm&40nm)
  - Delay burden
- Analog circuit
  - Reduced supply from 1V to 0.3~0.5V
  - Performance degradation (BW, Gain, Swing)
  - Noise requirement increases
- For low-power SoC (Digital > Analog) consideration
  - Ultra-low voltage (ULV) operation is preferred
  - Assuming single supply operation (no LDO regulator loss)

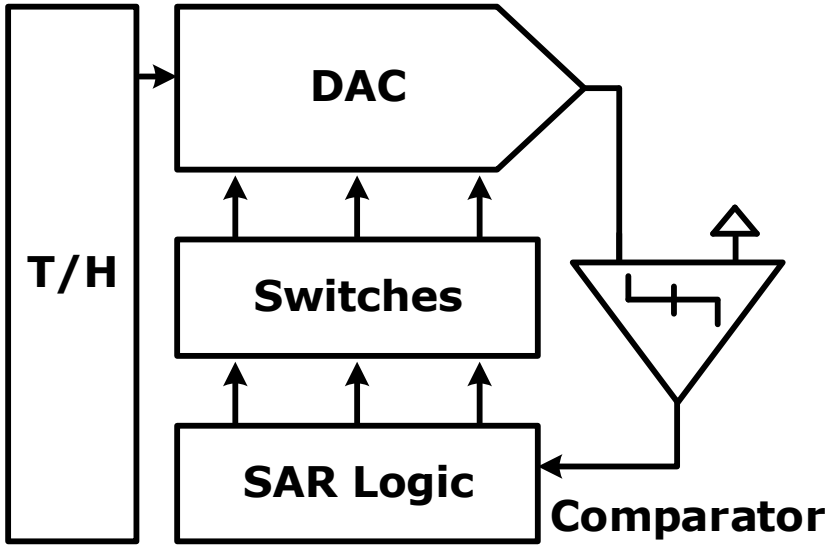
[3]



Low Voltage = Low Power?

- Digital circuit
  - V_{DD} ↓ ➔ $P_{dynamic} = f_s C V_{DD}^2$ ↓ (with same f_s)
  - Dynamic power reduction ☺
- Analog circuit (thermal noise dominated case)
  - V_{DD} ↓ ➔ V_{swing} ↓ ➔ SNR ↓
  - Reduce V_{DD} by 2 ➔ smaller LSB (÷2) ➔ SNR -6dB
  - To compensate SNR ➔ increase C by 4 (noise bandwidth ↓) ➔ no power benefit ☹
- Secondary effect
  - V_{DD} ↓ ➔ R_{ON}/R_{OFF} ↑ ➔ Speed ↓ & Leakage Power ↑
  - Flicker & latch noise in comparator ➔ C×4 ≠ SNR+6dB
  - ADC FoM degrades at ULV operation ☹

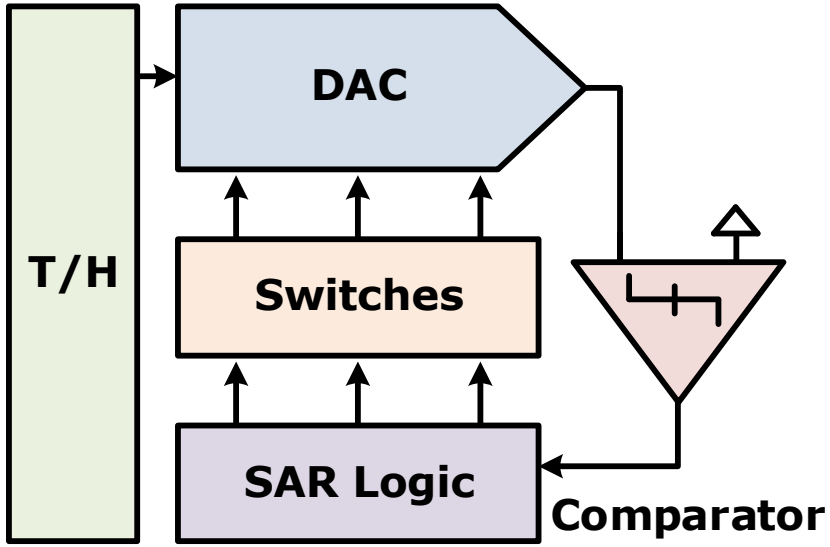
Building Blocks of SAR ADC



- Track & Hold (T/H) : input signal sampling
- DAC : level shift generation by charge conservation
- Switches : charge transfer control for DAC
- Comparator : polarity decision
- SAR logic : successive approximation operation

Design Challenges of SAR ADC

T/H :
- Speed
- Distortion
- Charge Injection
- Clock Feedthrough
- Leakage
- Signal Coupling
- Jitter



Comparator :
- Speed
- Resolution
- Noise
- Overdrive Recovery
- Meta-stability
- Dynamic Offset
- Gate Leakage
- Kick-back

DAC :
- kT/C noise
- Matching
- Gain Loss
- Parasitic

Switches :
- Slew Rate
- Settling
- Leakage
- Parasitic

SAR Logic :
- Delay
- Leakage
- Complexity

More Severe Design Challenges @ ULV Operation

T/H :
- Speed
- Distortion
- Charge Injection
- Clock Feedthrough
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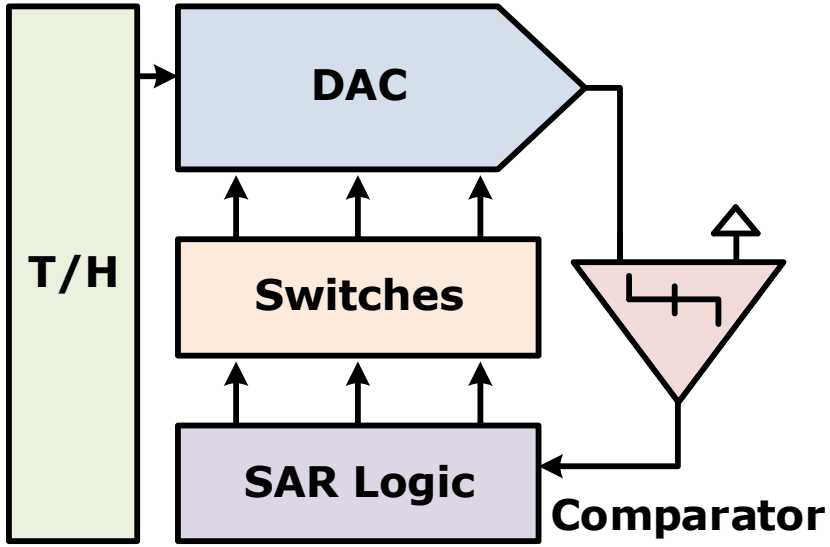
- Signal Coupling
- Jitter



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Switches :
- Slew Rate
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SAR Logic :
- Delay
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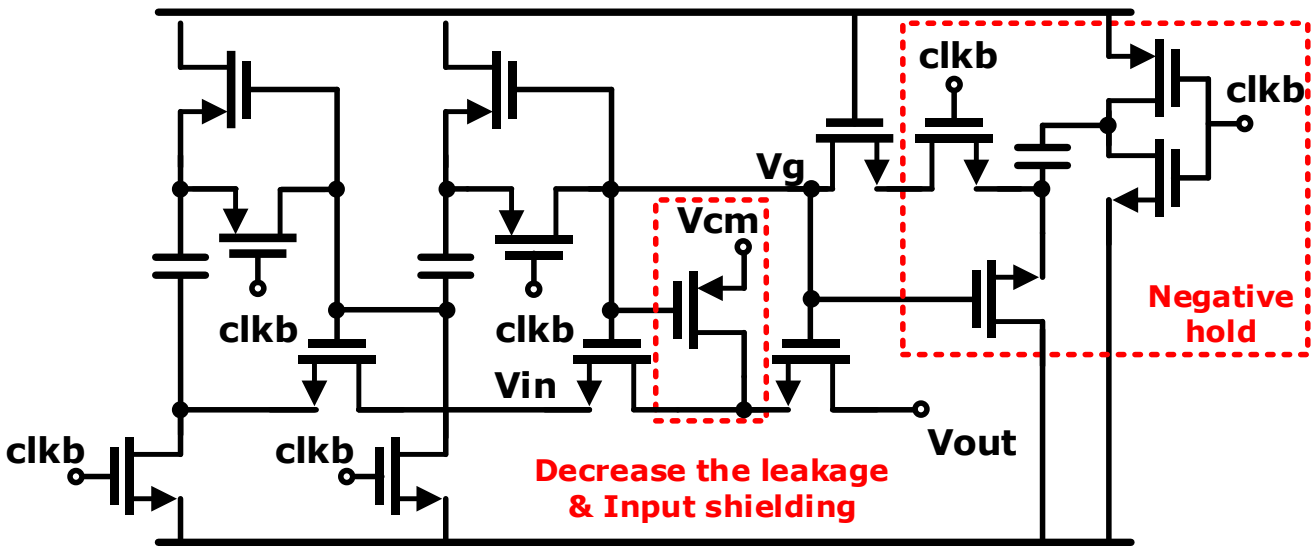
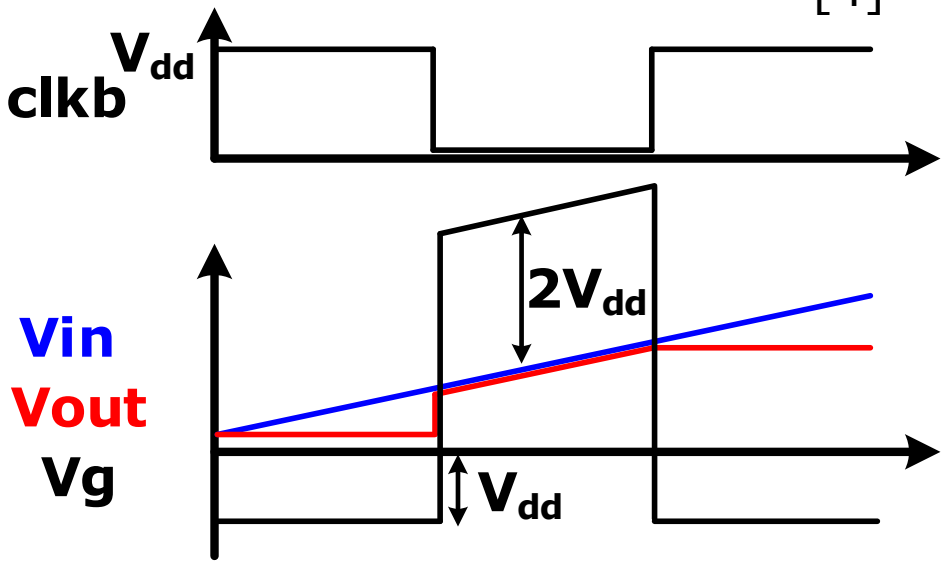
Design Challenges of ULV SAR ADC

- T/H
  - Degraded on/off switching performance
- DAC & Switches
  - Degraded settling speed & accuracy
  - Smaller LSB ➔ higher noise requirement ➔ larger C_{unit}
- Comparator
  - Degraded speed
  - Smaller LSB ➔ higher noise requirement
- SAR Logic
  - Larger delay & leakage

ULV Track & Hold (T/H)

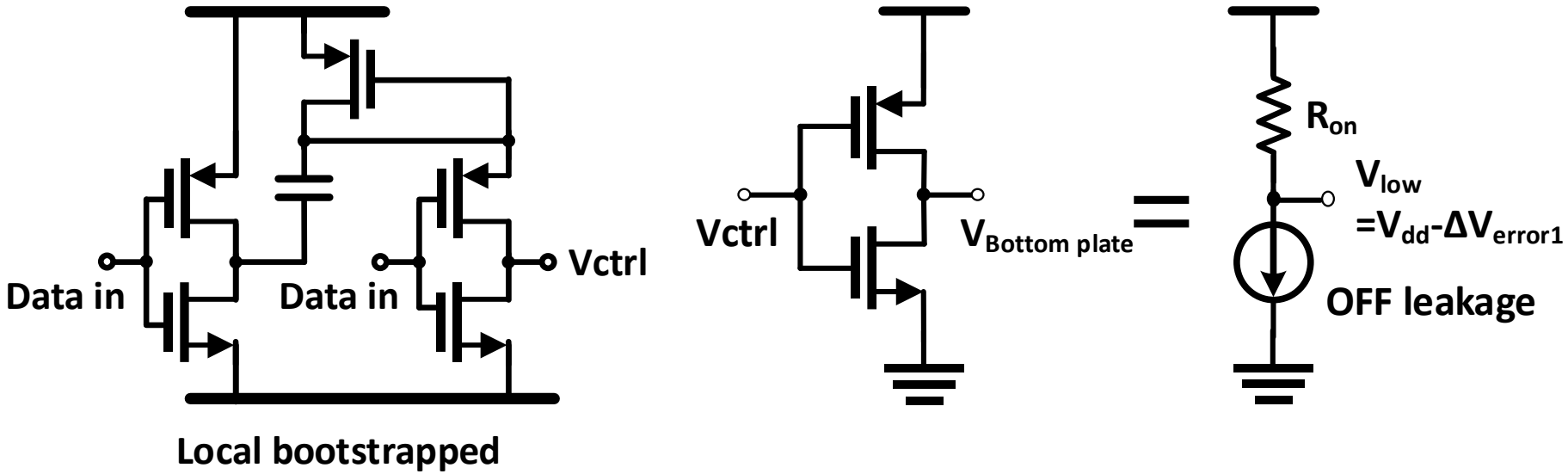
[4]





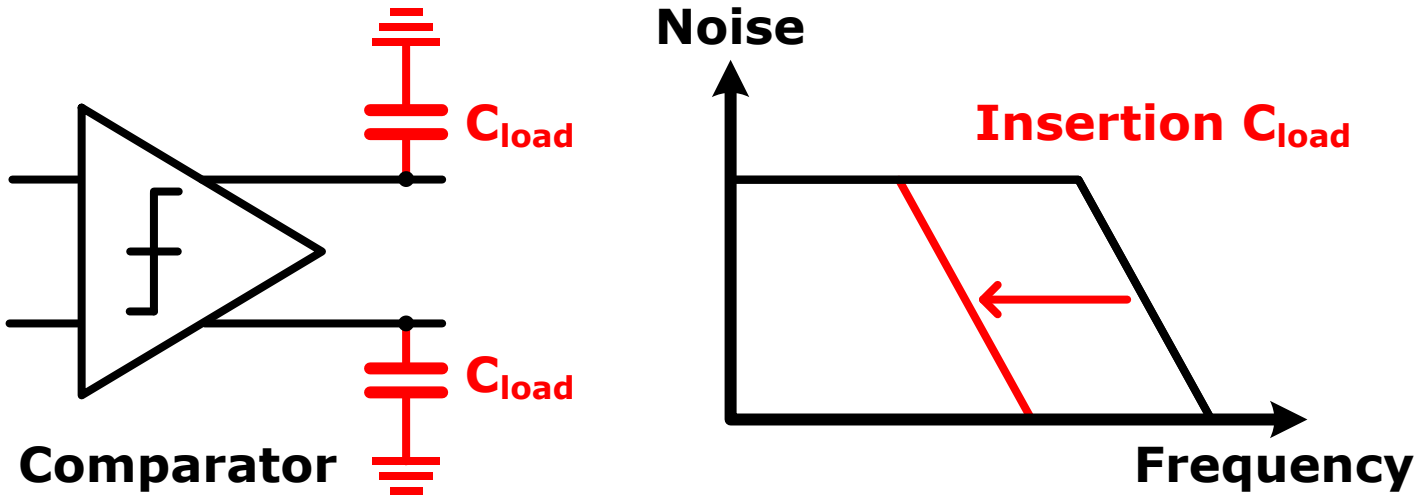
- Bootstrapped switch @ sampling
  - Constant overdrive voltage ➔ high linearity & sampling speed
  - Multiple bootstrap (V_{DD} < 1/2V_{core}) when necessary (reliability issue)
- Leakage control @ holding
  - Cascade sampling switch & input isolation
  - Negative hold

ULV DAC & Switches



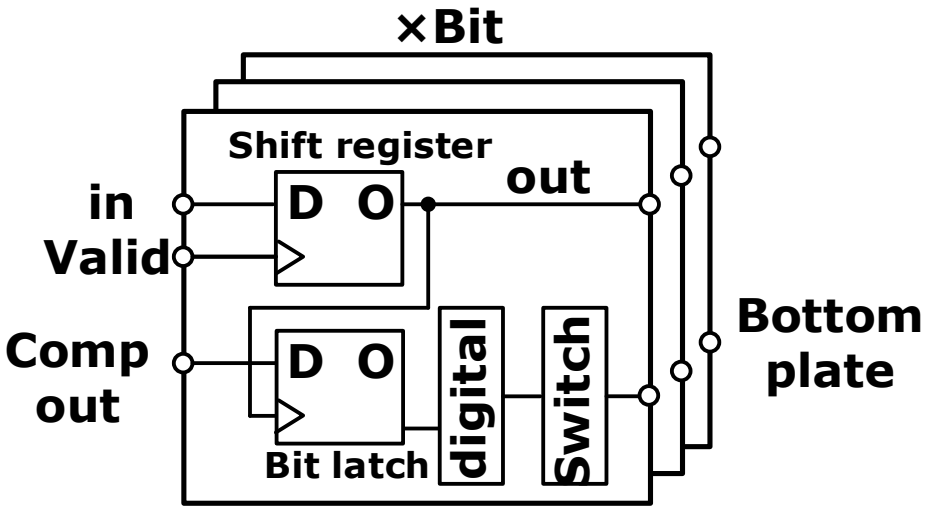
- Degraded on/off switching performance
  - Degraded settling speed & accuracy
  - Local bootstrapped switch
- Smaller LSB
  - Matching & kT/C noise requirement ➔ larger C_{total} (C_{unit})
  - Need efficient methodology for switching energy reduction

ULV Comparator



- Degraded speed
  - Larger biasing current (dynamic)
- Smaller LSB ➔ higher noise requirement
  - Adding C_{load} for noise bandwidth reduction
  - Noise $\propto \sqrt{C}$, SNR+6dB ➔ noise/2 ➔ C×4 ➔ P_{comp}×4
  - Need efficient designs to reduce comparator noise

ULV SAR Logic



- Larger delay & leakage
  - Moderate achievable operation frequency
- SAR logic mainly composed of registers
  - Need efficient implementation

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Low Power Design Techniques of SAR ADC

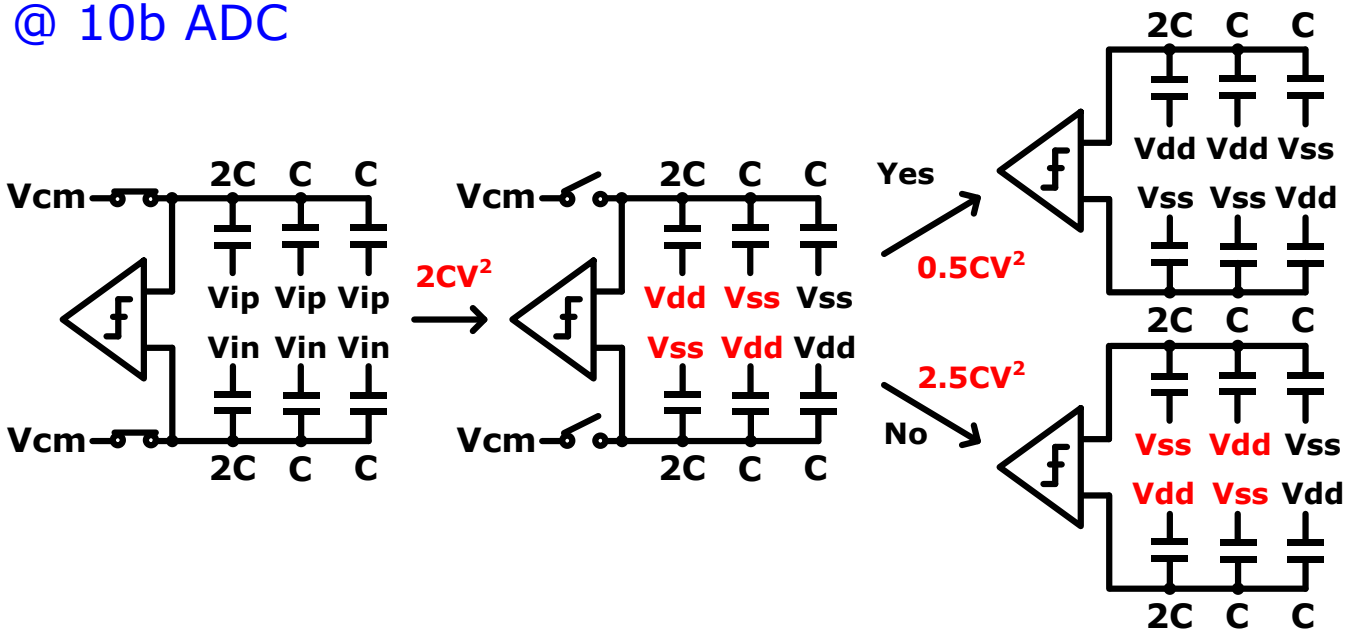
- Efficient DAC
  - DAC switching energy $E_{sw} \propto V_{ref} \times Q_{sw} = V_{ref} \times CV_{sw}$
  - Switching energy reduction
- Efficient Comparator
  - Noise $\propto P_{comp}^{0.5}$
  - Good tradeoff of power and noise
- Efficient SAR Logic
  - Dynamic power $\propto f_{sw}CV_{DD}^2$ (f_{sw}: switching activity frequency)
  - Logic simplification and optimal sizing

Efficient DAC Switching Techniques

- Avoid try-n-error / unnecessary capacitor switching
  - Monotonic switching
  - Aligned switching (subranging architecture)
  - Input range adaption
- Reduce bottom plate swing V_{sw} to $V_{FS}/2$ ($E_{sw} \propto V_{ref} \times CV_{sw}$)
  - Vcm-based switching
- Release extra reference (Vcm) requirement
  - Charge averaging switching
- Dual DAC with double input range ($V_{FS}=2V_{DD}$) ➔ bottom plate swing=$V_{FS}/2$
  - Semi-resting & INL splitting DAC switching

Conventional Switching

E_{sw} = 682.65 CV^2 @ 10b ADC

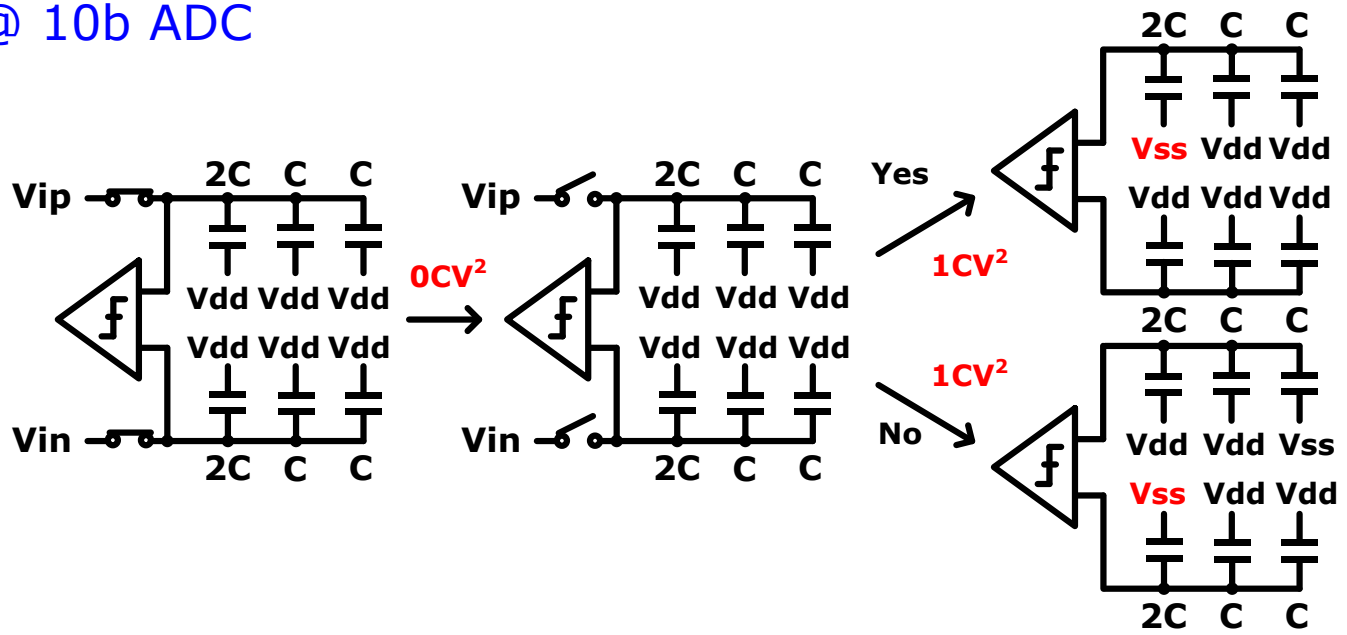


- Bottom plate sampling
  - Need DAC switching for MSB decision
  - Differential DAC switching ➔ fixed common-mode in conversion
  - 50% code need try-n-error switching operations ➔ energy waste ☹

Monotonic Switching

[5]

E_{sw} = 255.5 CV^2 @ 10b ADC

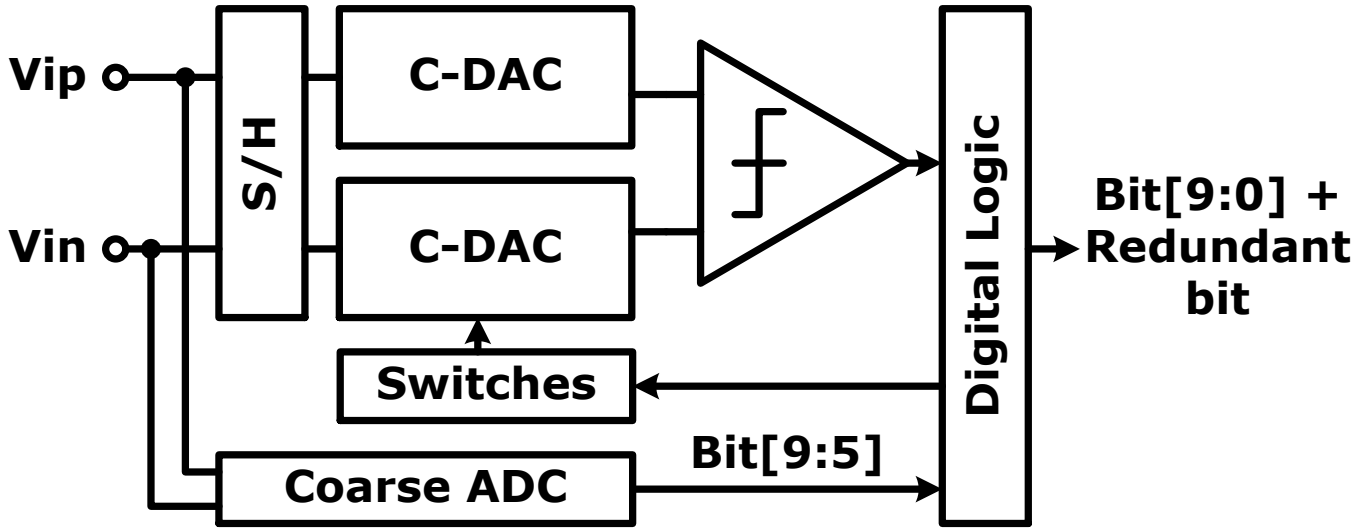


- Top-plate sampling with bottom-plate reset to Vdd
  - No energy waste for MSB decision ☺
  - Single capacitor switching for every bit conversion (no try-n-error) ☺
  - Common mode voltage shift ☹

Subranging Architecture + Aligned Switching

[6]

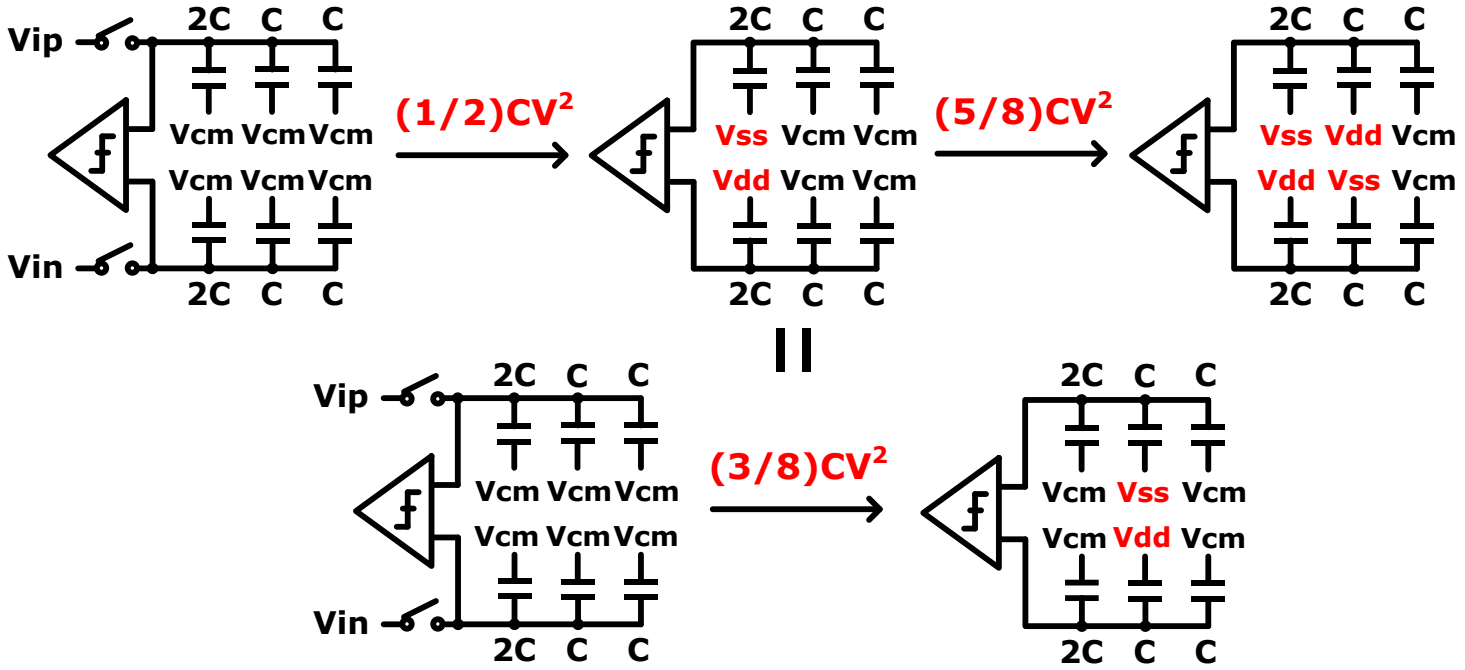
E_{sw} = 69.8 CV^2 (conversion) + 159.9 CV^2 (reset) @ 10b ADC



- Extra 5-bit coarse ADC + 10-bit main ADC
  - Aligned switching to avoid try-n-error energy waste ☺
  - Consume energy in reset phase ☹
  - Require complex two-step operation control & redundancy ☹

Aligned Switching (Detect-and-Skip)

[6]

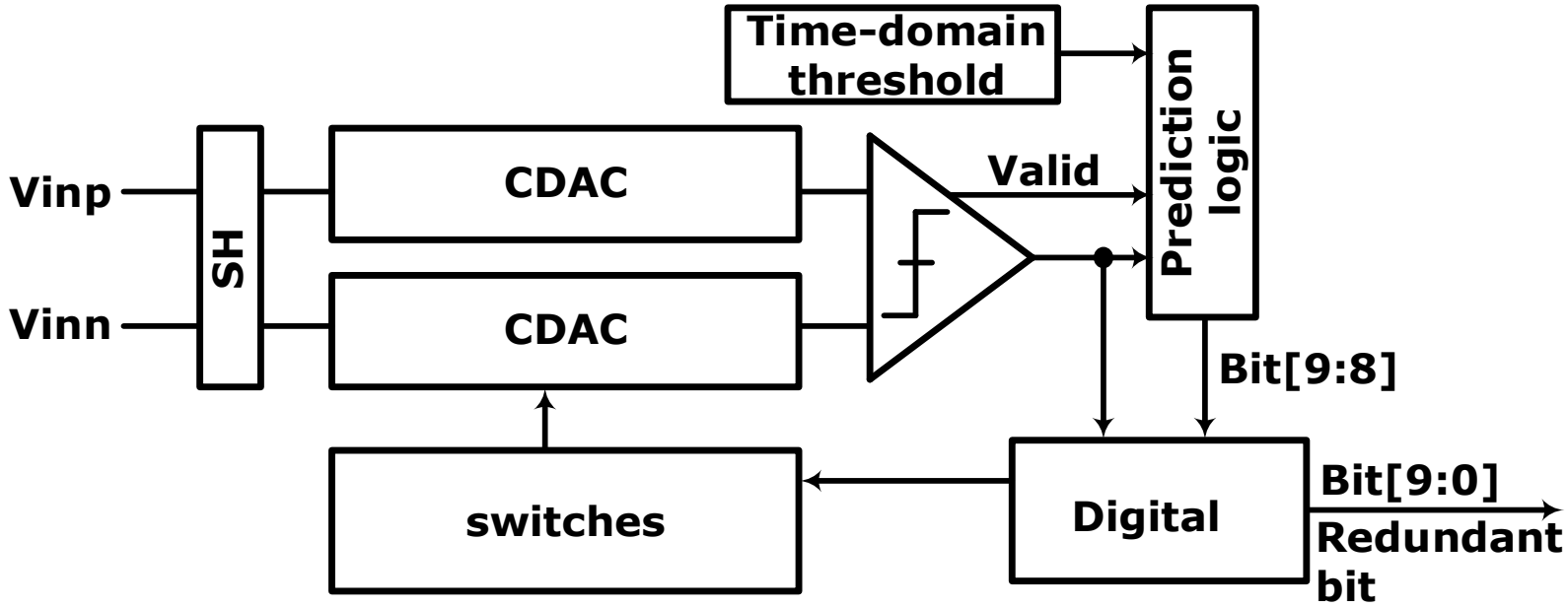


- Aligned switching skips the unnecessary switching and energy waste ☺
  - Need input level detection

Input Range Adaption (Detect-and-Skip)

[7]

E_{sw} = 106.2 CV^2 + 20.5 CV^2 (redundancy) @ 10b ADC

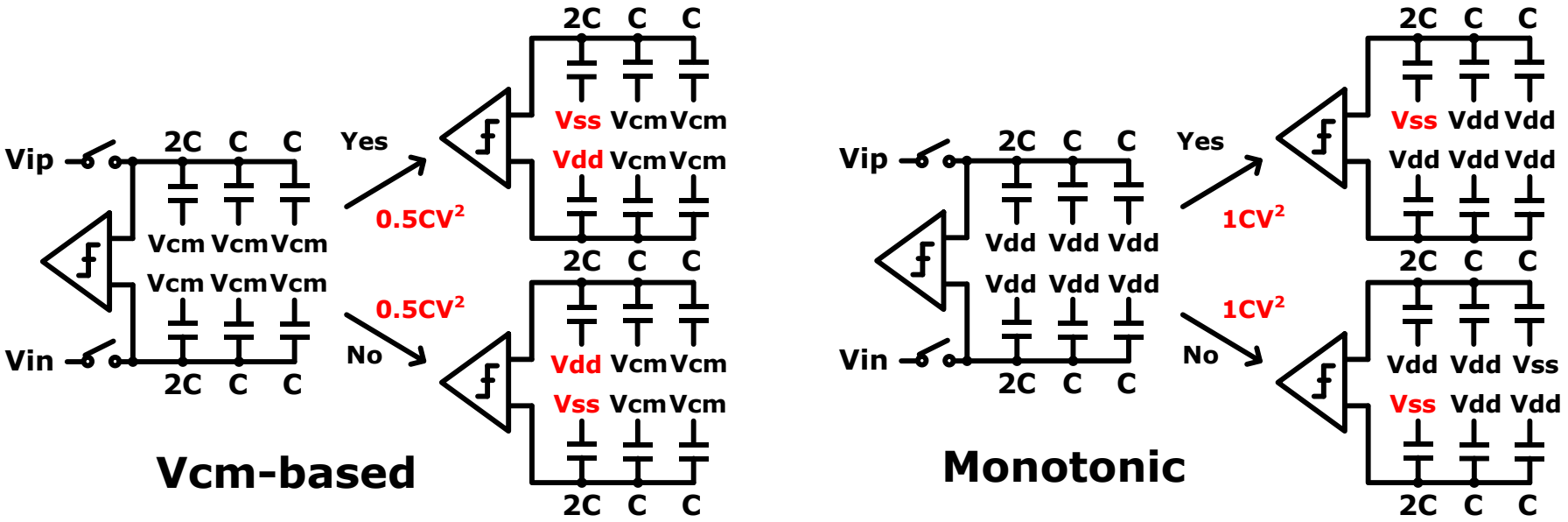


- Use comparison time to define MSB and MSB-1
  - Reduce the most energy consuming switching ☺
  - No extra coarse ADC (DAC & comparator) ☺
  - Require time-domain foreground calibration & redundancy ☹

Vcm-Based Switching

[8]

E_{sw} = 170.2 CV^2 @ 10b ADC

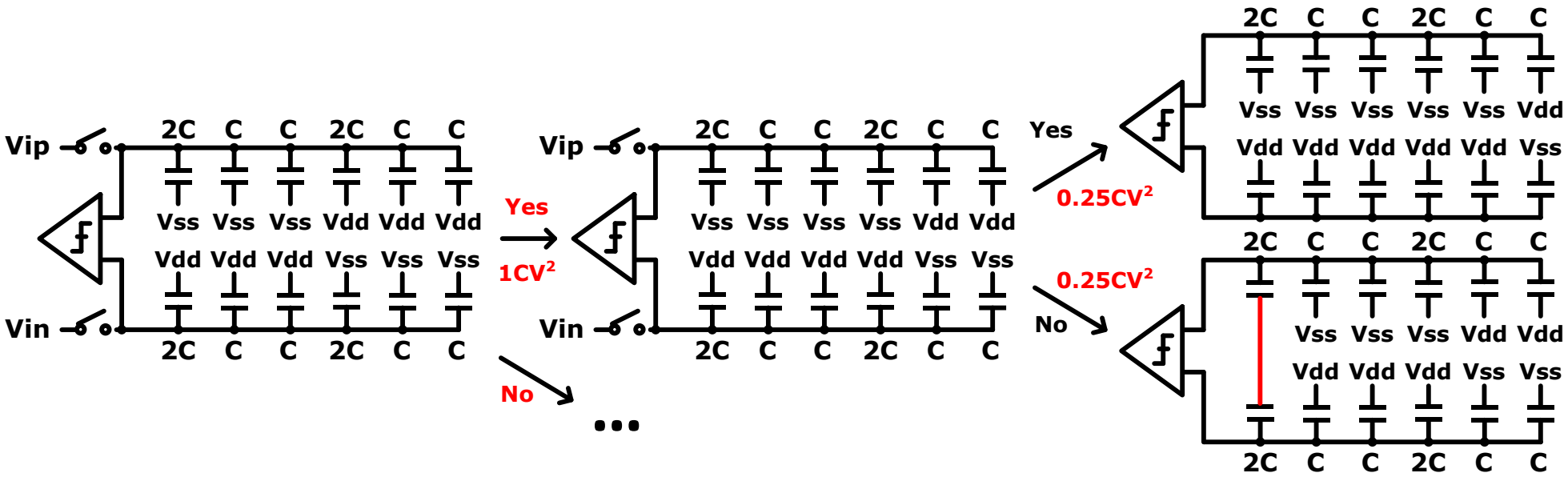


- Reset bottom plate to Vcm instead of Vdd
  - Reduced bottom plate voltage swing $V_{SW} = V_{FS}/2$ ☺
  - No common-mode voltage shift ☺
  - Additional Vcm supply is required ☹

Charge-Averaging Switching

[9]

E_{sw} = 88.6 CV^2 (conversion) + 255.5 CV^2 (reset) @ 10b ADC

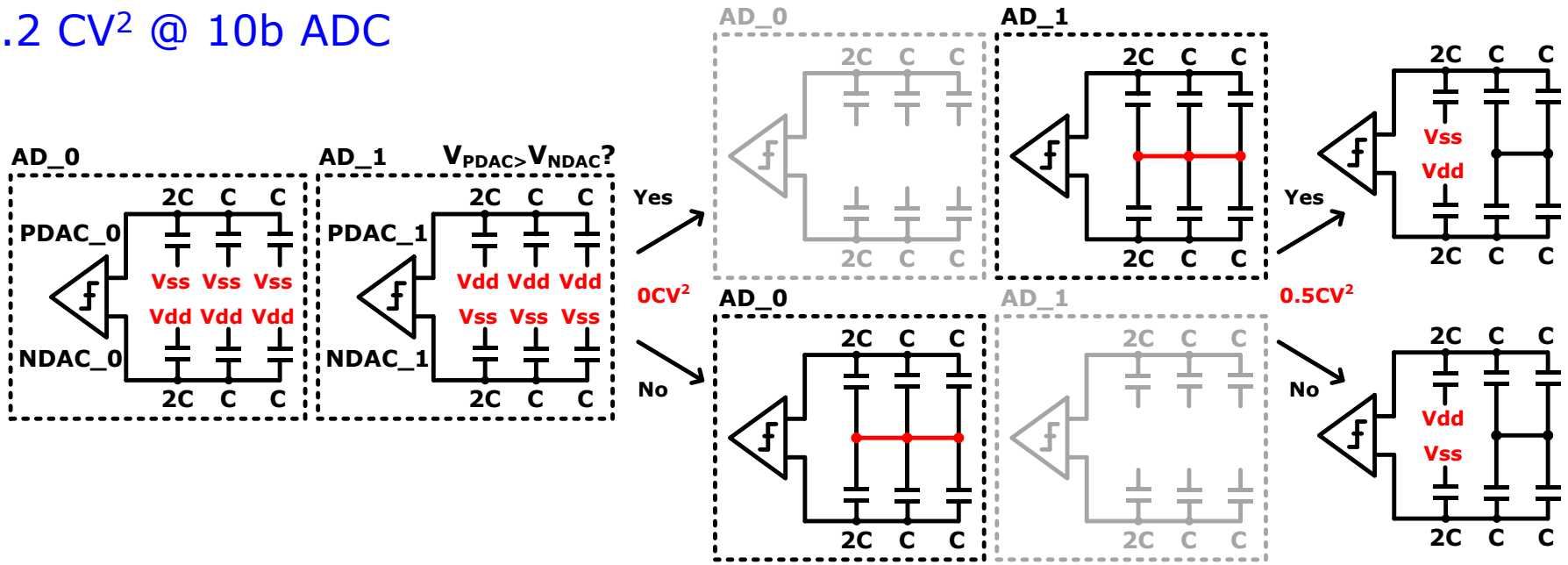


- Use charge averaging operation to create Vcm level
  - No additional Vcm supply ☺
  - Reduced switching energy in conversion phase ☺
  - Consume energy in reset phase ☹

Semi-Resting Switching

[10]

E_{sw} = 46.2 CV^2 @ 10b ADC

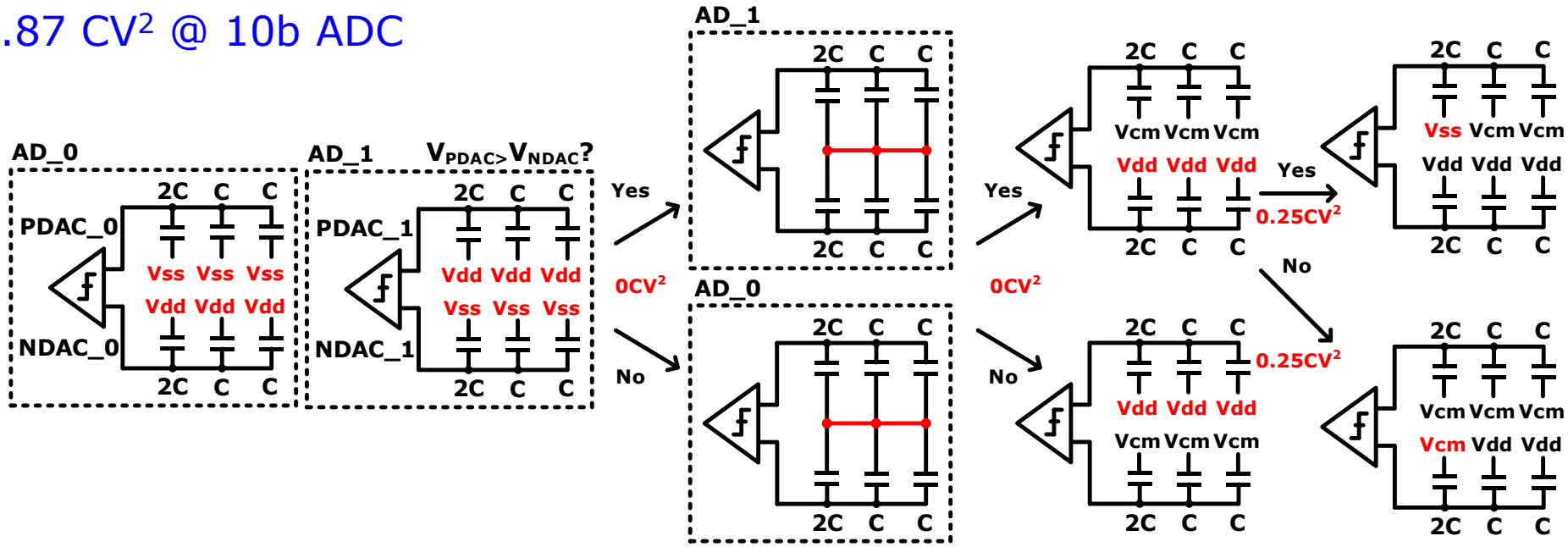


- Dual DAC with double input range ($V_{FS} = 2V_{dd}$)
  - Bottom plate voltage swing = $V_{FS}/2$ without Vcm supply ☺
  - No reset power ☺
  - Double V_{LSB} to release noise requirement ☺
  - Foreground calibration is needed ☹

INL-Splitting Switching

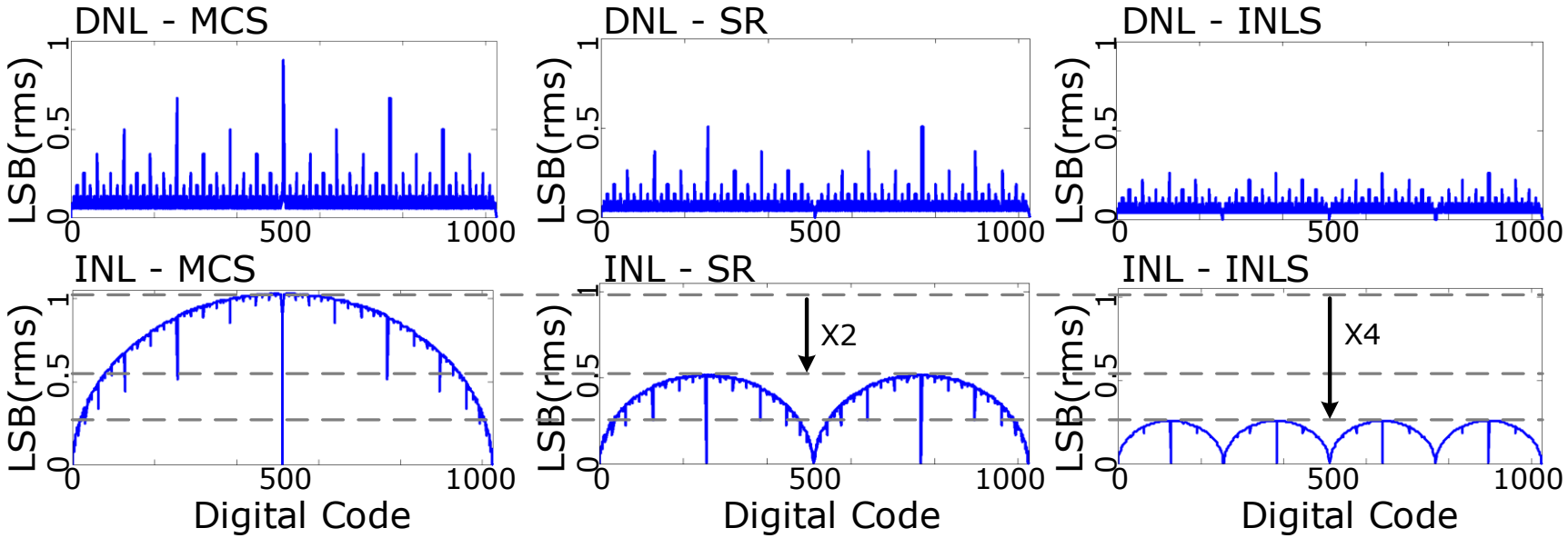
paper 14.6 [11]

E_{sw} = 15.87 CV^2 @ 10b ADC



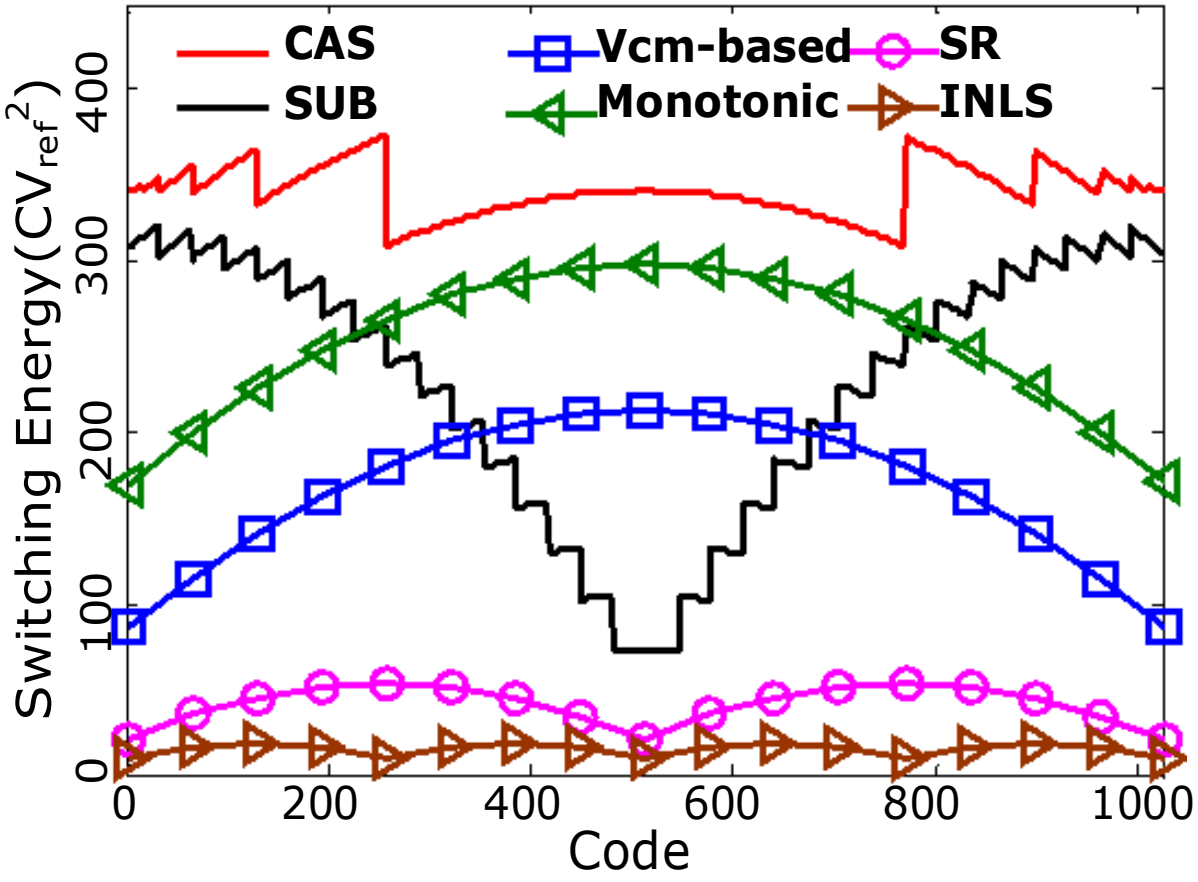
- Level shift operation
  - No switching energy for MSB to MSB-2 comparisons ☺
  - Enhanced DNL/INL performance by x4 ☺
  - On-chip voltage divider for Vcm with redundancy
  - Foreground calibration is needed ☹

Input Driver Power Requirement of SR & INLS



- Dual DAC of SR & INLS requires input driver power x2 @ sampling ?
  - Yes, if the design is kT/C noise dominated!
  - No, if it is DAC matching dominated! (This is our case due to the double LSB)
- INL performances of SR & INLS improve by x2 & x4
  - C_{DAC} of SR & INLS can be smaller x4 & x16
  - Input driver power can be reduced by 2 in SR and by 8 in INLS

Switching Energy Comparison



Architecture	Switching Energy(CV^2)*	
	w/o reset	w/i reset
Conventional	682.65 CV^2	682.65 CV^2
Monotonic	255.5 CV^2	255.5 CV^2
Sub-Ranging	69.8 CV^2	229.7 CV^2
IRA	126.7 CV^2	126.7 CV^2
Vcm-based	170.2 CV^2	170.2 CV^2
CAS	88.6 CV^2	344 CV^2
SR	46.2 CV^2	46.2 CV^2
INLS	15.87 CV^2	15.87 CV^2

*Normalized to the same V_{FS} & C_{total}

- DAC switching energy decreases dramatically with efficient methodologies

Efficient Comparator Techniques

- Only critical decisions in SAR conversion require low-noise comparator
- Enable high-power low-noise comparison only when needed
  - Majority voting ➔ requires critical decision detection
  - Two-step architecture ➔ coarse-fine mismatch
  - Adaptive time-domain comparator ➔ needs optimized time-domain threshold
- Efficient high-performance comparator
  - Bidirectional comparator
  - Cascade input comparator

Majority Voting

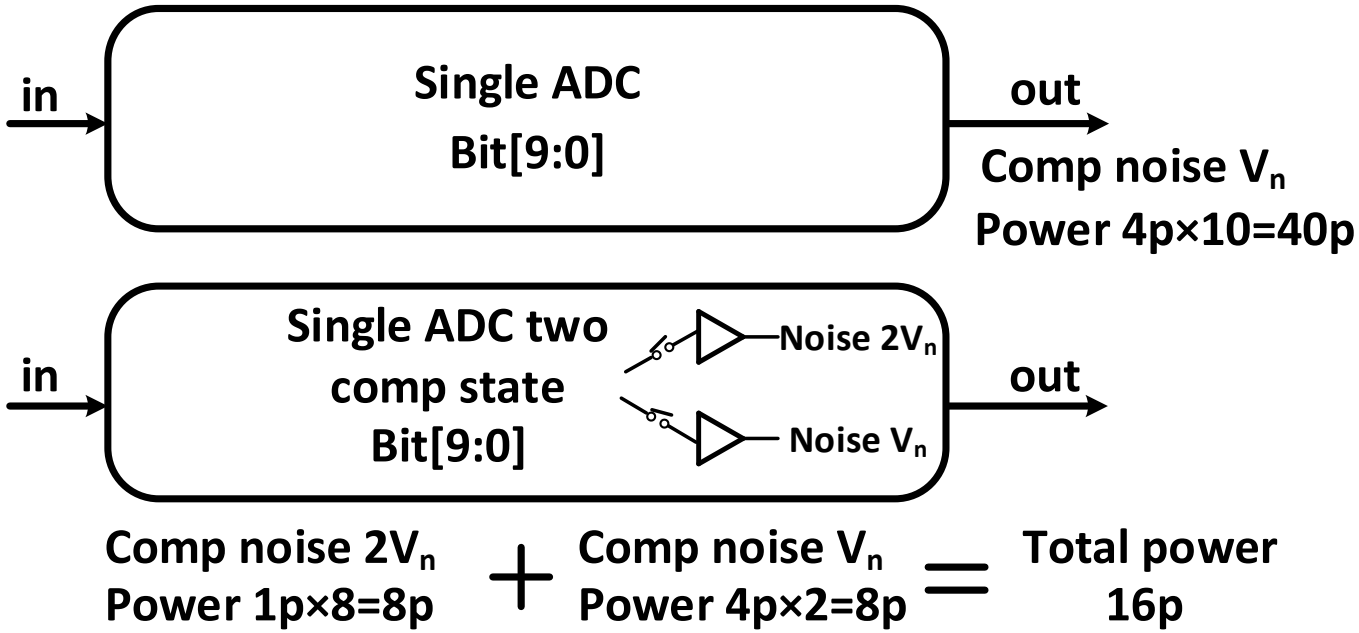
[12]

Assumption:

$P_{comp}=4p@n_{comp}=1V_n$

$P_{comp}=1p@n_{comp}=2V_n$

p: unit power



- Use multiple votes to suppress the noise
  - Only enabling multiple comparison (high power) at critical decision ☺
  - Reduces comparator power by ~60% ☺
  - Critical decision detection & voting circuit penalty: uncertainty, power, speed ☹

Two-Step Architecture

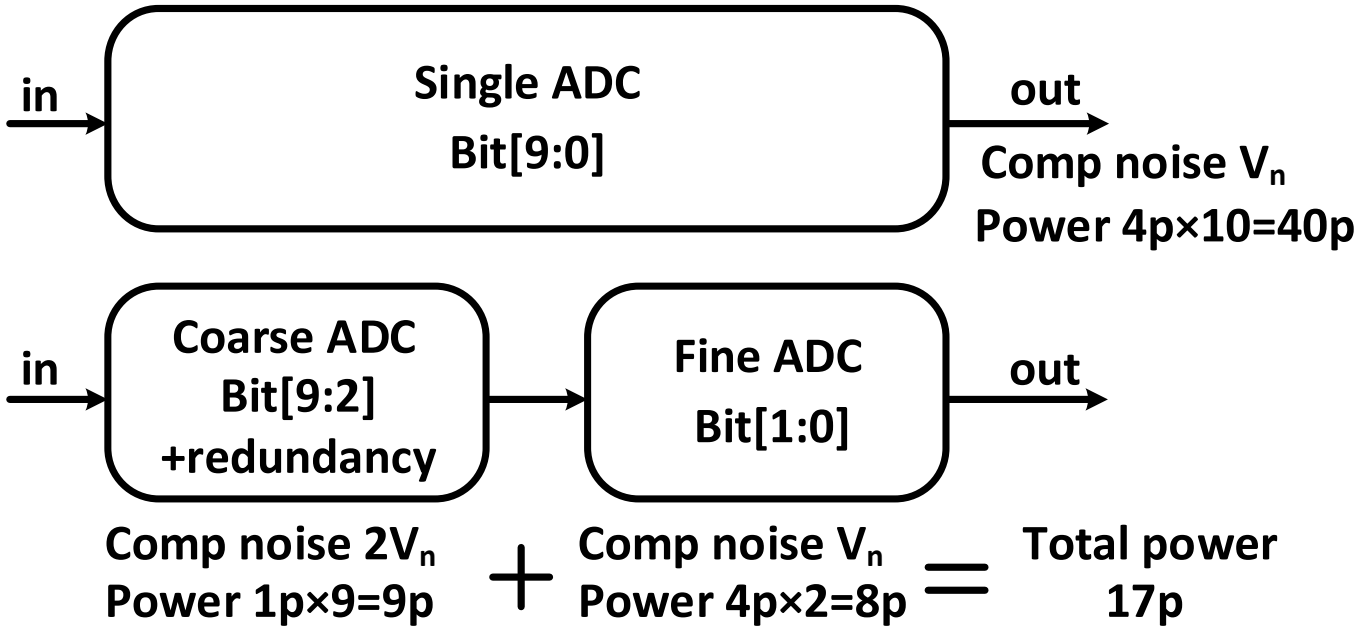
[13]

Assumption:

$P_{comp}=4p@n_{comp}=1V_n$

$P_{comp}=1p@n_{comp}=2V_n$

p: unit power

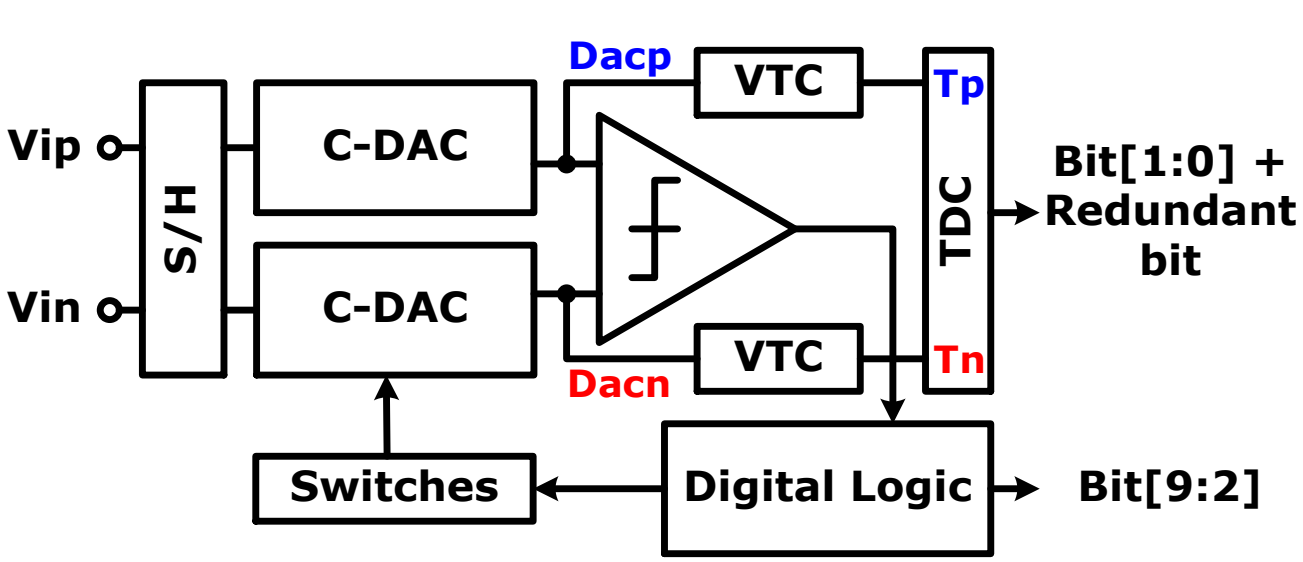


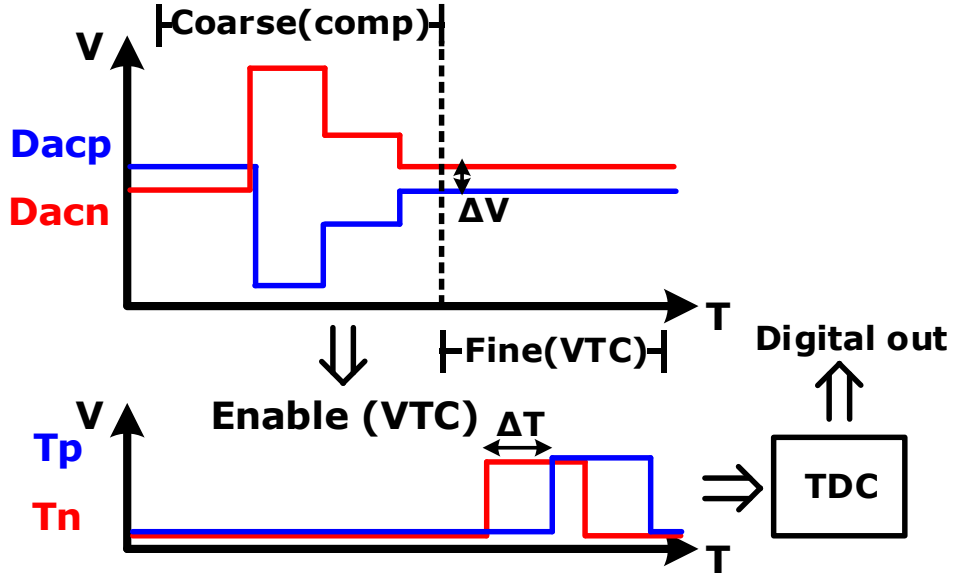
- Combination of high-noise coarse and low-noise fine ADCs
  - No critical decision detection circuit ☺
  - Reduces comparator power by ~60% ☺
  - Requires redundancy and calibration ☹

Two-Step + Time Domain Fine ADC

[14]

*Voltage to time converter (VTC)

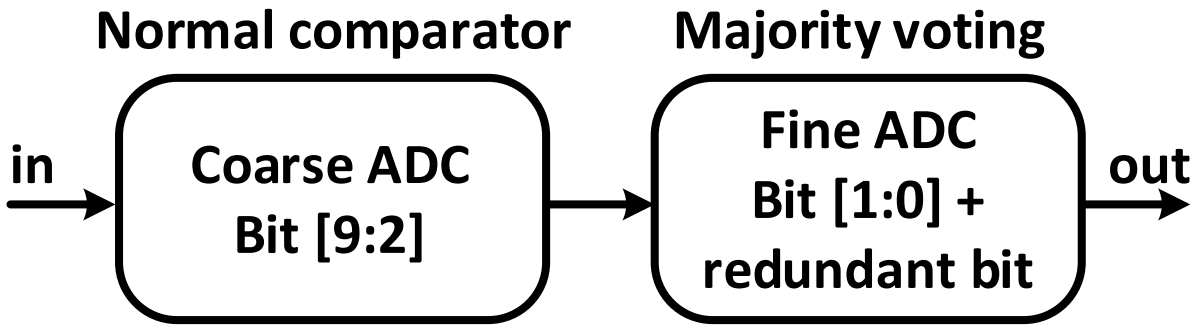




- Coarse SAR ADC (8bits) + fine TDC (2bits)
  - Small DAC area and routing parasitic ☺
  - Potential for efficient high-resolution time-domain fine ADC ☺
  - TDC penalty: power and calibration ☹

Two-Step + Majority Voting Architecture

[15]

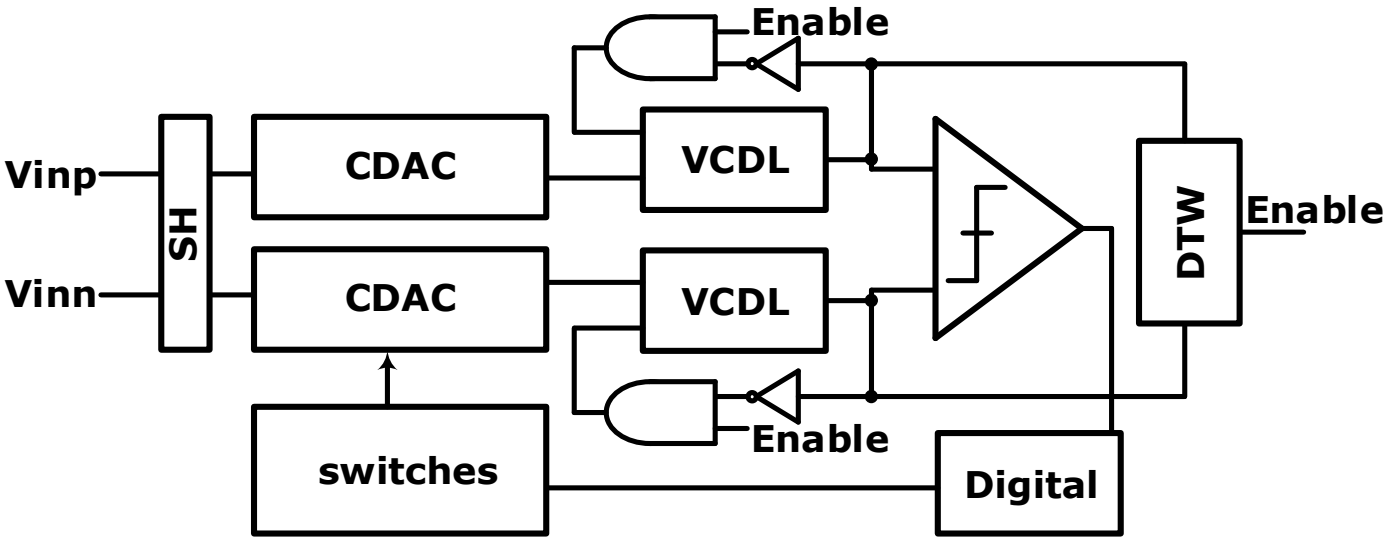


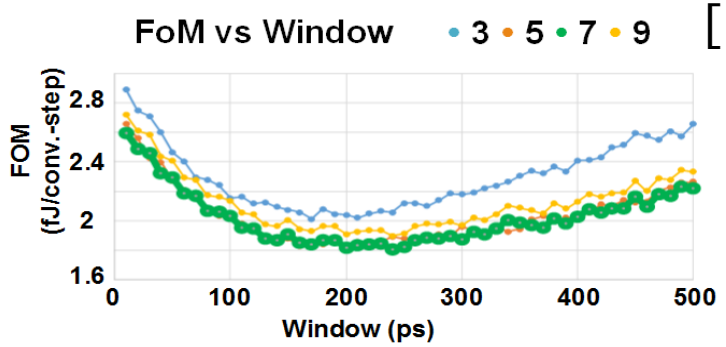
Method	Noise Requirement	Average Comparison Times	Normalized Energy
0-vote 0C-rd	0.52LSB	12	1
0-vote 1C-rd	0.56LSB	13	0.93
5-vote 1C-rd	0.95LSB	19	0.47
9-vote 1C-rd	1.11LSB	25	0.46

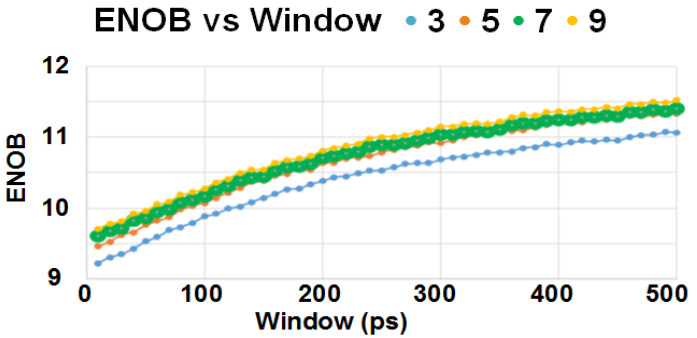
- Normal comparison coarse ADC (8 bits) + Majority voting fine ADC (2 bits)
  - Single comparator without calibration requirement ☺
  - No critical decision detection ☺
  - More comparison times ☹

Adaptive Time-Domain Comparator

[16]







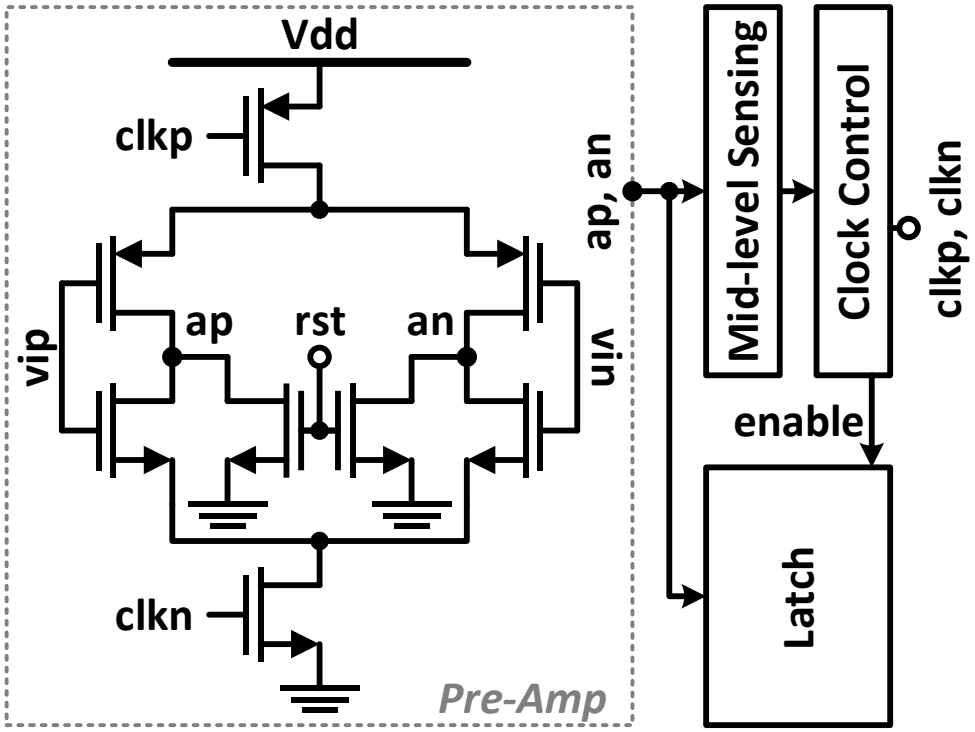
- Oscillation-based V-to-T converter + PD with programming threshold
  - Use oscillation cycles to increase VTC gain ➔ reduce input-referred noise
  - Differential threshold window (DTW) to define critical decision
  - Adaptive comparison with optimized power-noise tradeoff ☺
  - Need to find the optimized DTW for FoM performance ☹

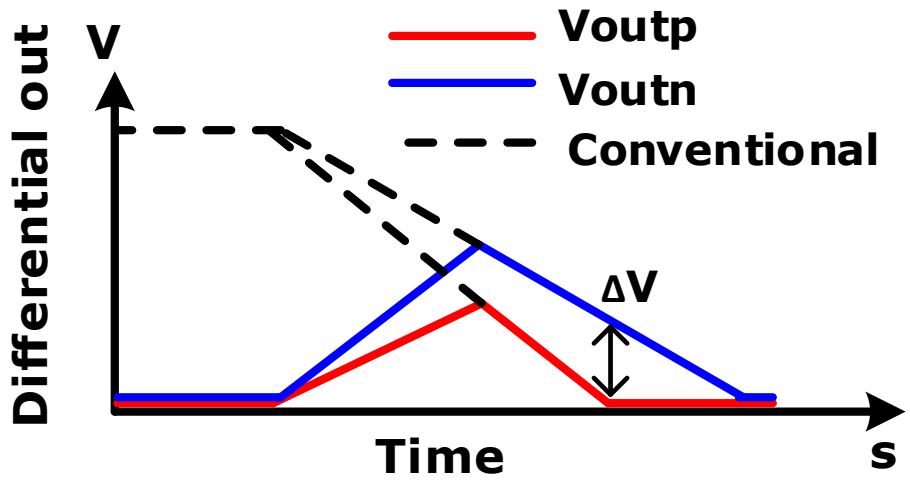
Efficient High-Performance Comparator

- Efficient low-noise pre-amplifier design (no adding C_{load})
  - Bi-directional comparator ➔ less energy waste of preamp
  - Cascade input comparator ➔ larger gain of preamp

Bi-directional Comparator

[17]

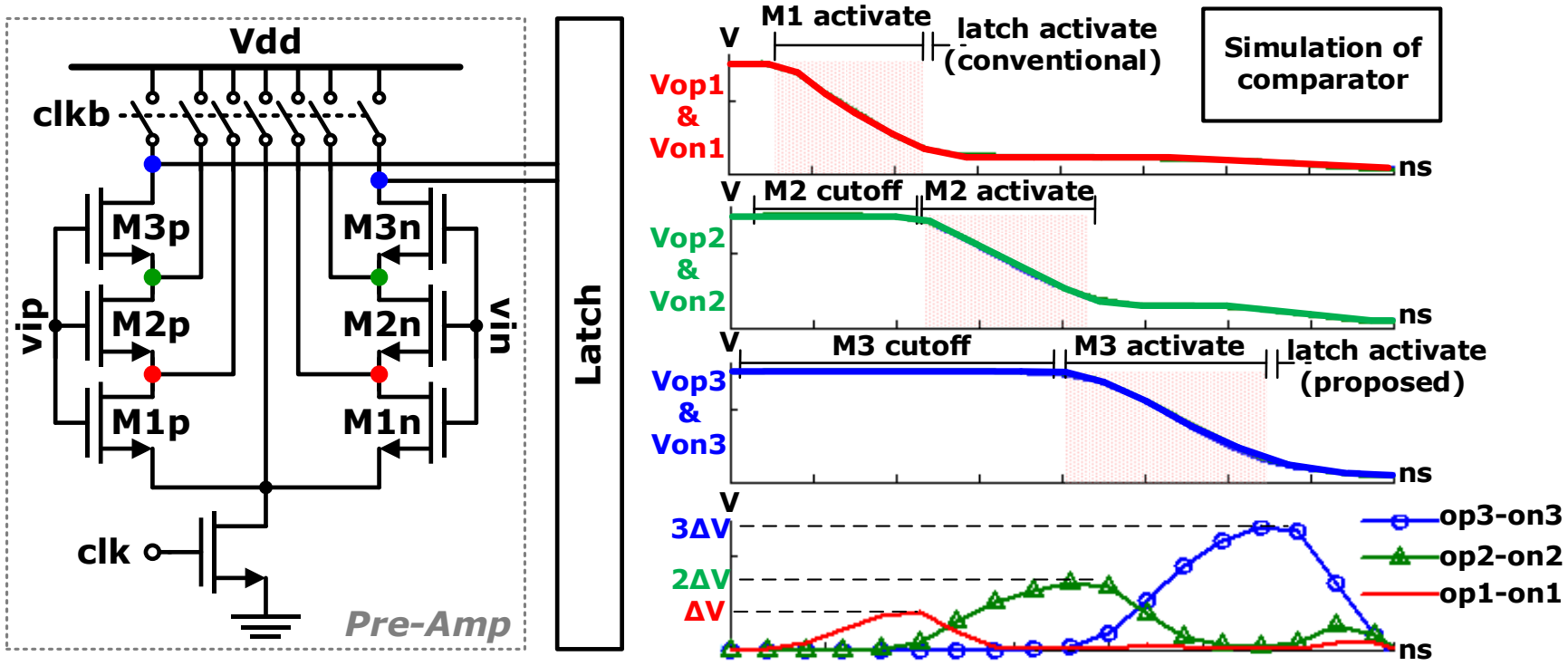




- Bi-directional output amplification with middle level detection
  - Consumes $0.5CV^2$ energy per comparison (compared to CV^2) ☺
  - Middle level sensing and clock control are required ☹

Cascade Input Comparator

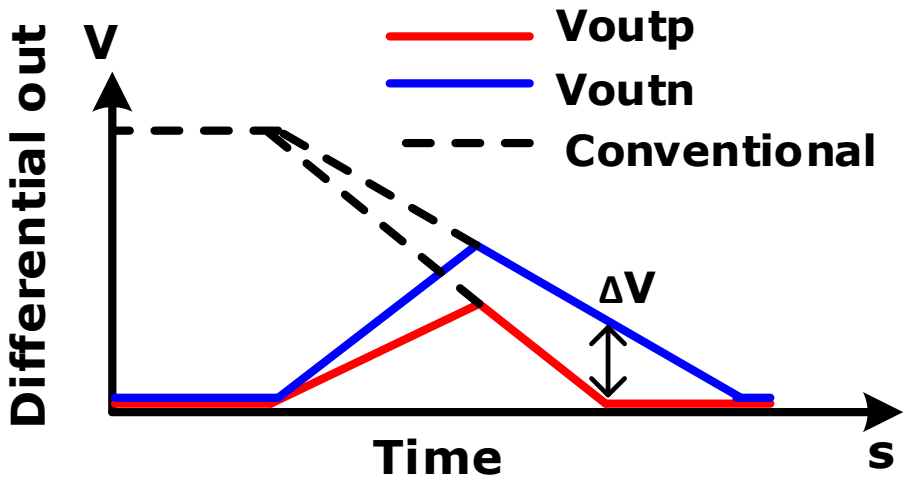
[10]



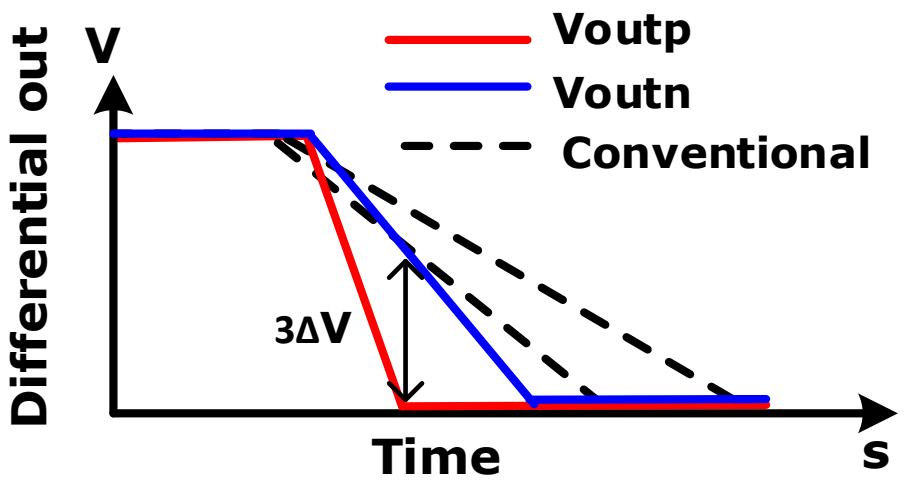
- Turn-on cascaded input devices sequentially to boost preamp gain 3x
  - No extra power consumption ☺
  - Reduces input referred noise by √2 ☺ (extra noise from added devices)
  - Increased signal-dependent input capacitance ☹

Efficiency Comparison

Bi-directional Preamp

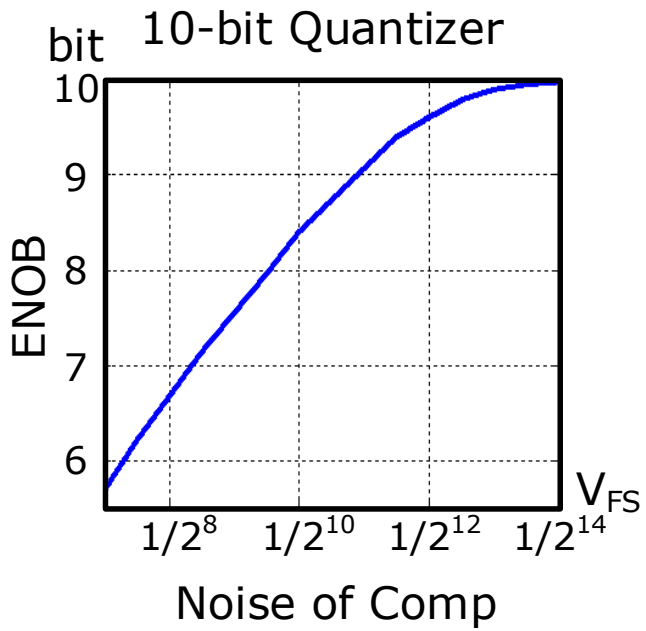


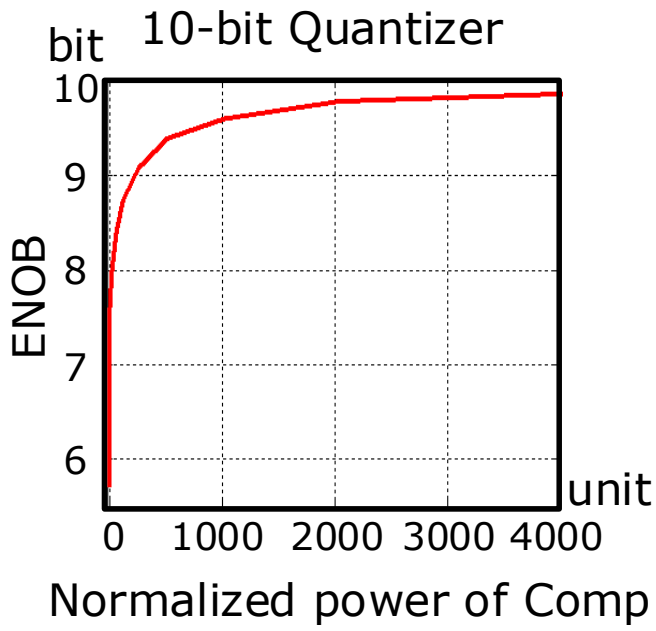
Cascade Input Preamp

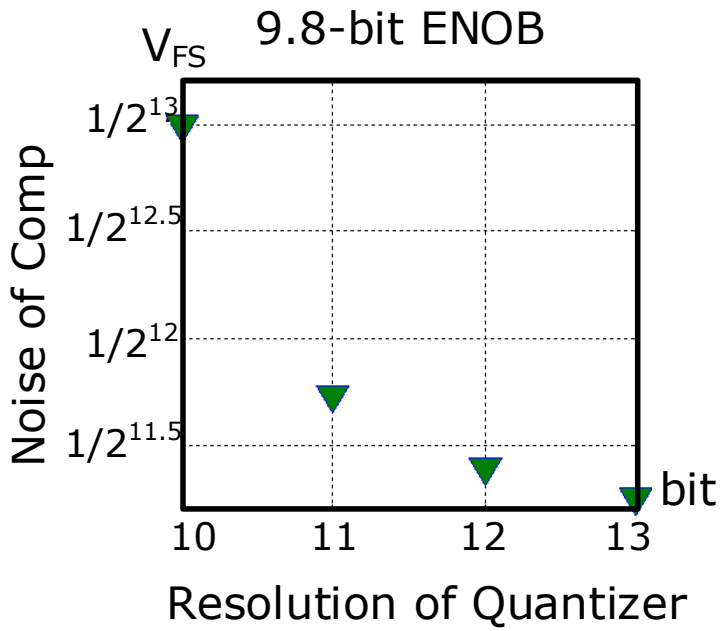


- Save 50% power compared to the conventional pre-amplifier
  - Bidirectional: same loading capacitance with smaller energy consumption
  - Cascade-input: smaller loading capacitance with higher preamp gain (3x gain, 1.5x faster)

Efficient Comparator Noise Spec Choice



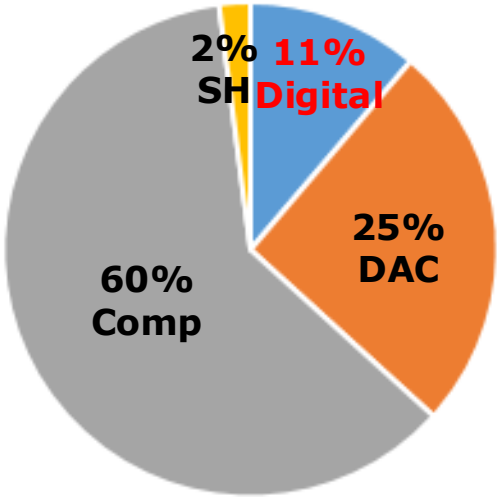




- For 10-bit ADC design
  - To achieve ENOB > 9, the comparator power increases dramatically
  - To implement a comparator with a noise spec < 0.5 LSB is not efficient, due to the quantization noise
- **Tip: choose the quantizer resolution 1 bit higher than the desired ENOB**

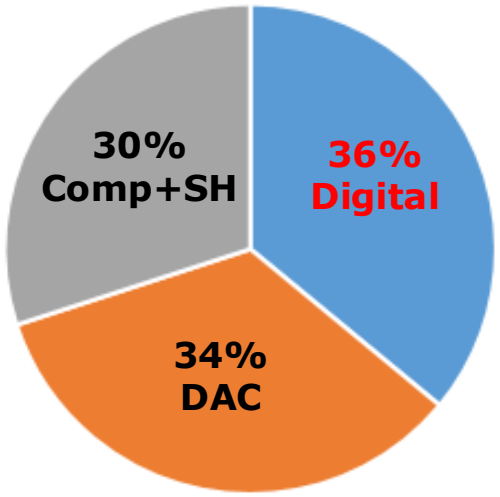
Power Distribution Trend of SAR ADC

2013 ISSCC



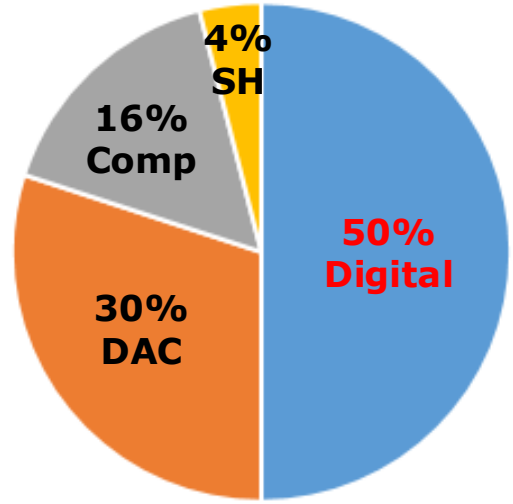
Majority voting[13]

2014 ISSCC



Aligned switching[6]

2015 VLSI



Semi-resting[11]

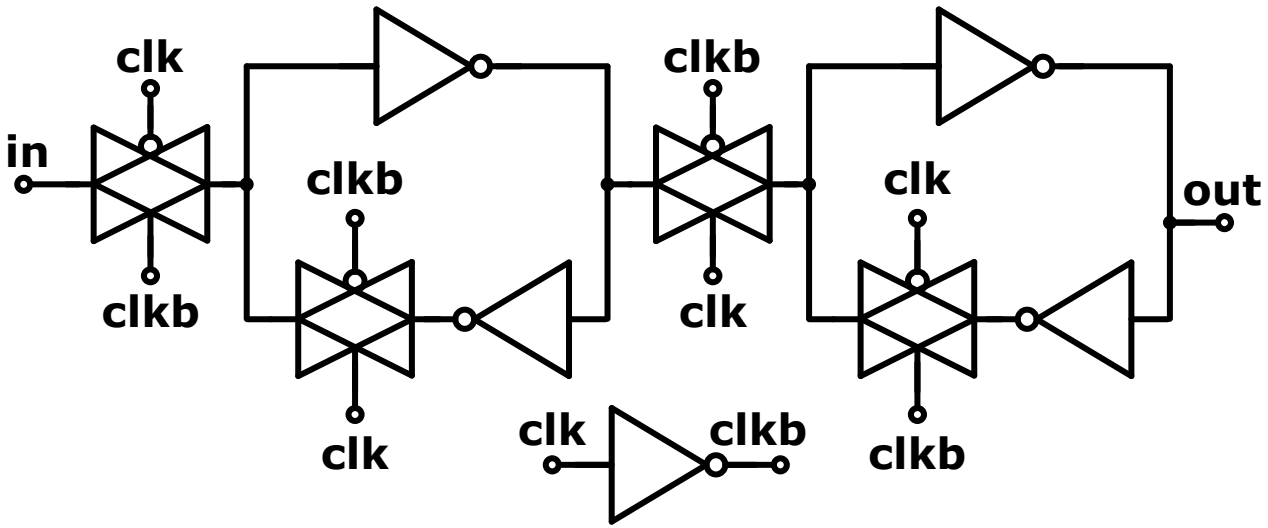
- Efficient DAC & comparator designs decrease the analog power contribution
  - Digital power consumption >50% of total power
  - Efficient SAR logic implementation becomes important
  - Need to deal with the delay and leakage issues in ULV operation

Efficient SAR Logic Implementation

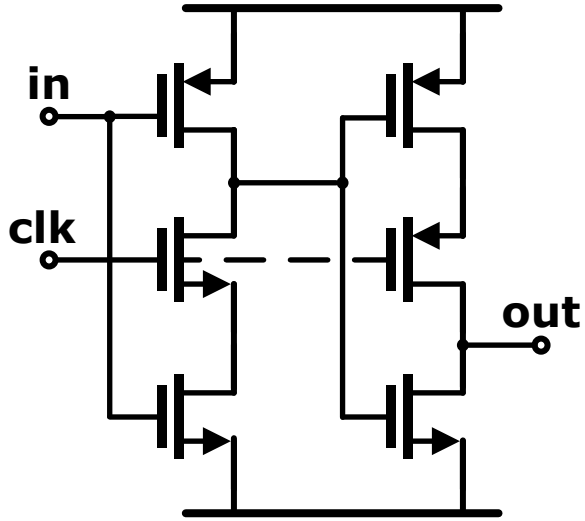
- Low power SAR logic
  - ULV operation
  - Simplified register implementation
  - Optimal gate sizing
  - Leakage control

Simplified Register Implementation

Conventional DFF



Dynamic SR



- Conventional vs. dynamic shift register
  - 18 transistors vs. 6 transistors
  - Multiple transition vs. single transition per conversion
  - Leakage issue of dynamic logic (low speed limitation)

Optimal Gate Sizing

- Smaller device ➔ less parasitic capacitance ≠ lower power consumption
  - Routing dominates the overall parasitic capacitance

- Rule of thumb ➔ size of MOS ↑
  - $C_{total} = C_{routing} + C_{MOS}$ almost keeps the same
  - $P = CV^2$ almost keeps the same
  - Speed ↑ ☺
  - Mismatch ↓ ☺
  - Noise margin ↑ ☺
  - PVT robustness ↑ ☺
  - Gate leakage ↑ ☹

- **Tip: use large logic gate for better performance with acceptable leakage**

Outline

- nW SAR ADC Applications
- Optimal Supply Voltage and Design Challenges
- Power Reduction Design of SAR ADC
- Conclusions

Conclusions

- Ultra-low voltage (ULV) operation is optimal for low-power SoC
- SAR ADC is the best candidate for low-voltage, low-power, medium-speed, moderate-resolution applications
- Design techniques including DAC switching methodologies, efficient comparison, and simplified logic are essential to achieve nW ULV SAR ADCs
- For high-speed high-resolution applications, ULV SAR ADC techniques can be adopted to the hybrid architectures to improve overall power efficiency

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