CHAPTER 9

Successive Approximation ADC

Outline

1. Basic Operation Principle of SAR ADC
2. Block Introduction (S/H, DAC, Comparator, SAR)
3. DAC Switching Energy Calculation
4. DAC Switching Method
5. Comparator Requirement (Matching)
6. SAR Logic Implementation

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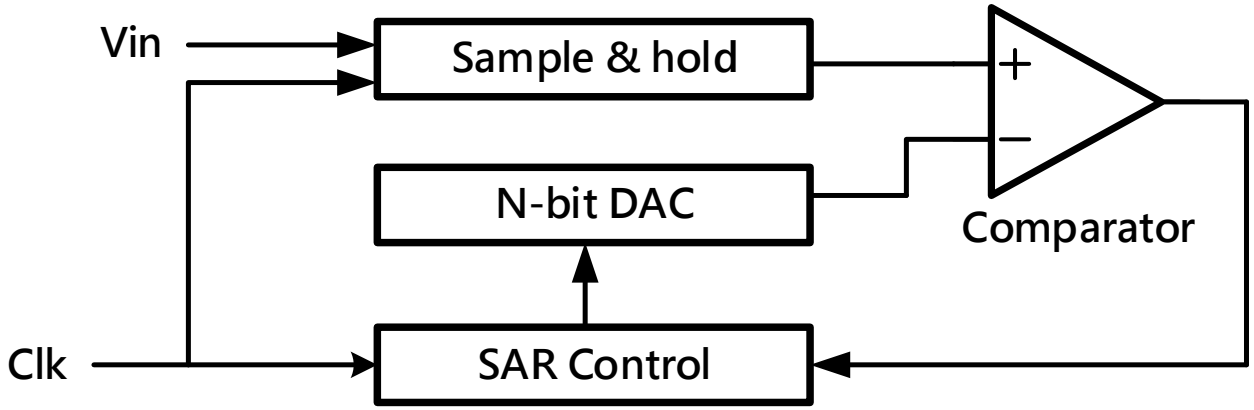
SAR ADC

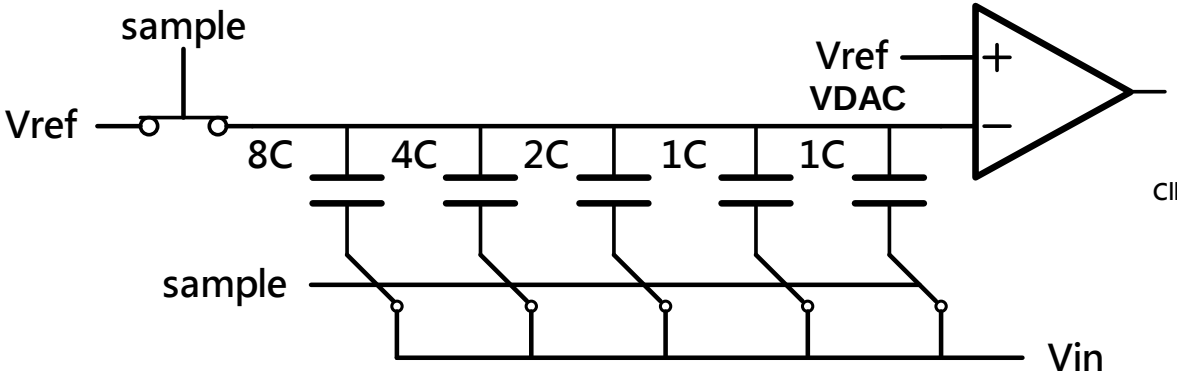


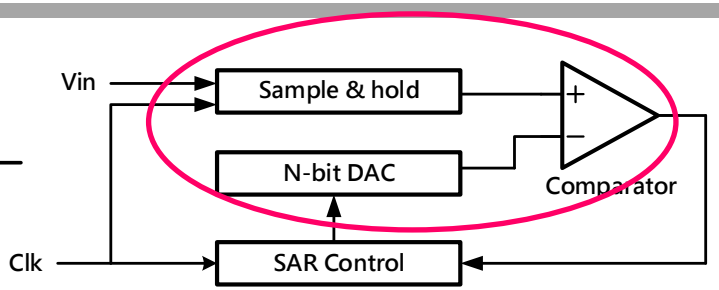
- SAR ADC is composed of sample & hold, DAC, comparator and SAR control logic
- Conversion procedure
  - Sampling phase

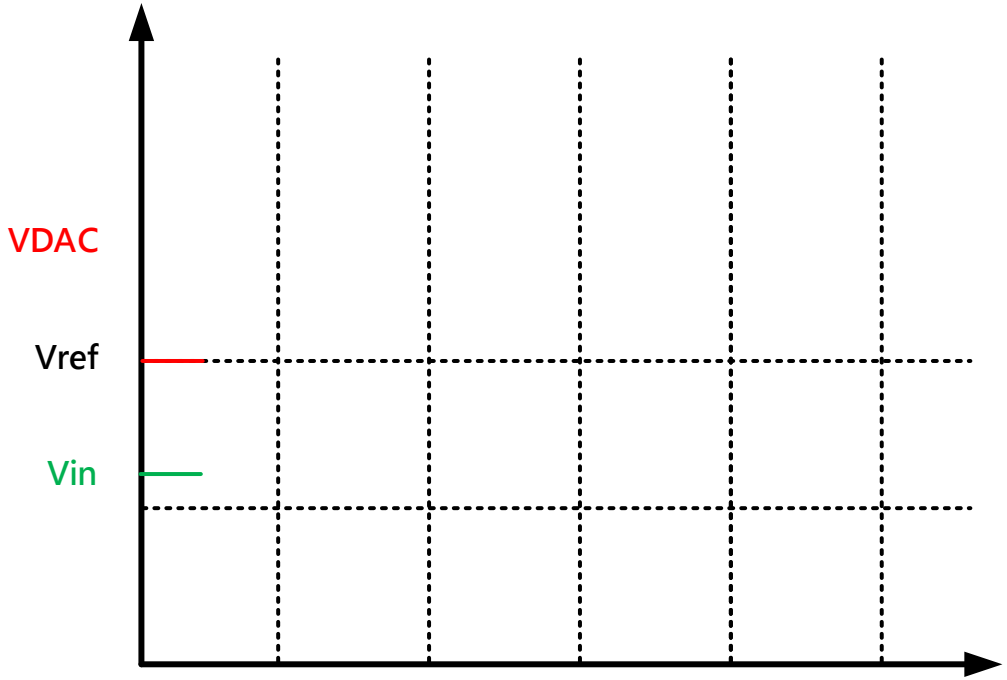
    S&H sample the input and reset DAC to initial value
  - Conversion phase

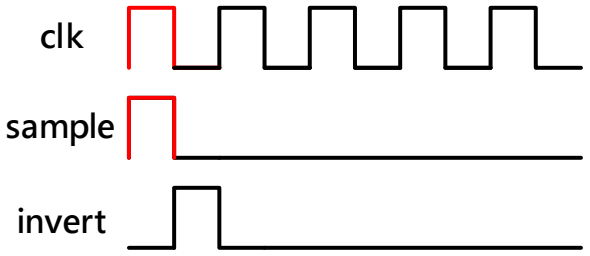
    Comparator compare the input signal and DAC output, then control the SAR logic to perform the binary search from MSB to LSB

Single Ended SAR ADC







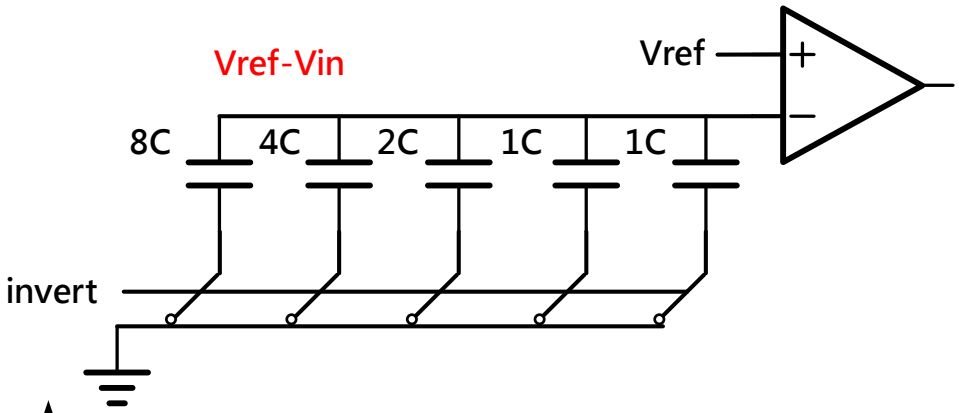


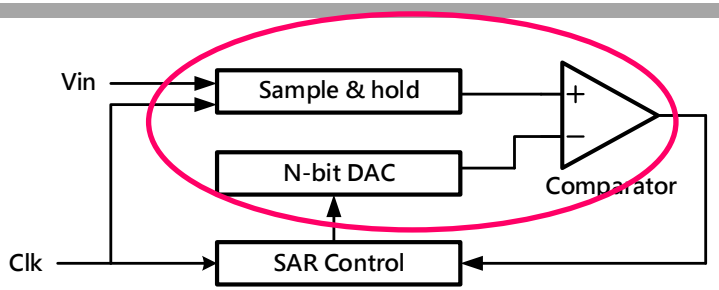
$$Vin=b0(\frac{1}{2})Vref+b1(\frac{1}{4})Vref+b2(\frac{1}{8})Vref$$

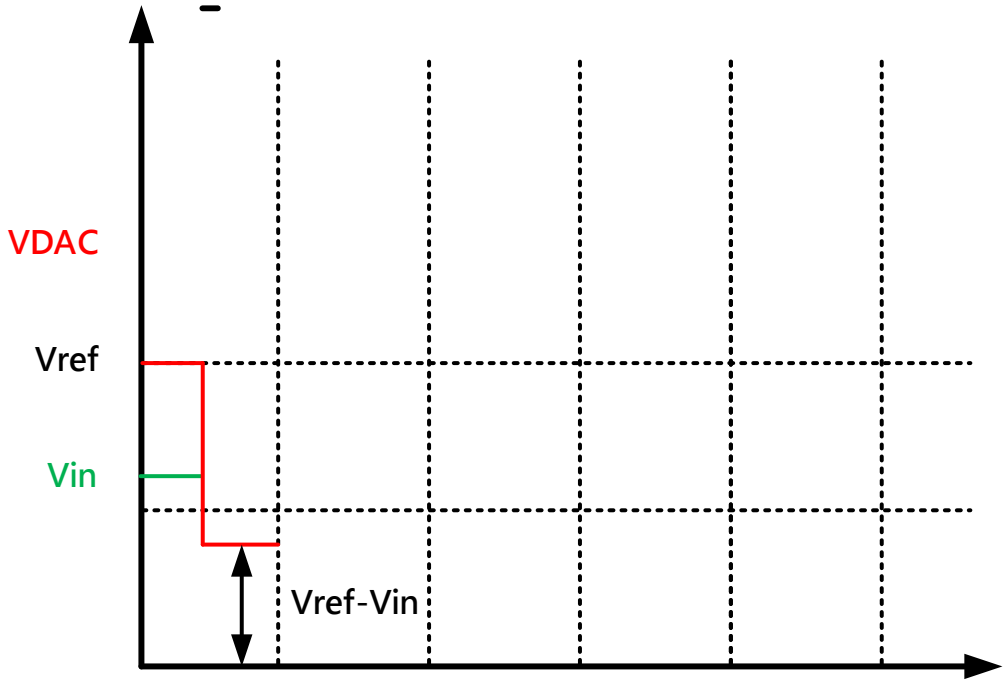
$$+b3(\frac{1}{16})Vref+Nq$$

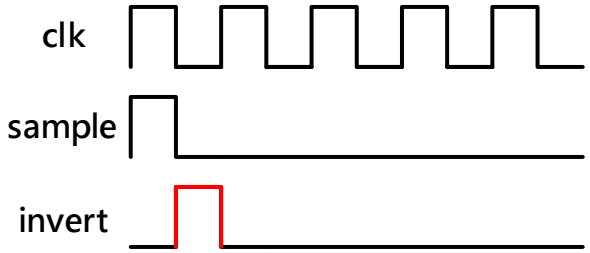
$$VDAC=Vref$$

Single Ended SAR ADC





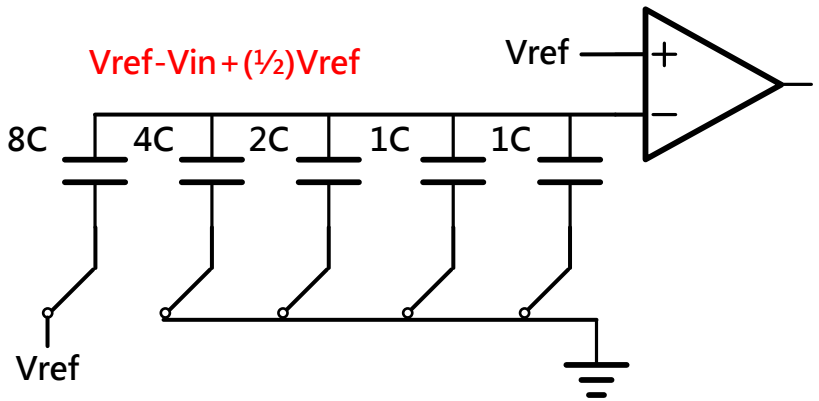


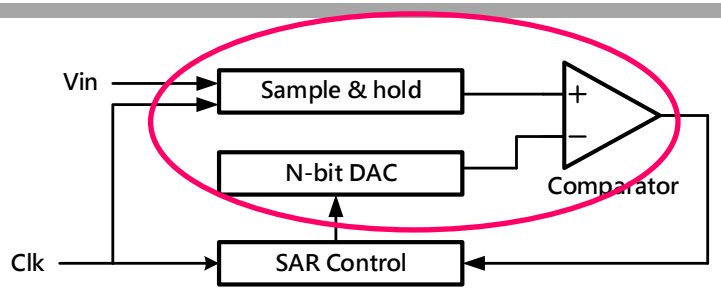


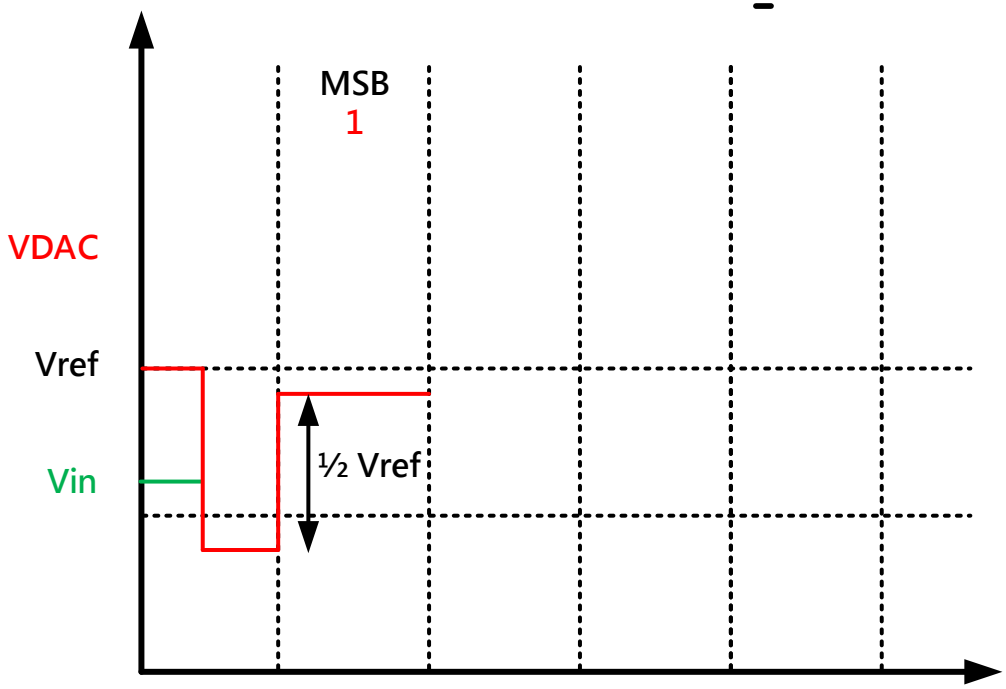
$$Vin=b0(\frac{1}{2})Vref+b1(\frac{1}{4})Vref+b2(\frac{1}{8})Vref+b3(\frac{1}{16})Vref+Nq$$

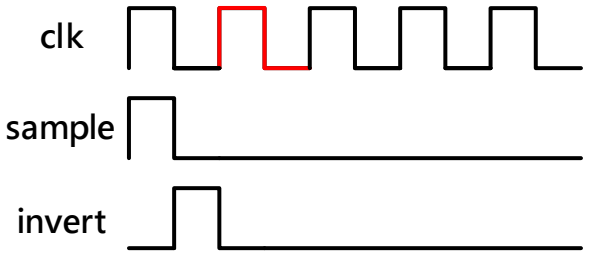
$$VDAC=Vref-Vin$$

Single Ended SAR ADC





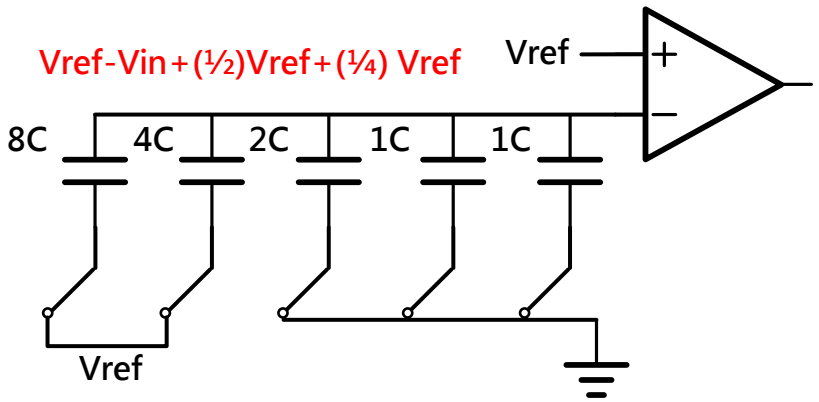


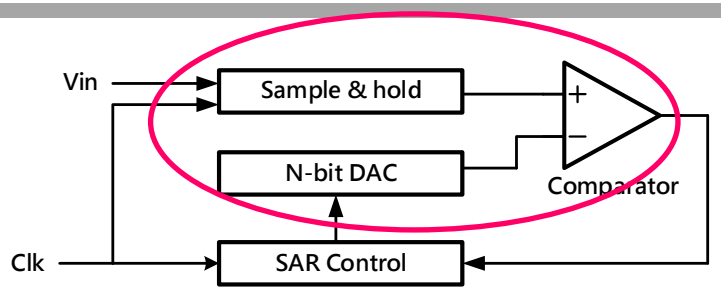


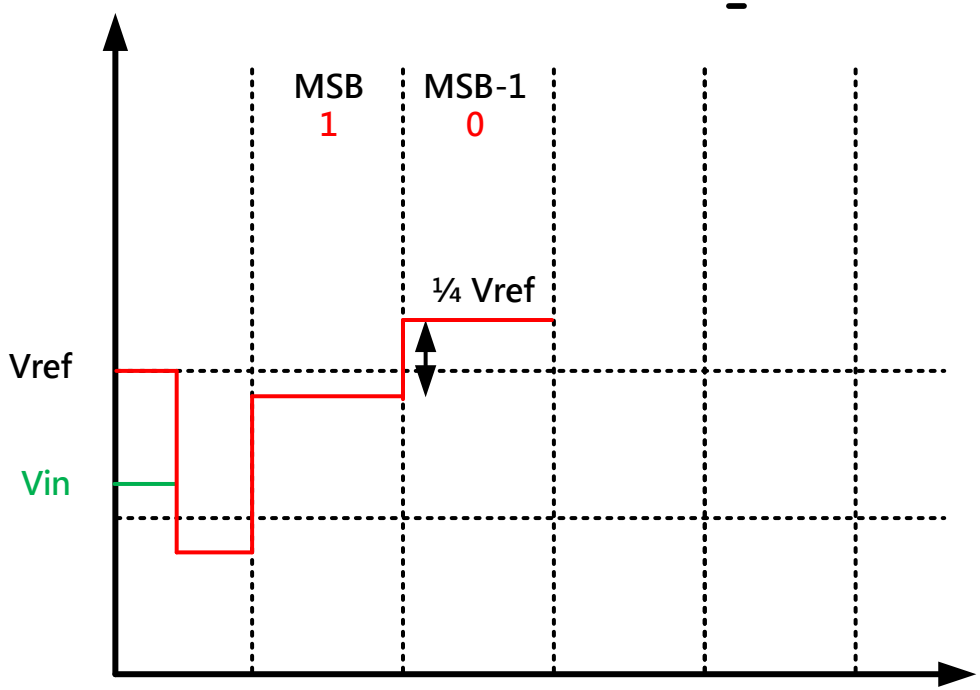
$$Vin=b0(\frac{1}{2})Vref+b1(\frac{1}{4})Vref+b2(\frac{1}{8})Vref+b3(\frac{1}{16})Vref+Nq$$

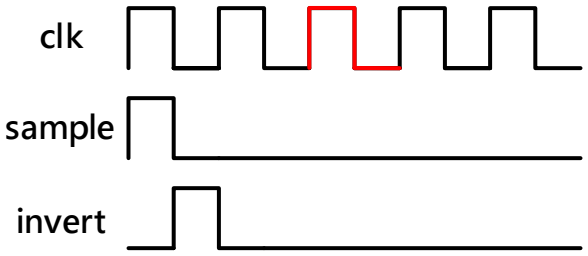
$$VDAC=Vref-Vin+(\frac{1}{2})Vref$$

Single Ended SAR ADC





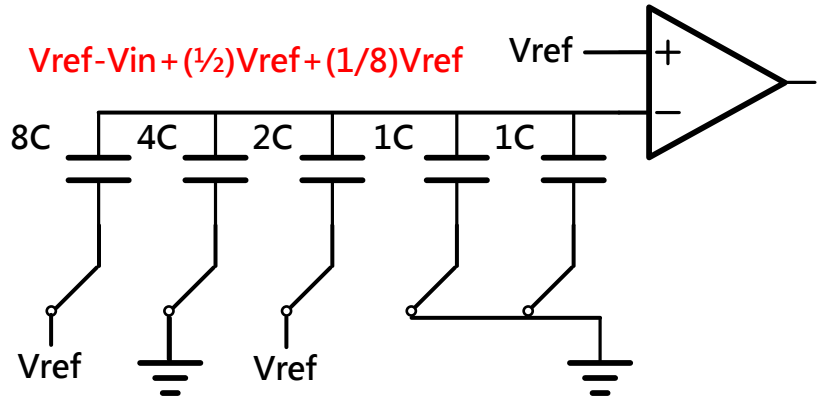


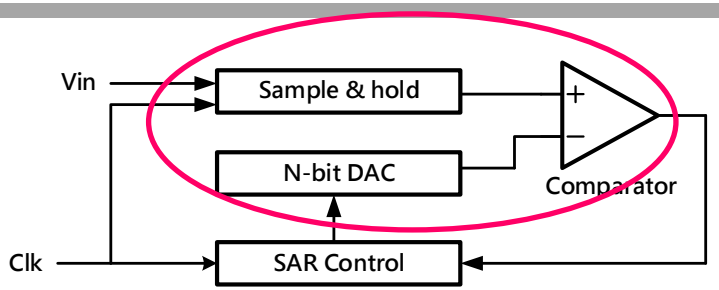


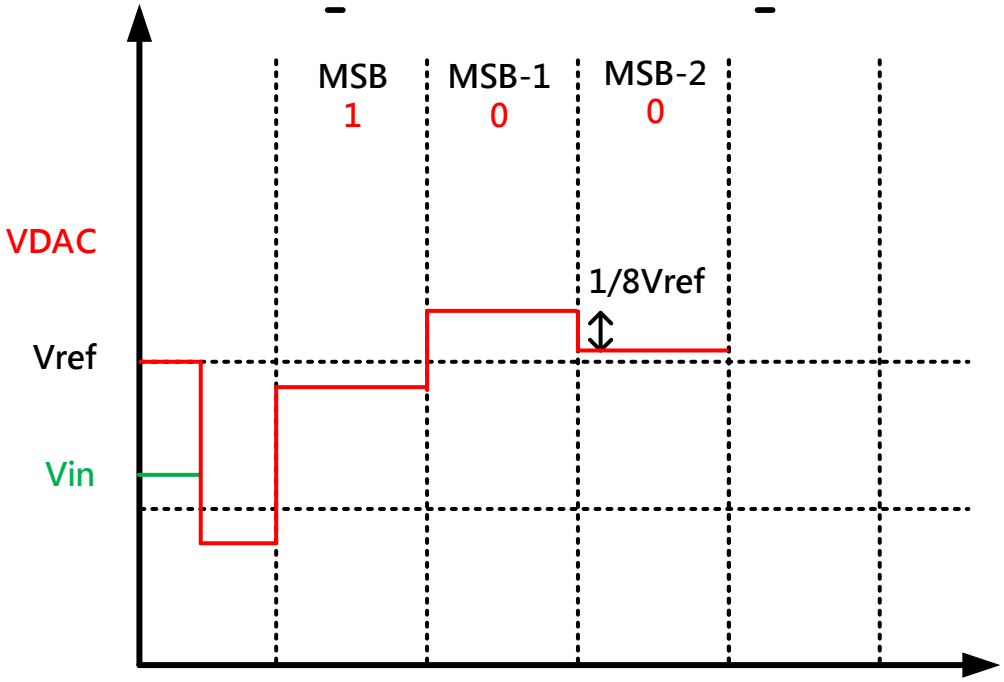
$$Vin=b0(\frac{1}{2})Vref+b1(\frac{1}{4})Vref+b2(\frac{1}{8})Vref+b3(\frac{1}{16})Vref+Nq$$

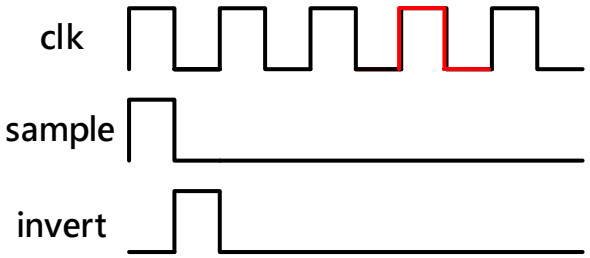
$$VDAC=Vref-Vin+(\frac{1}{2})Vref+(\frac{1}{4})Vref$$

Single Ended SAR ADC





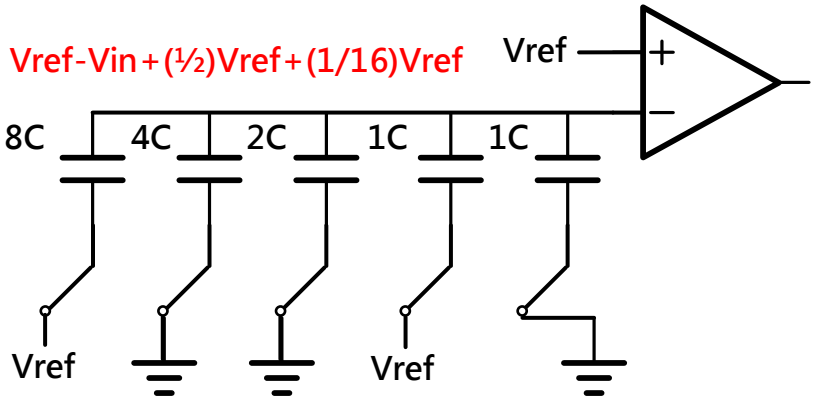


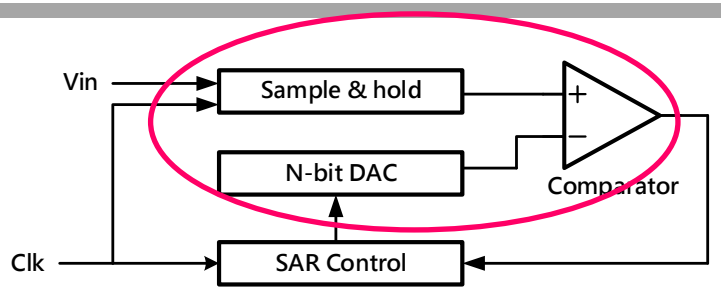


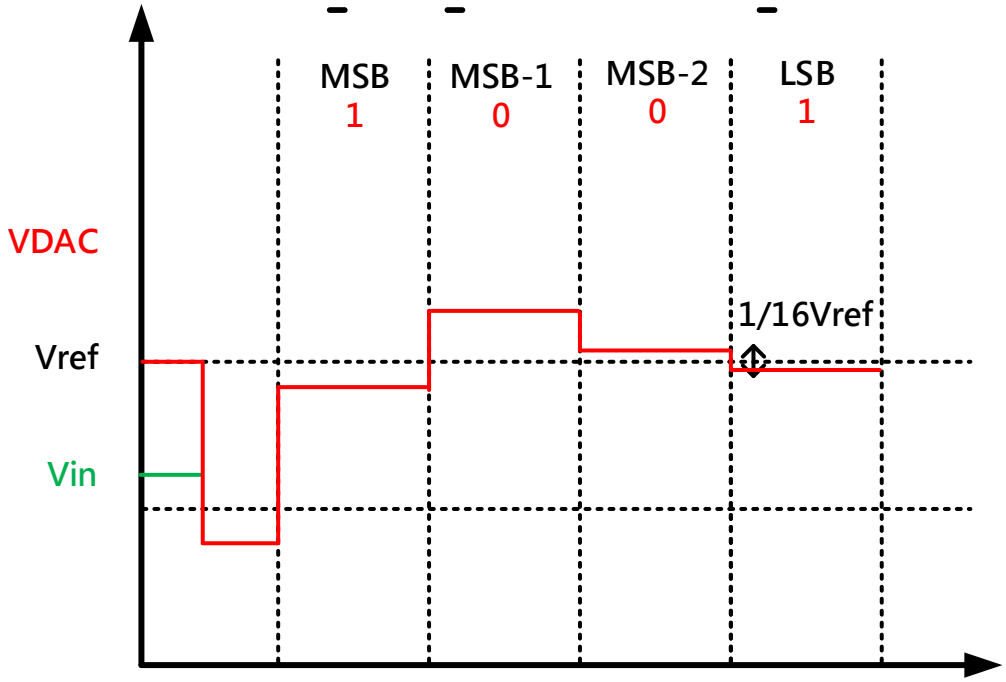
$$Vin=b0(\frac{1}{2})Vref+b1(\frac{1}{4})Vref+b2(\frac{1}{8})Vref+b3(\frac{1}{16})Vref+Nq$$

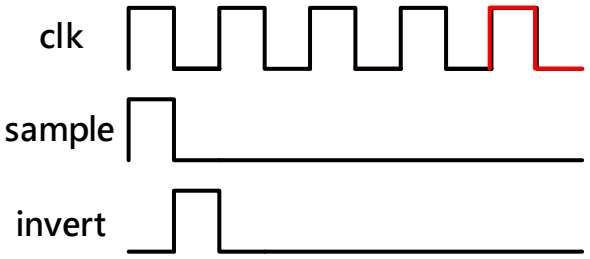
$$VDAC=Vref-Vin+(\frac{1}{2})Vref+(\frac{1}{8})Vref$$

Single Ended SAR ADC









$$Vin=b0(\frac{1}{2})Vref+b1(\frac{1}{4})Vref+b2(\frac{1}{8})Vref+b3(\frac{1}{16})Vref+Nq$$

$$VDAC=Vref-Vin+(\frac{1}{2})Vref+(\frac{1}{16})Vref$$

$$b0=1,\ b1=0,\ b2=0,\ b3=1$$

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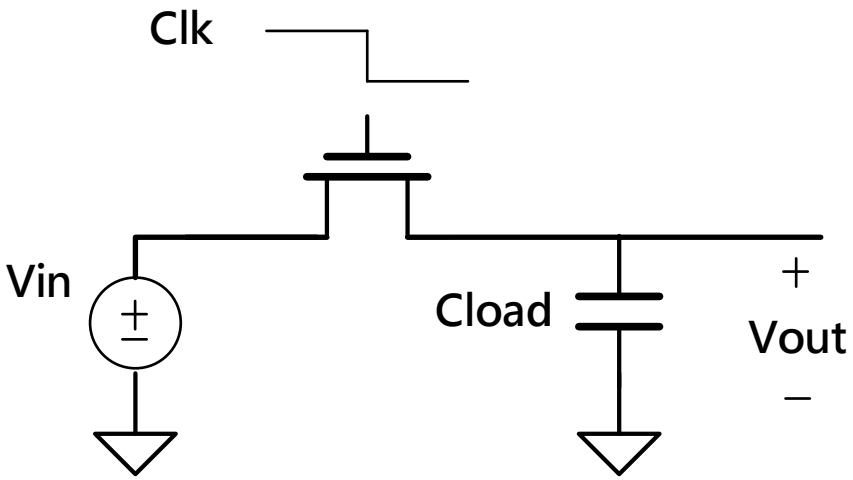
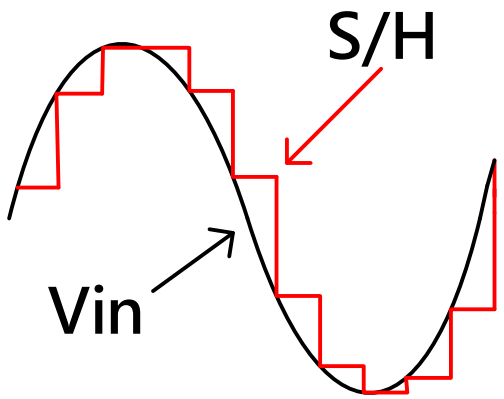
7. Low Power Design Case Study

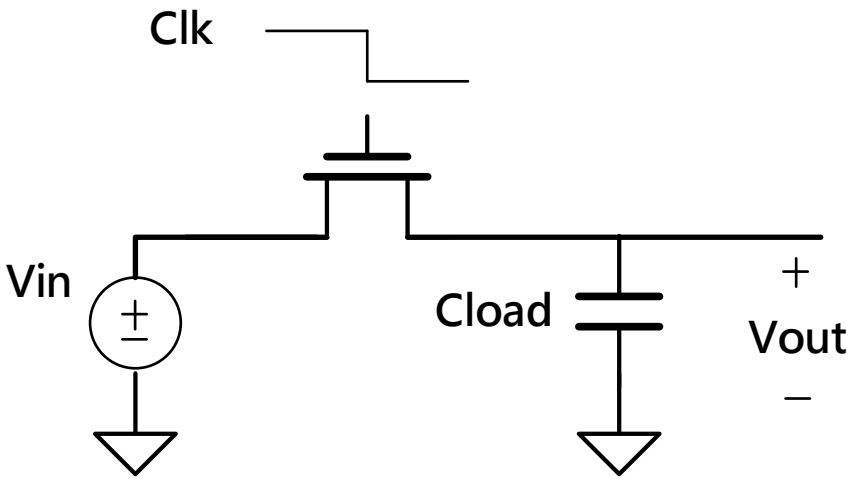
Sample and Hold

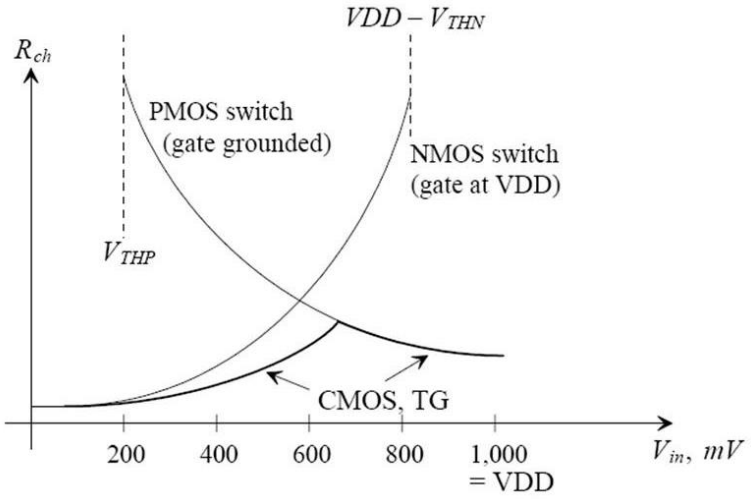




- Simple S/H concept using a NMOS and a capacitor
- When Clk is high, Vin is sampled on the sampling capacitor (Cload)
- Clk becomes low, Vin is held on Cload to perform conversion

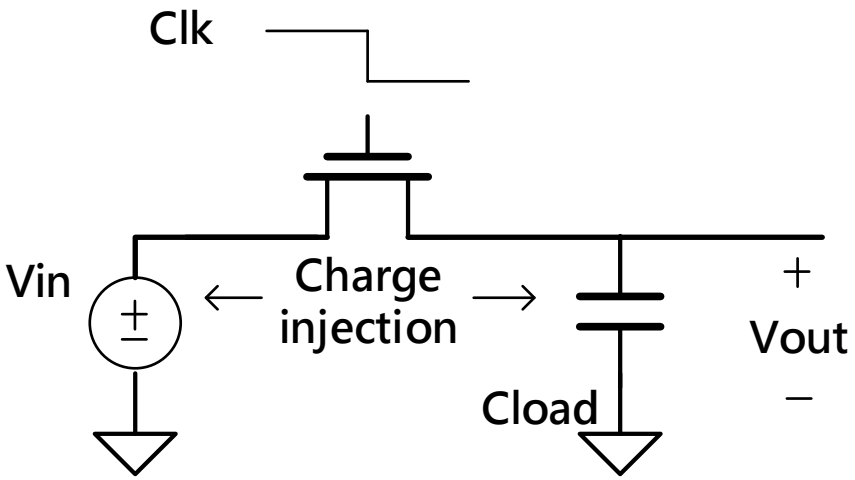
Sample and Hold – On-Resistance





- Because of threshold drop, NMOS only can pass the signal from 0 to VDD-Vth
- $R_{on} = \frac{L}{W} \frac{1}{\mu_n C_{ox}(V_{gs} - V_{th})}$
- On resistance is signal-dependent, which leads to non-linearity error

Sample and Hold – Charge Injection



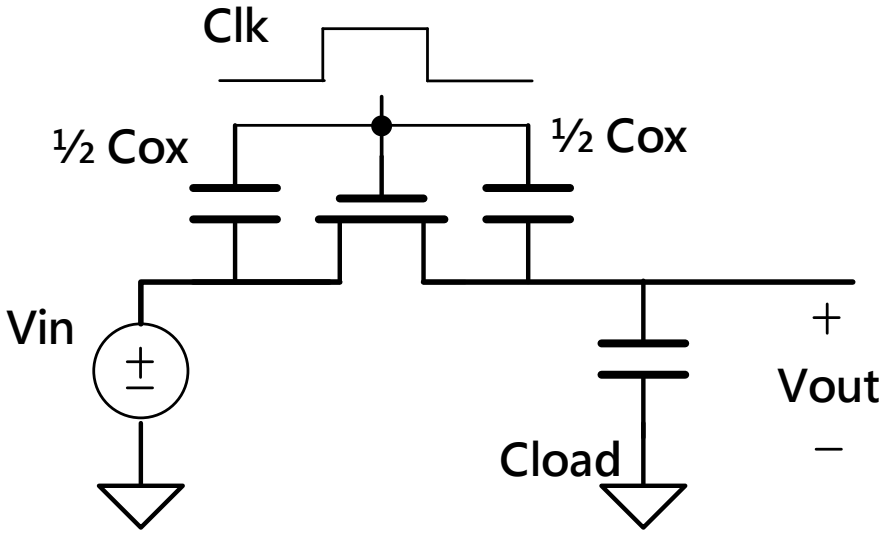
- When MOS turns off, stored charges are injected into Vin and Cload, results in voltage change across capacitor

$$\mathrm{Q} = C_{ox} \cdot W \cdot L \cdot (V_{gs} - V_{th})$$

$$\Delta V = \frac{C_{ox} \cdot W \cdot L \cdot (VDD - V_{in} - V_{th})}{2C_{load}}$$

- Voltage change across Cload is signal-dependent, which leads to nonlinearity and harmonic distortion

Sample and Hold – Clock Feedthrough



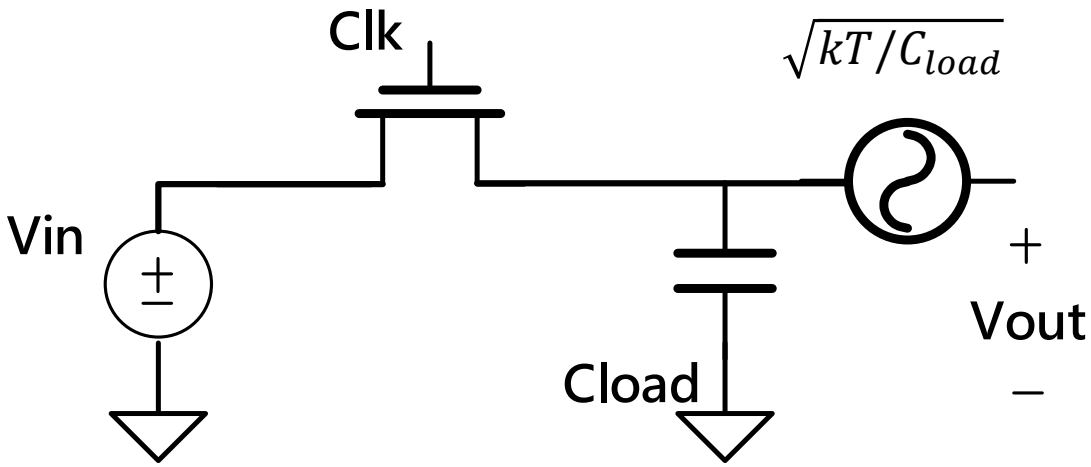
- When Clk goes from high to low, the capacitance between the gate and source or drain will couple the voltage onto the loading capacitance

$$\Delta V = \frac{C_{overlap} \cdot VDD}{C_{load} + C_{overlap}}$$

$$C_{overlap} = C_{ox} \cdot W \cdot LD$$

- LD is the length of the gate that overlap the drain/source

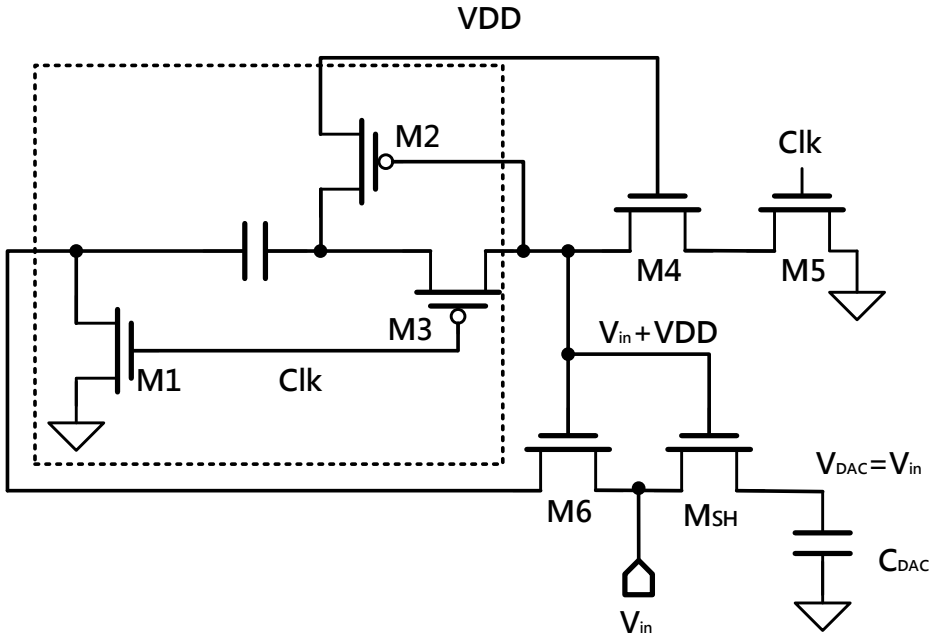
Sample and Hold – kT/C noise



$$V_n^2 = \frac{kT}{C_{load}}$$

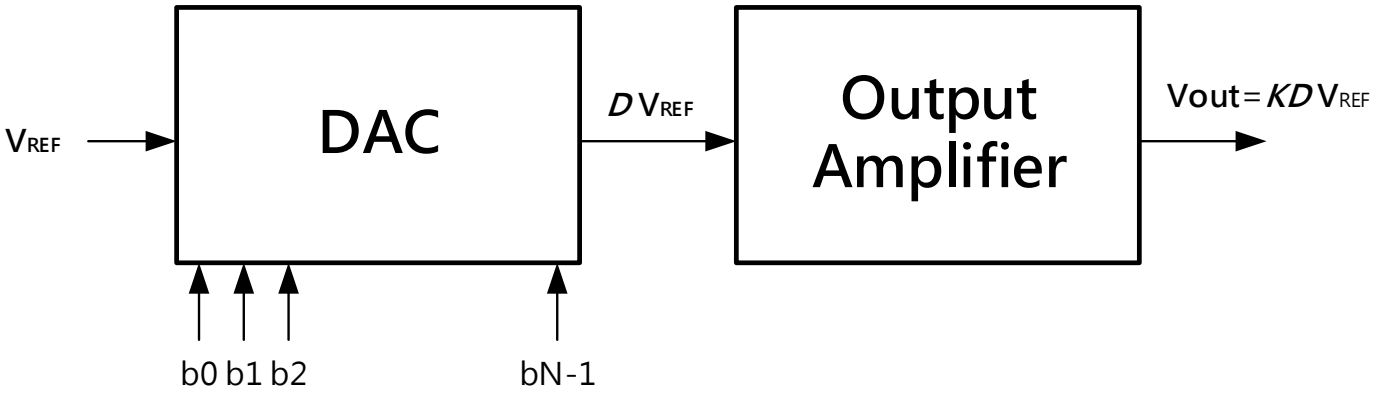
- To achieve higher precision and lower noise, larger sampling capacitor is better
- Larger sampling capacitance needs more settling time
- Trade-off between speed and precision

Sample and Hold – Bootstrapped



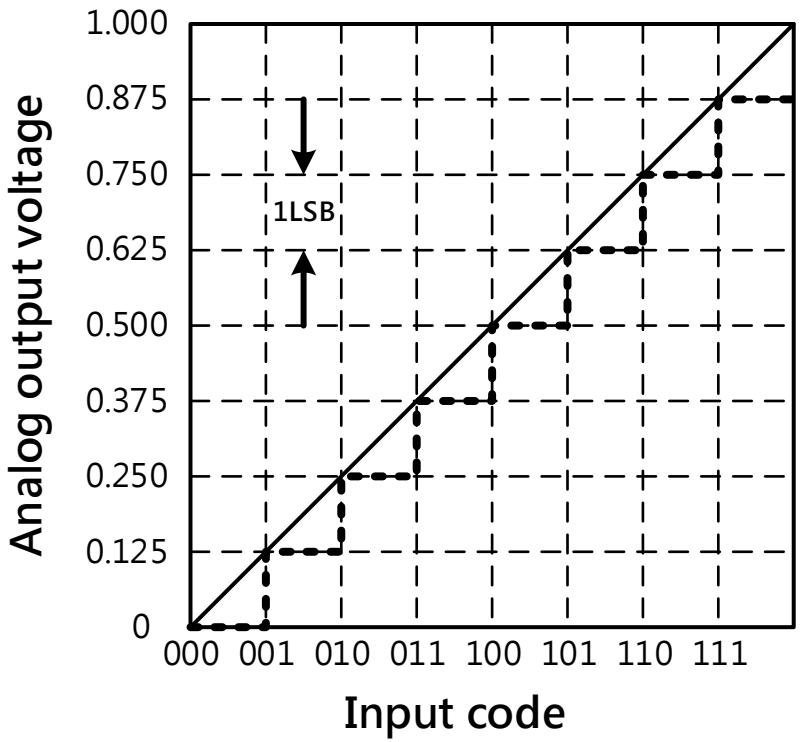
- Under low voltage operation, the gate-source voltage of sampling switch is limited and increases the on-resistance
- The on-resistance results in sampled signal loss
- By the bootstrapped technique, the gate-source of sampling switch is boosted and signal independent

Digital-Analog Converter



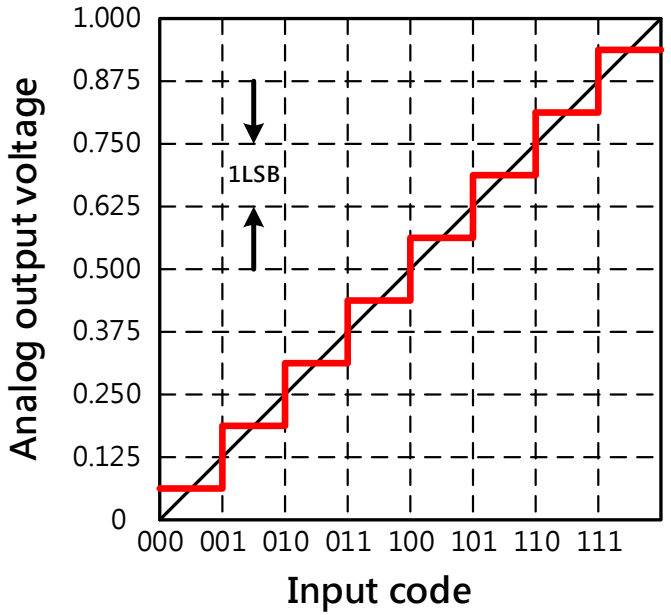
- N-bits(b0,b1,b2…,bN-2,bN-1)
- Reference voltage V_{REF}
- b0 is most significant bit(MSB)
- bN-1 is least significant bit(LSB)
- $D = \frac{b0}{2^1} + \frac{b1}{2^2} + \frac{b2}{2^3} + \cdots + \frac{bN-1}{2^N}$
- $\mathrm{Vout} = \mathrm{KV_{REF}}(\frac{b0}{2^1} + \frac{b1}{2^2} + \frac{b2}{2^3} + \cdots + \frac{bN-1}{2^N})$

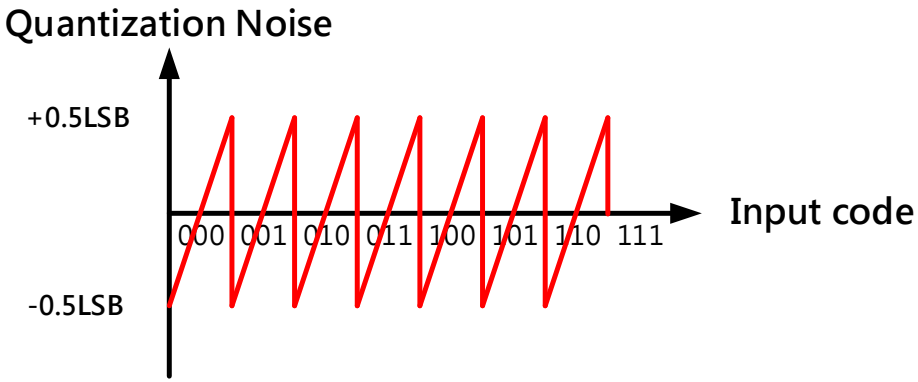
Static Characteristic of DAC



- Ideal input-output of a 3-bit DAC
  - $\text{LSB} = \frac{Vref}{2^N}$
  - Full scale(FS)$= Vref - LSB$
    $= Vref\left(1 - \frac{1}{2^N}\right)$
  - $FSR = \lim_{N\to\infty} FS = Vref$
  - Dynamic range(DR)$= \frac{FSR}{LSB} = \frac{FSR}{(FSR/2^N)} = 2^N = 6.02N\ dB$

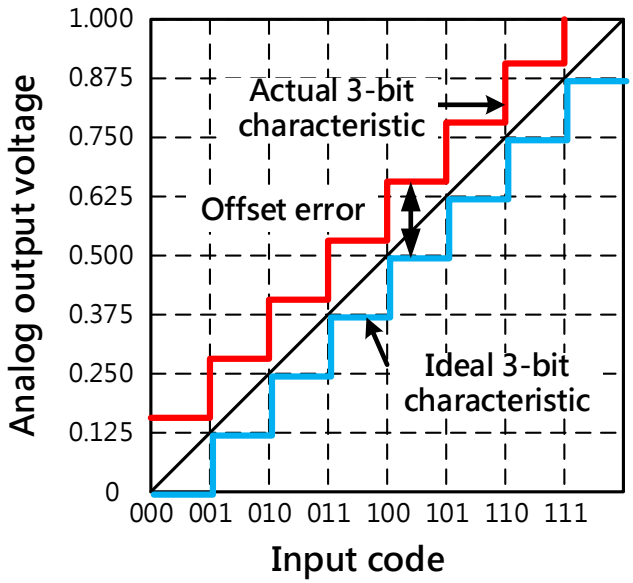
Static Characteristic of DAC

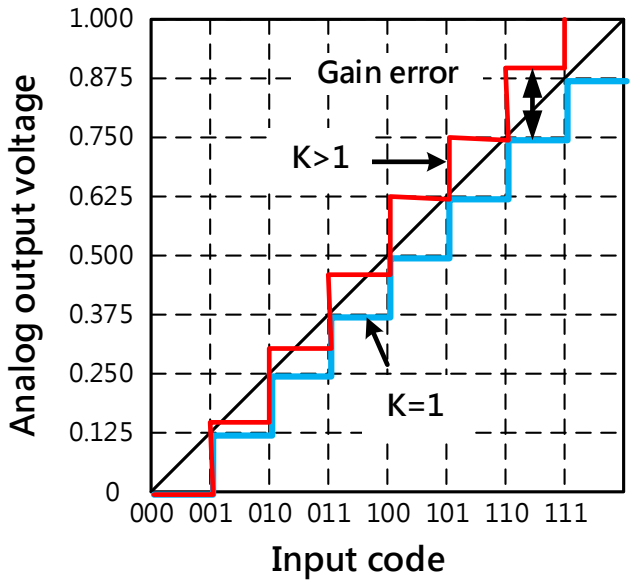




- Quantization noise
  - Analog output of infinite-bit DAC minus the output of finite-bit DAC
- Signal-to-noise ration(SNR)
  - Ratio of the full scale value to the rms value of the quantization noise
  - $\text{rms} = \sqrt{\frac{1}{T}\int_0^T LSB^2(\frac{t}{T} - 0.5)^2 dt}$
    $= \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N\sqrt{12}}$
  - $SNR = \frac{FSR/(2\sqrt{2})}{FSR/(2^N\sqrt{12})} = \frac{2^N\sqrt{6}}{2}$
  - $SNR(dB) = 20\log\left(\frac{2^N\sqrt{6}}{2}\right) = 6.02N + 1.76$
  - $ENOB = \frac{SNR-1.76}{6.02}$

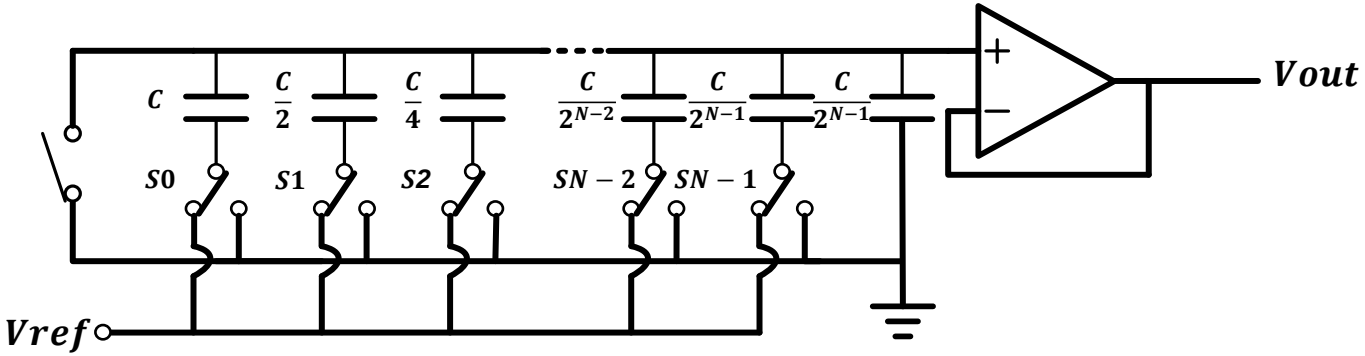
Static Characteristic of DAC





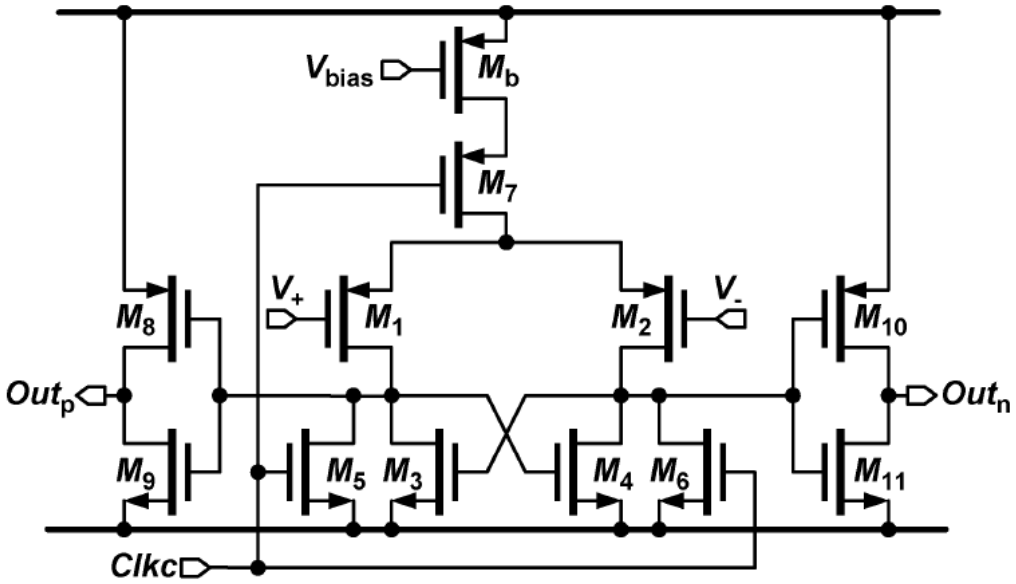
- Integral nonlinearity(INL)
  - $((V_i-V_{i,Ideal})/V_s)LSB$ V_s is the ideal change of bit-to-bit
- Differential nonlinearity(DNL)
  - $(((V_i-V_{i-1})/V_s)-1)LSB$ V_s is the ideal change of bit-to-bit

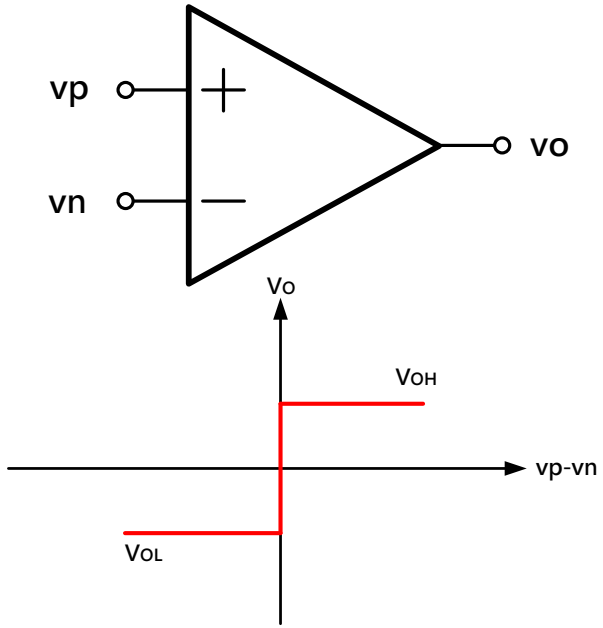
Charge Redistribution DAC



- Operate by binary dividing the total charge applied to a capacitor array
- By charge conservation
  - $VrefCeq = Vref\left(b0C + \frac{b1C}{2^1} + + \cdots + \frac{bN-1}{2^{N-1}}\right) = CtotVout = 2CVout$
  - $Vout = Vref(\frac{b0}{2^1} + \frac{b1}{2^2} + \frac{b2}{2^3} + \cdots + \frac{bN-1}{2^N})$

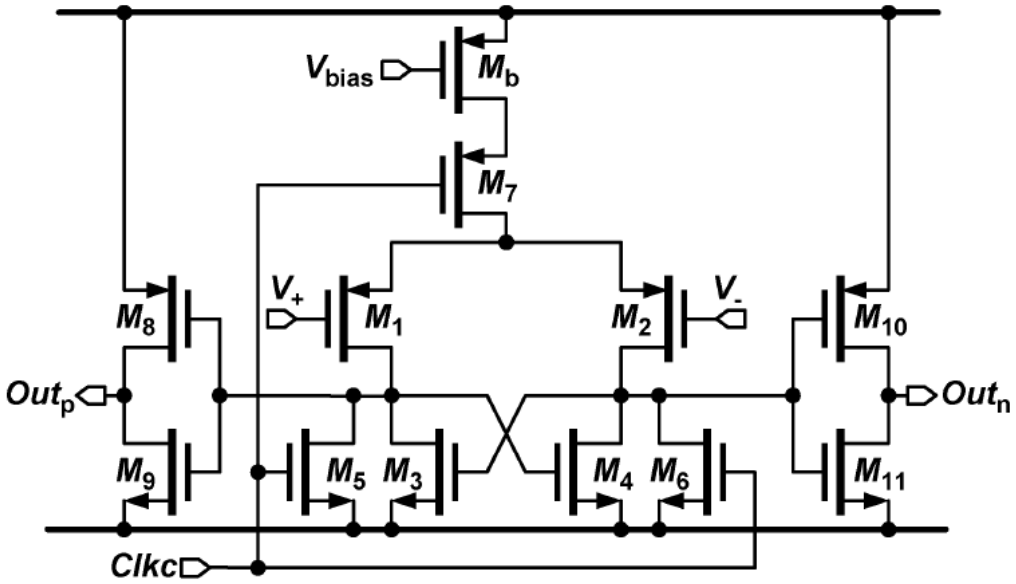
Comparator

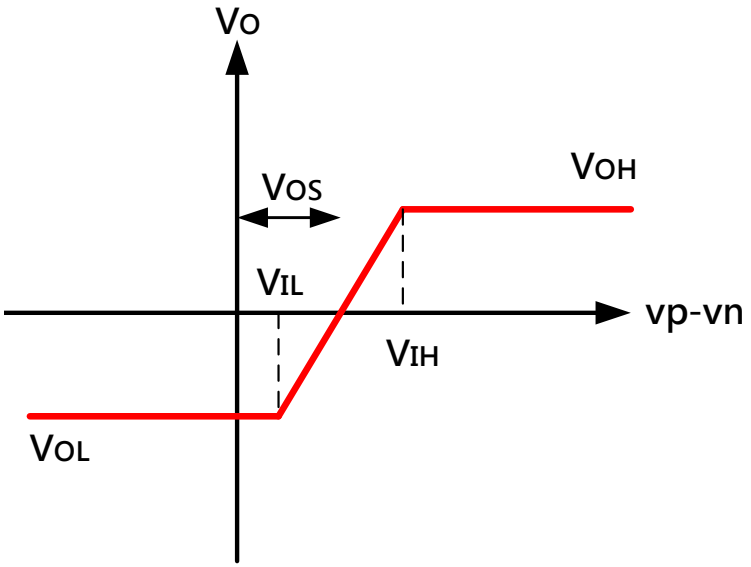




- A comparator is defined as a circuit that has a binary output whose value is based on a comparison of two analog inputs
- Gain=Av= $\lim_{\Delta V \to 0} \frac{V_{OH}-V_{OL}}{\Delta V}$

Comparator – Input Offset





- $V_{OS} = \Delta V_{TH1,2} + \frac{(V_{gs}-V_{TH})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right)$
- $\Delta S_{1,2}$ is the dimension mismatch between M1 and M2
- ΔR is the loading difference induced by M3-M6
- The input common-mode varies the input pair effective voltage which results the dynamic offset and degrades the performance

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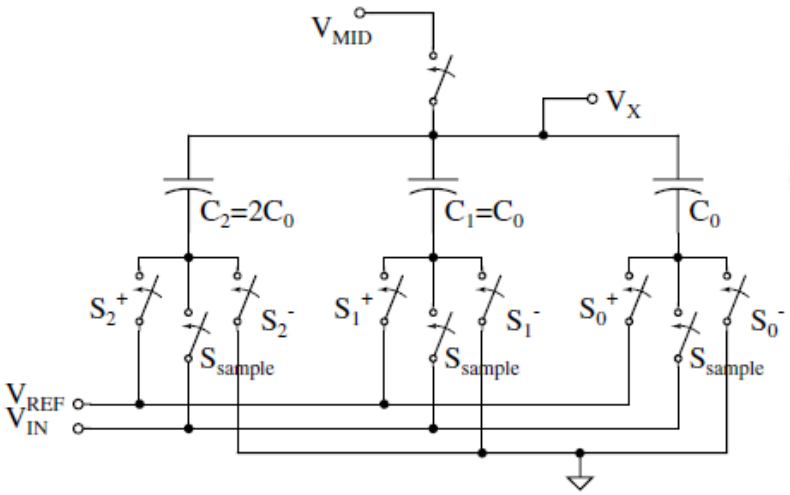
6. SAR Logic Implementation

Switching Energy

- Assume that at time 0^-, the input voltage has been sampled on the capacitor array and all switches are open. At time 0, the bottom plate of C_2 is switched to V_{REF}. The capacitor array is then charged to reach the final value. If the capacitor array settles in time T_P, the total energy drawn from V_{REF} is



$$E_{0\to 1} = \int_{0^+}^{T_P} i_{REF}(t) V_{REF} dt = V_{REF} \int_{0^+}^{T_P} i_{REF}(t) dt$$

$$E_{0\to 1} = -V_{REF} \int_{0^+}^{T_P} \frac{dQ_{C_2}}{dt} dt = -V_{REF} \int_{Q_{C_2}(0^+)}^{Q_{C_2}(T_P)} dQ_{C_2}$$

$$= -V_{REF}(Q_{C_2}(T_P) - Q_{C_2}(0^+))$$

$$= -V_{REF} 2C_0 \left((V_X[1] - V_{REF}) - V_X[0]\right)$$

An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC, ISCAS'05

Switching Energy

- The capacitor switched from ground to V_{REF} consumes $E_{0->1}$

$$E_{0\to 1}=CV_{REF}(V_{REF}-\Delta V_X) \qquad (1)$$

- The remaining capacitor connected to V_{REF} consumes E_{TOP}

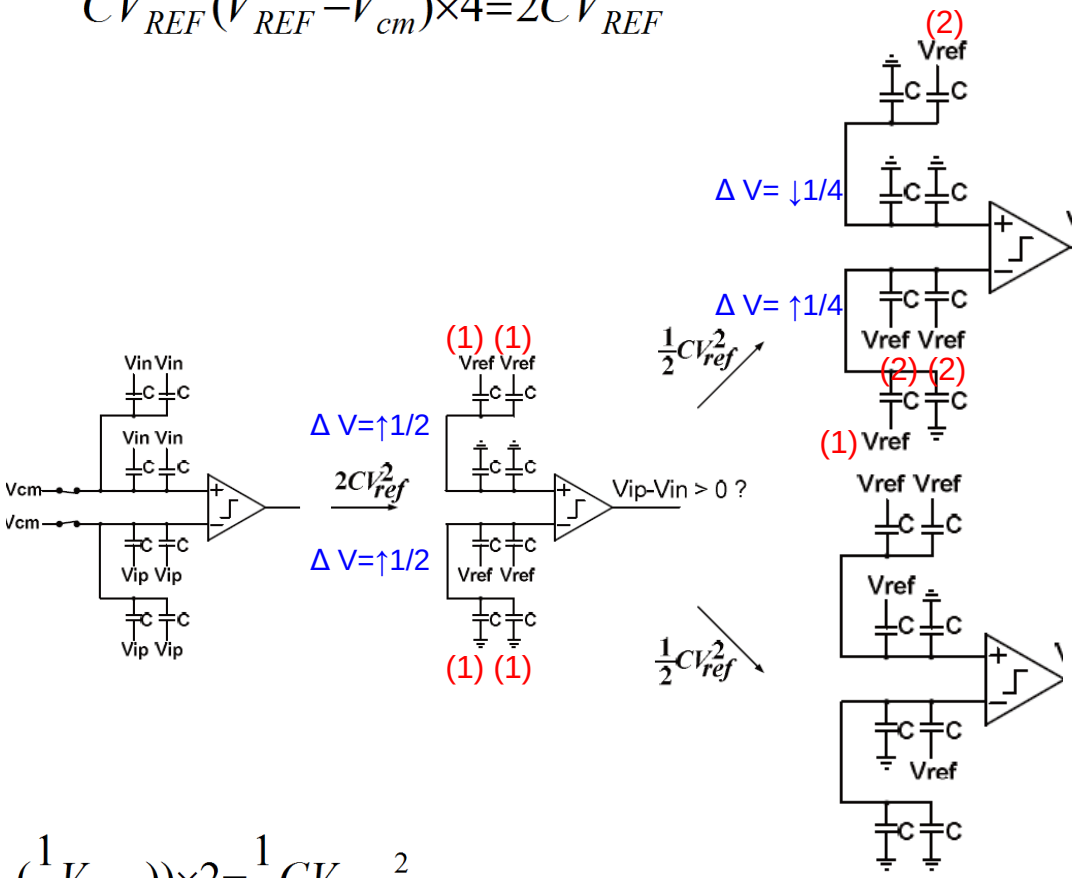
$$E_{TOP}=CV_{REF}(-\Delta V_X) \qquad (2)$$

Example

- The first step switches 4C to V_{REF} and consumes

$$CV_{REF}(V_{REF}-V_{cm})\times 4=2CV_{REF}^{\ 2}$$

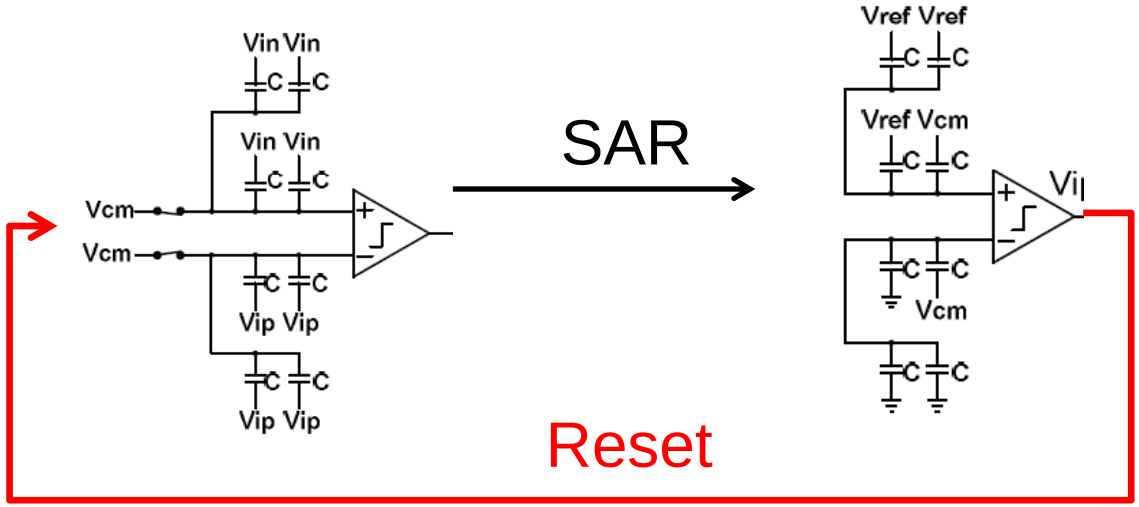
- The second step switches 1C from V_{REF} to ground on non-inverting input, and 1C from ground to V_{REF} on inverting input. That consumes



$$CV_{REF}(-(-\frac{1}{4}V_{REF}))=\frac{1}{4}CV_{REF}^{\ 2}$$

$$CV_{REF}(V_{REF}-(\frac{1}{4}V_{REF}))+CV_{REF}(-(\frac{1}{4}V_{REF}))\times 2=\frac{1}{4}CV_{REF}^{\ 2}$$

Reset Energy



- Reset energy is defined as DAC energy consumed before the next sampling
- Some switching method consumes zero reset energy. Ex: Vcm-based and set-and-down switching method
- Some switching method consumes reset energy. Ex: CAS switching method

Outline

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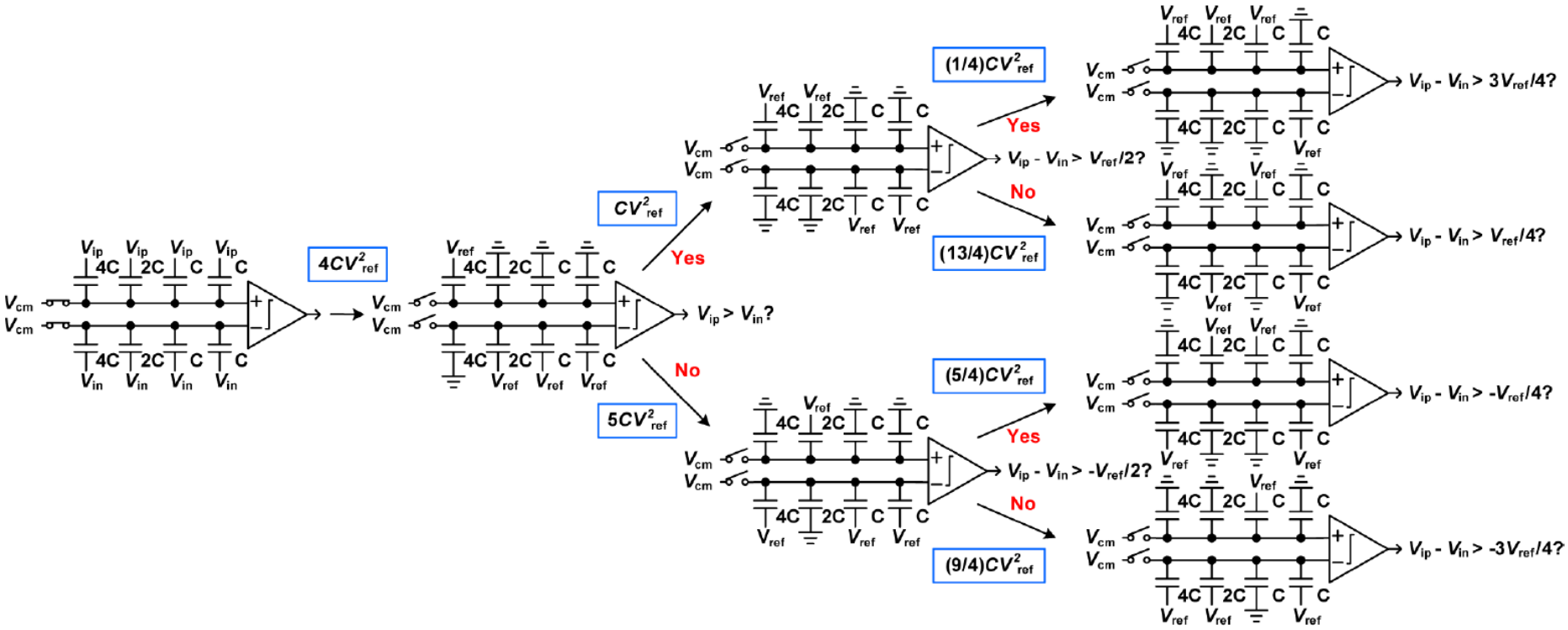
Conventional Switching



3-bit Conventional DAC switching procedure

Split Capacitor Switching

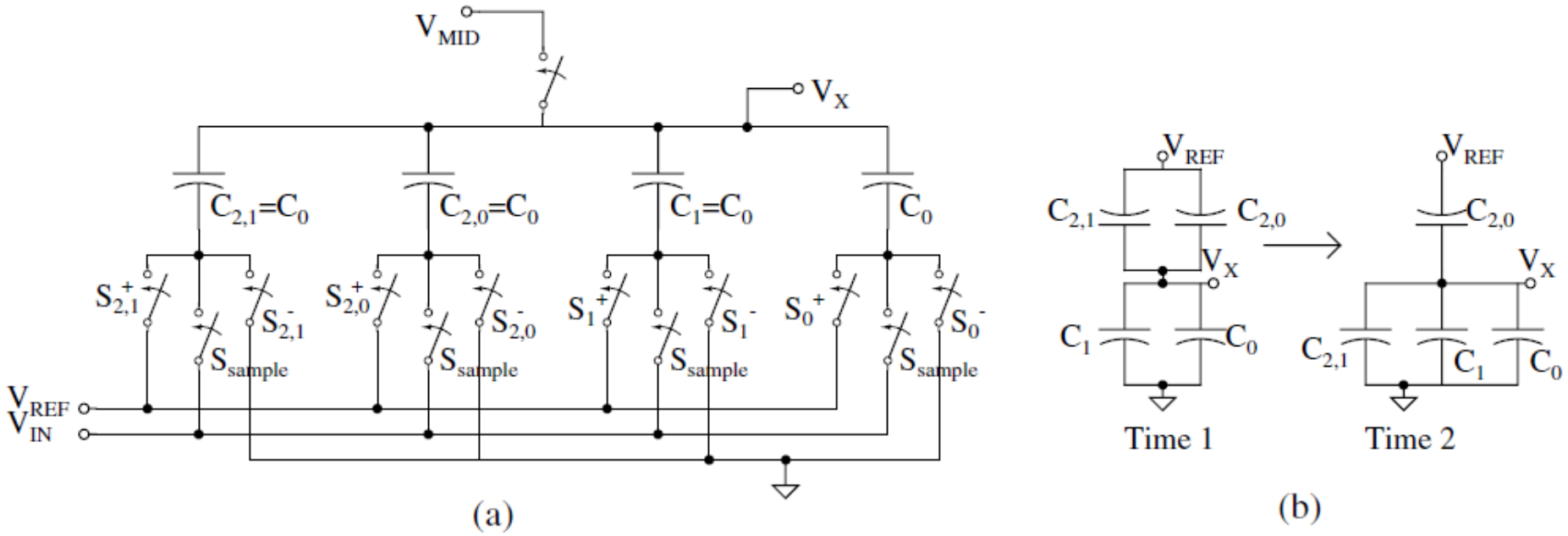


Fig. (a) 2-bit Split capacitor DAC (b) MSB capacitor C_2 has been split into $C_{2,1}$ and $C_{2,2}$

- Split the MSB capacitor into sub-array which is same as the remaining capacitor array
- “down” transition is power-efficient

Set-and-Down Switching

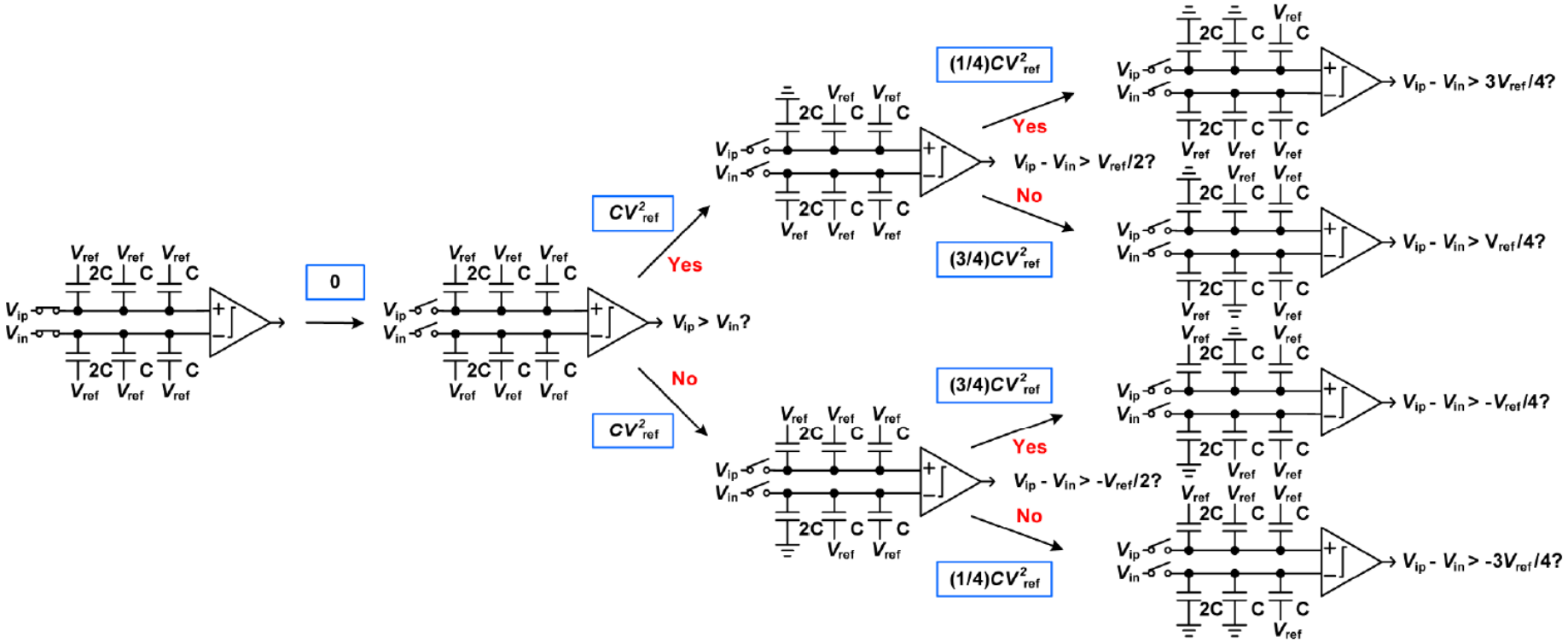


Fig. 3-bit set-and-down DAC switching procedure

- Reset to reference high, V_{REF}, then monotonically switch down
- Common mode voltage varies with every transition

Vcm-Based Switching

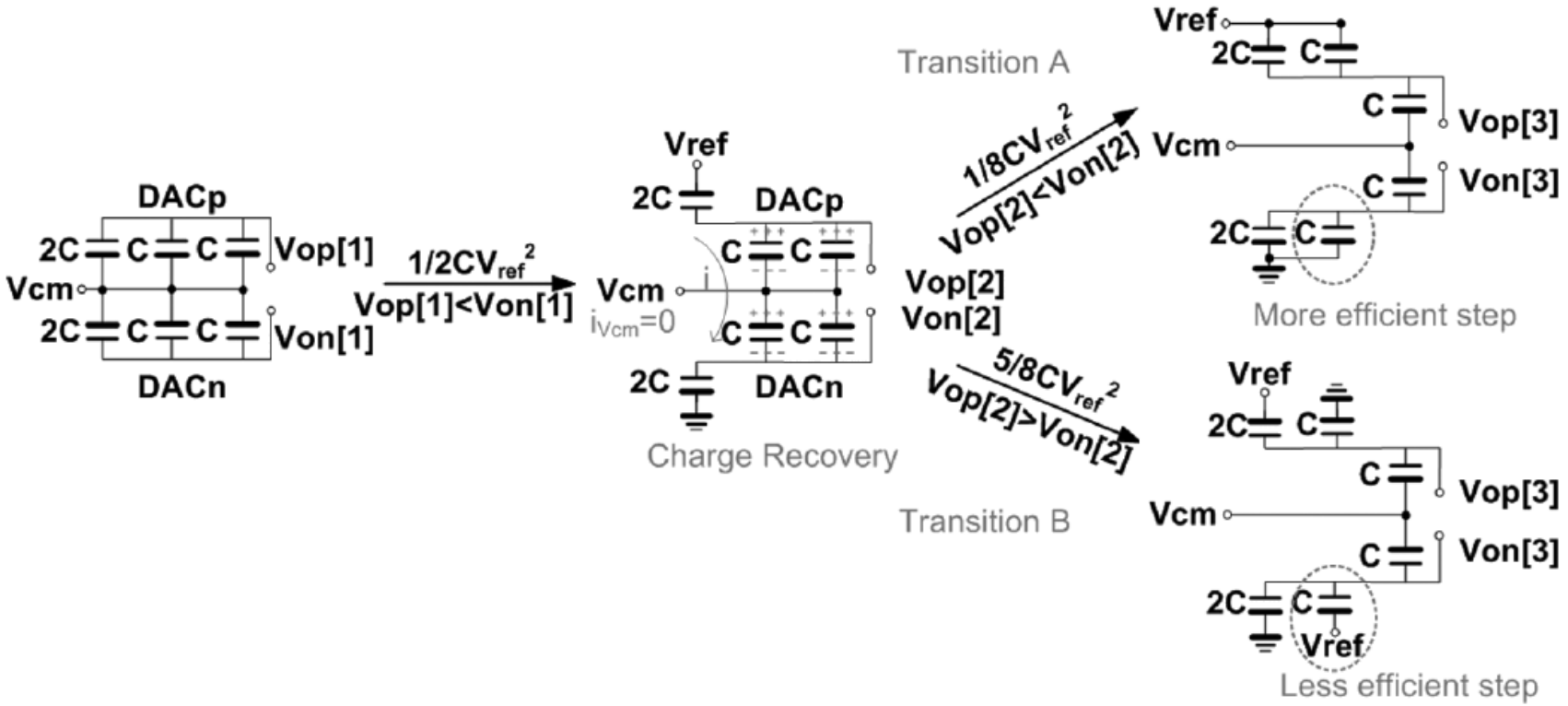


Fig. 3-bit Vcm-based DAC switching procedure

- Additional voltage source Vcm is needed
- Common mode voltage is fixed

Capacitor Average Switching

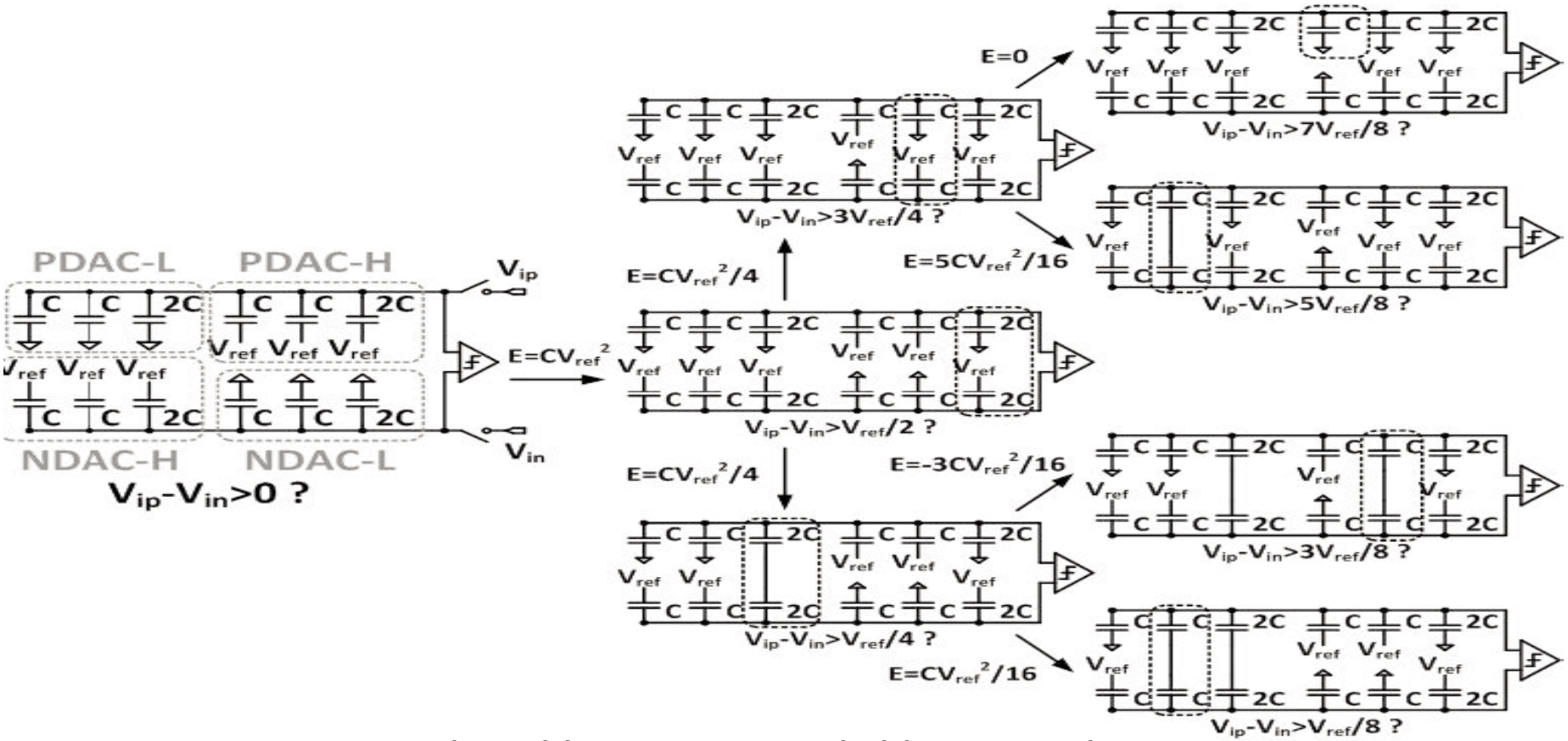
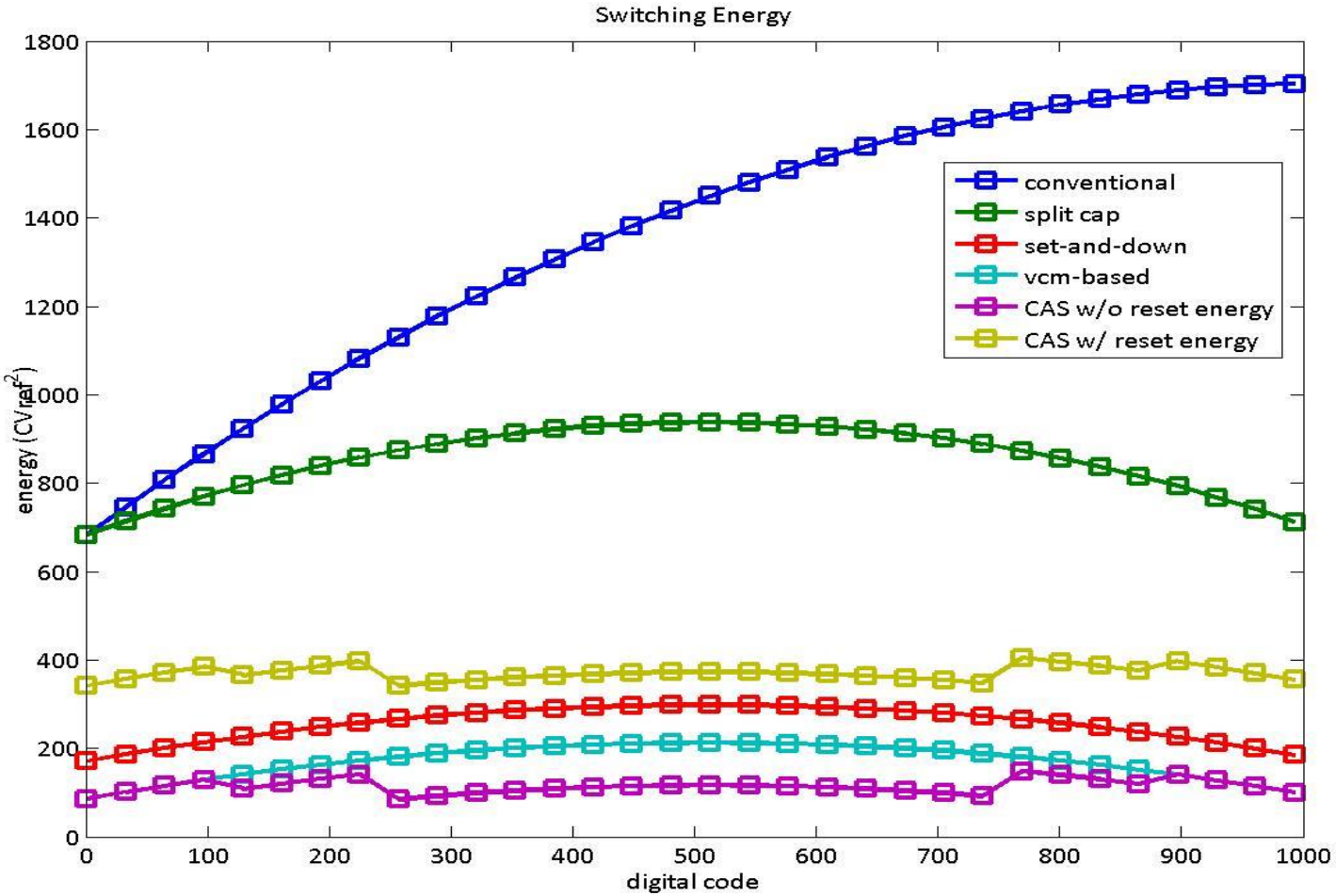


Fig. 4-bit CAS DAC switching procedure

- Efficient switching energy but has reset energy

Switching Energy Comparison



10-bit DAC switching energy

Switching Energy Comparison

	Conventional	Split cap	Set-and-down	Vcm-based	CAS
Normalized Energy(%)	100	62.5	18.75	12.5	8.37
No. of switches	6n+6	12n-2	4n-2	6n-4	8n-8+2m
No. of binary caps	2n+2	4n	2n	2n	4n-4
No. of unit caps	2^n	2^n	2^{n-1}	2^{n-1}	2^{n-1}

† "m" depends on how many steps using CAS technique

Table. Comparison of switching schemes for N-bit SAR ADC

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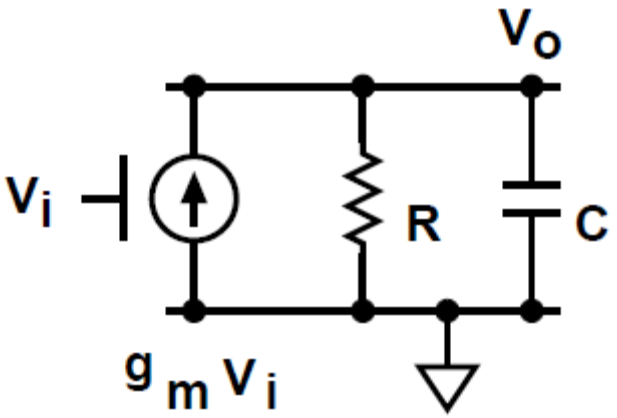
Single-Pole Amplifier

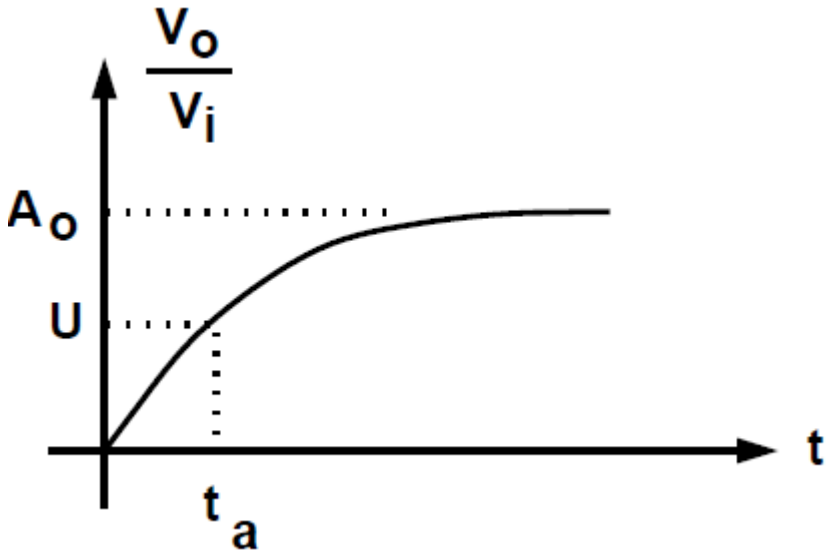
- The comparator amplification gain is

$$U = \frac{V_o}{V_i} = A_o[1 - e^{-t_a/(RC)}] \qquad A_o = g_m R \qquad \tau_m = \frac{C}{g_m}$$

- The relation between amplification gain U and time t_a is

$$\frac{t_a}{\tau_m} = A_o \times \ln\left(\frac{1}{1 - \frac{U}{A_o}}\right)$$





Positive-Feedback Regeneration

- The comparator amplification gain is

$$C\frac{dV_{O1}}{dt}+\frac{V_{O1}}{R}+g_mV_{O2}=0 \qquad C\frac{dV_O}{dt}+\frac{V_O}{R}+g_mV_O=0$$

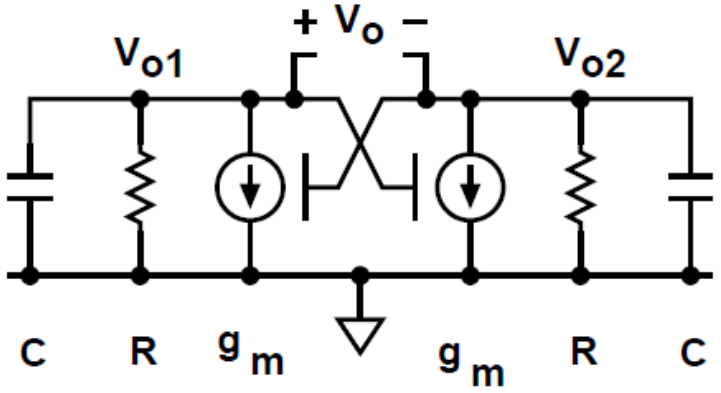
$$C\frac{dV_{O2}}{dt}+\frac{V_{O1}}{R}+g_mV_{O1}=0 \qquad V_O=V_{O1}-V_{O2}$$

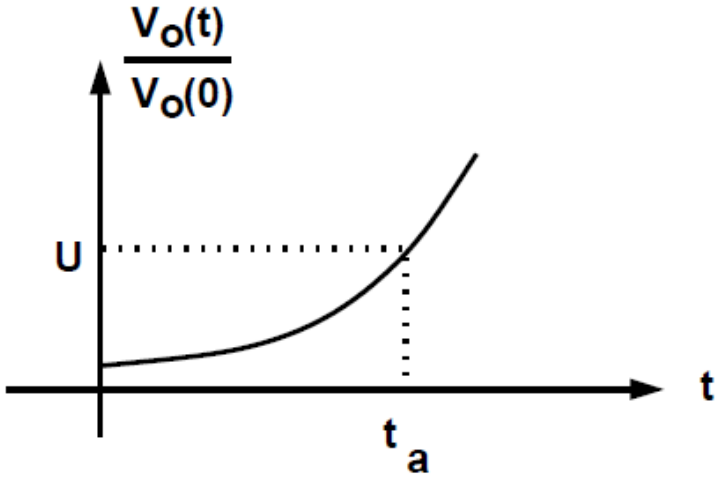
$$\Rightarrow \quad U=\frac{V_O(ta)}{V_O(0)}=e^{t_a/\tau_r} \qquad A_O=g_mR$$

$$\tau_r=\frac{RC}{A_O-1}=\frac{\tau_m}{1-1/A_O} \qquad \tau_m=\frac{C}{g_m}$$

- The relation between amplification gain U and time t_a is

$$\frac{t_a}{\tau_m}=\frac{1}{1-\frac{1}{A_O}}\times\ln(U)$$



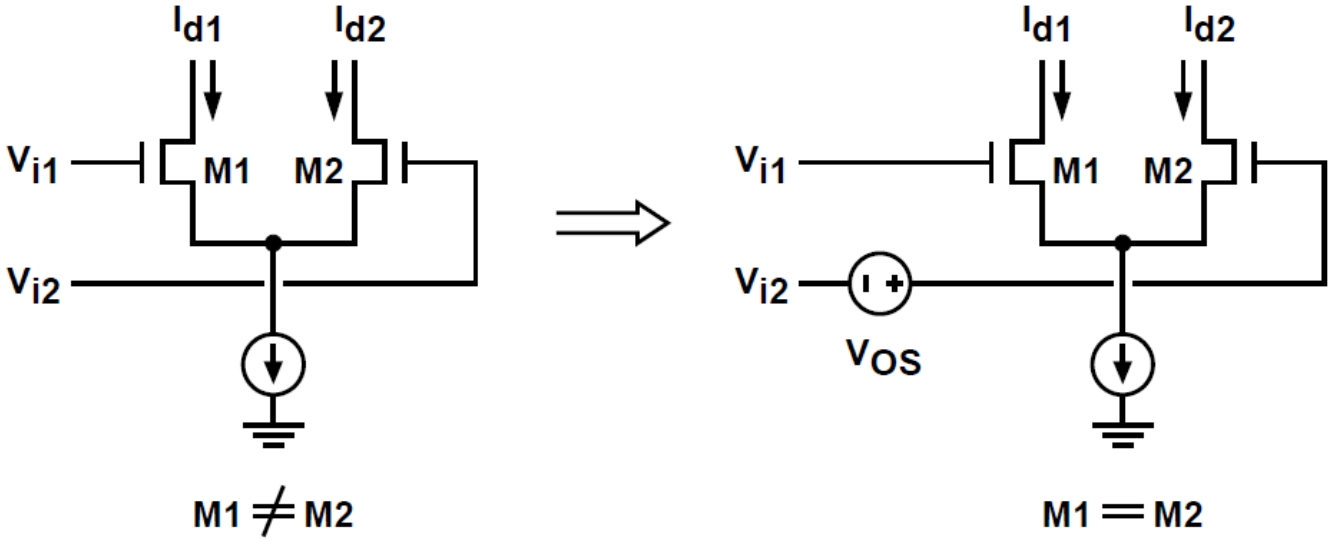


Offset of a Source-Coupled Pair

- The equivalent input offset is

$$\sigma^2(V_{OS}) = \sigma^2(\Delta V_t) + \left(\frac{V_{OV}}{2}\right)^2 \times \frac{\sigma^2(\Delta\beta)}{\beta^2} = \frac{1}{W \times L}\left(A_{V_t}^2 + \frac{V_{OV}^2}{4} \times A_\beta^2\right)$$

$$\beta = \mu C_{OX}\frac{W}{L} \qquad \sigma^2(\Delta V_t) = \frac{A_{V_t}^2}{W \times L} \qquad \frac{\sigma^2(\Delta\beta)}{\beta^2} = \frac{A_\beta^2}{W \times L}$$

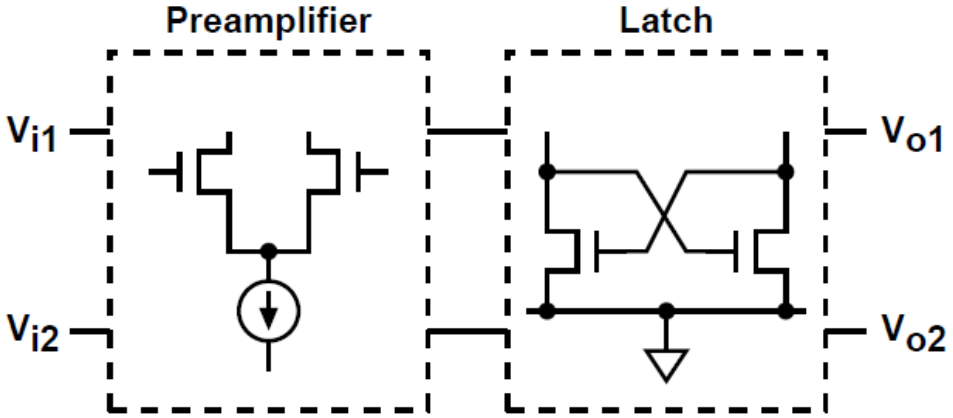


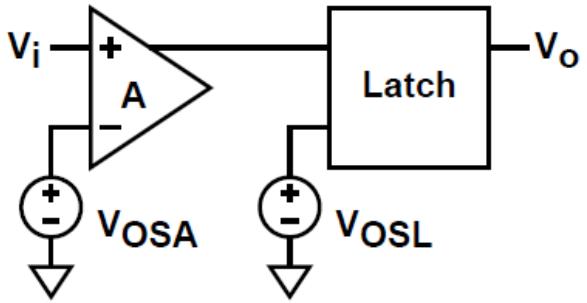
Comparator Typical Architecture

- The equivalent input offset is

$$V_{OS} = V_{OSA} + \frac{V_{OSL}}{A} \qquad \sigma^2(V_{OS}) = \sigma^2(V_{OSA}) + \frac{\sigma^2(V_{OSL})}{A^2}$$

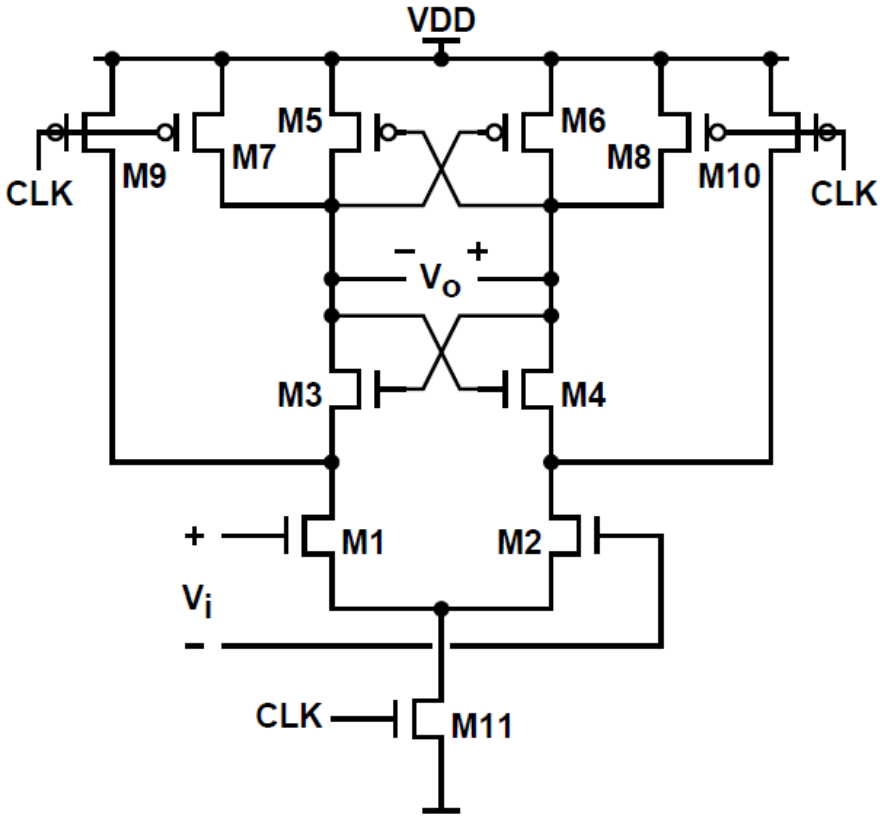
- The preamplifier provides:
  - Input common-mode rejection
  - Kick-back noise reduction





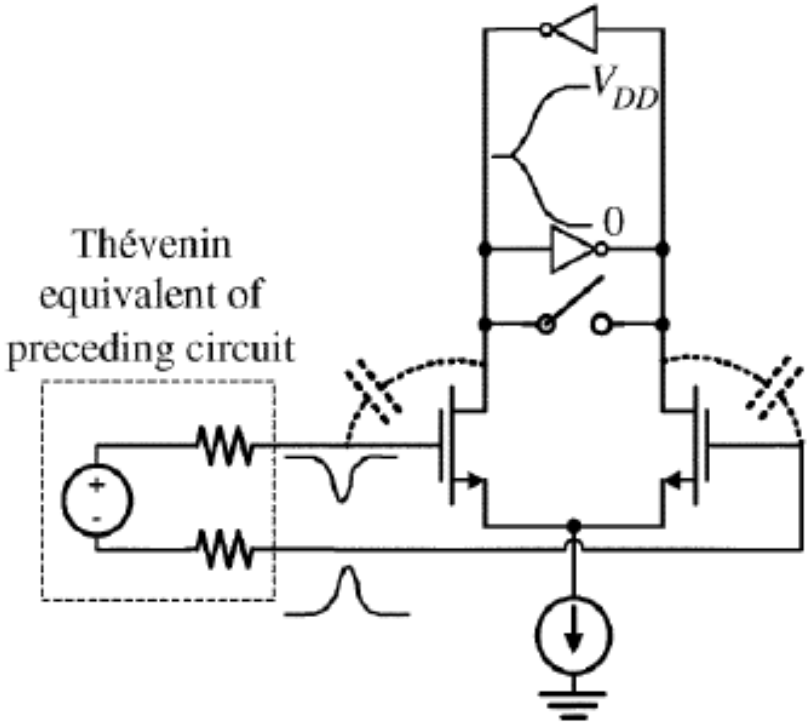
Regenerative Latch

- When CLK=0, latch is disable and no power dissipation.
- When CLK=1
  - The M1-M2 pair is activated first
  - The M3-M4 pair is then activated
  - The M5-M6 pair is last activated.



Kickback-Noise

- After comparison, one of the comparator output would force to ground and the other to supply voltage
- The comparator inputs coupled with different voltage resulting a equivalent noise source.
- The coupled value is corresponding to the ratio of parasitic capacitance of comparator input device and the loading capacitance of comparator input



Comparator Trade-Off

- For a MOS pair, mismatch and input-referred offset are modeled as

$$\sigma^2(V_{OS}) = \frac{1}{W \times L}\left(A_{V_t}^2 + \frac{V_{OV}^2}{4} \times A_\beta^2\right)$$

- For a comparator

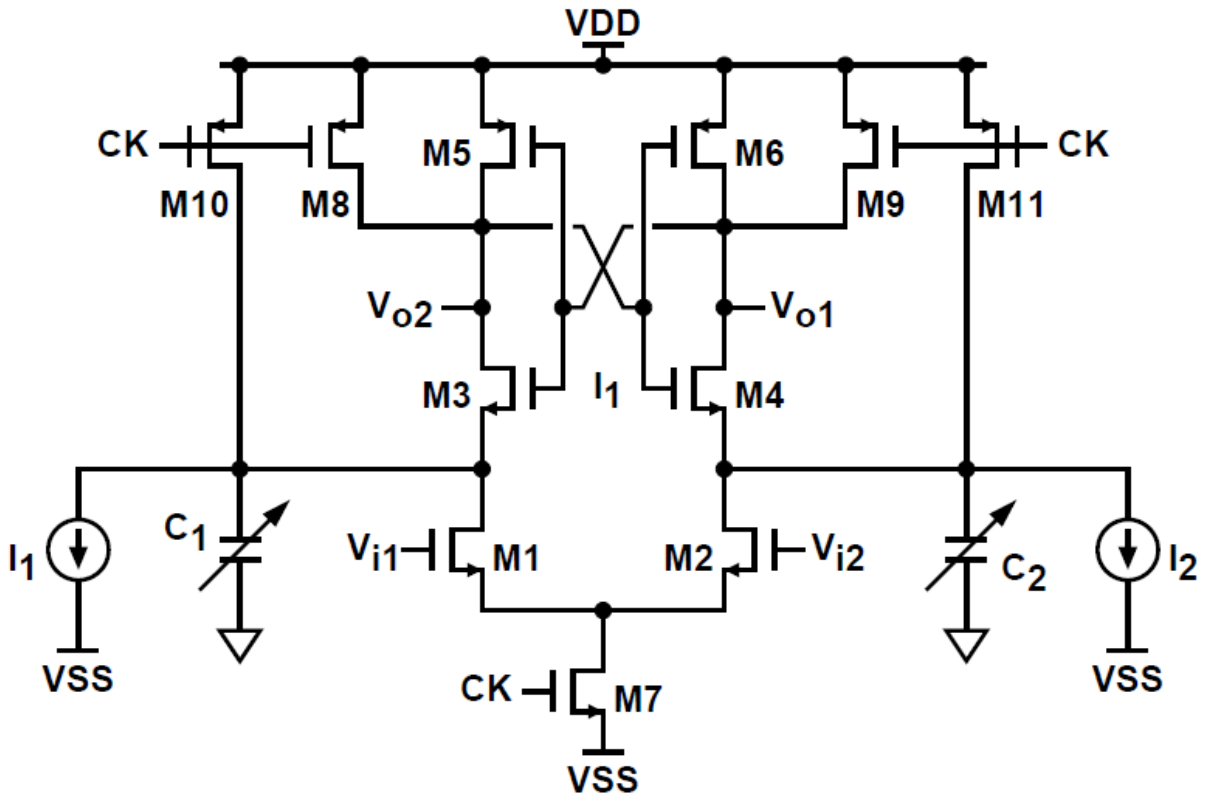
$$Speed \propto \frac{g_m}{C} \approx \frac{2I / V_{OV}}{(2/3) \cdot WL \cdot C_{OX}} \qquad \frac{1}{Accuracy^2} \propto \frac{\sigma^2(V_{OS})}{V_{DD}^2} \approx \frac{A_{V_t}^2 + \frac{V_{OV}^2}{4} \times A_\beta^2}{WL \times V_{DD}^2}$$

$$Power \propto I \cdot V_{DD} \Rightarrow \frac{Speed \times Accuracy^2}{Power} \alpha \frac{1}{C_{OX} \cdot \left(A_{V_t}^2 + \frac{V_{OV}^2}{4} \times A_\beta^2\right)} \times \frac{V_{DD}}{V_{OV}}$$

K. Uyttenhove and M. Steyaert, “Speed-power-accuracy tradeoff in high-speed CMOS ADCs,” TCAS-II, 2002/4, pp. 280–286.

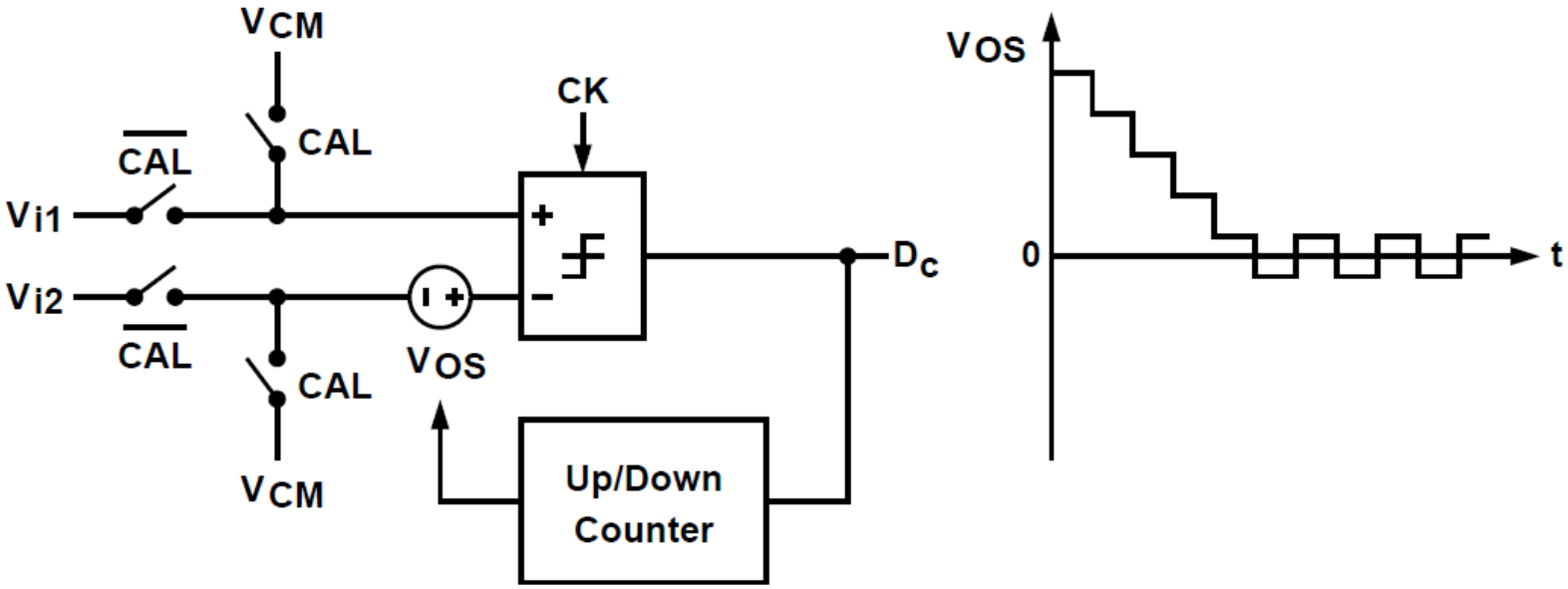
Variable-Offset Regenerative Latch

- Comparator offset is adjusted by varying C_1 and C_2, or I_1 and I_2.



Comparator offset Calibration

- During Calibration, $V_i = V_{i1} - V_{i2} = 0$.



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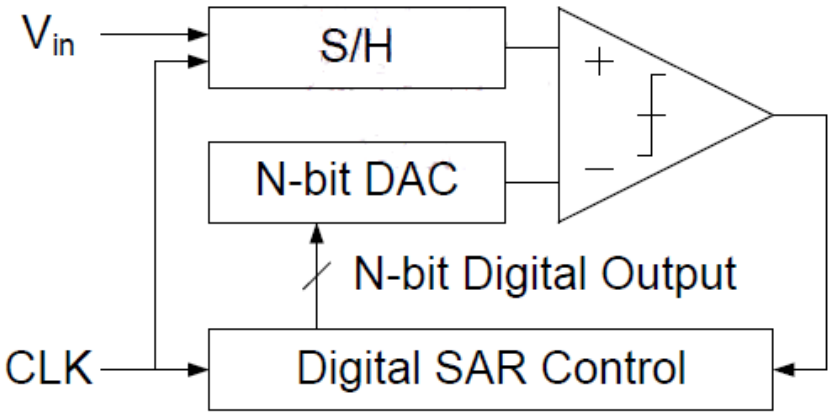
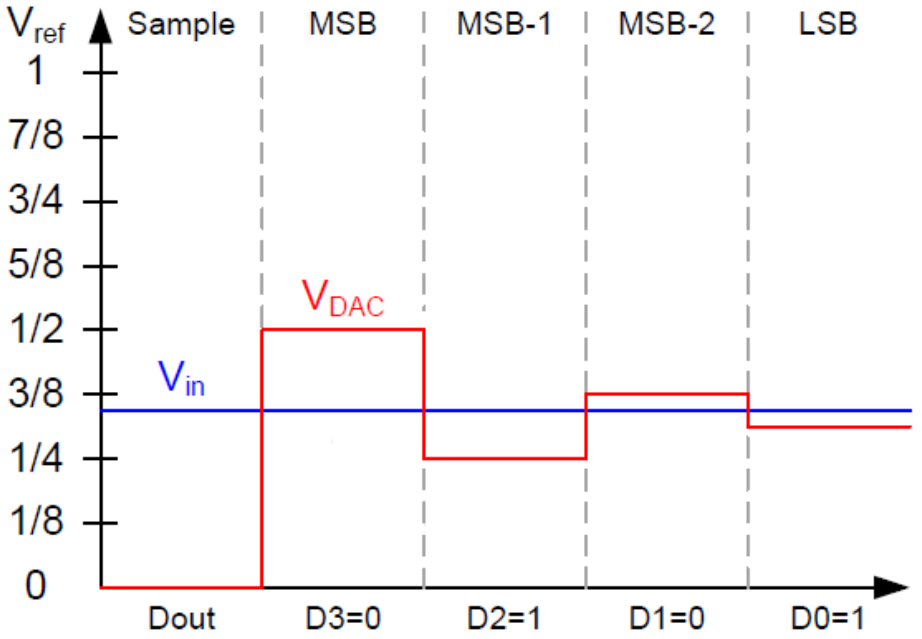
SAR ADC Architecture

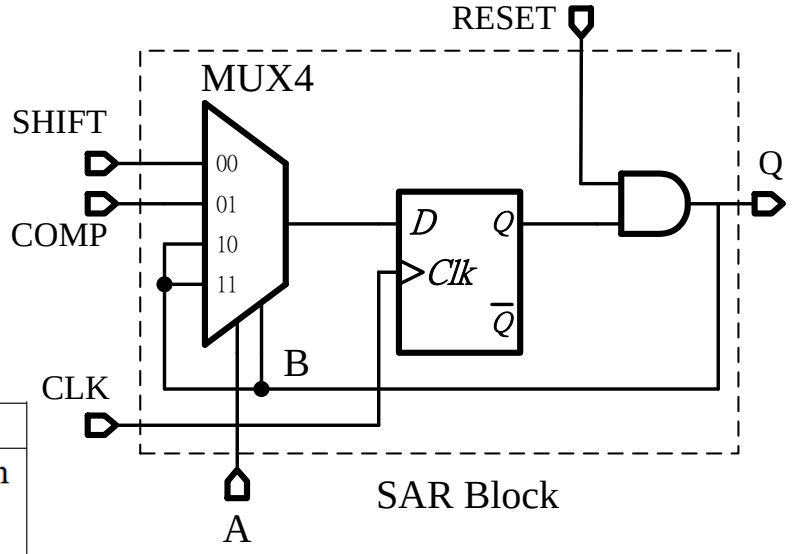
- The SAR ADC is composed of a sample and hold (S/H), DAC, comparator and digital SAR control logic.
- N comparisons per conversion
- DAC voltage is converged to input voltage by SAR Control, which is determined by comparison results



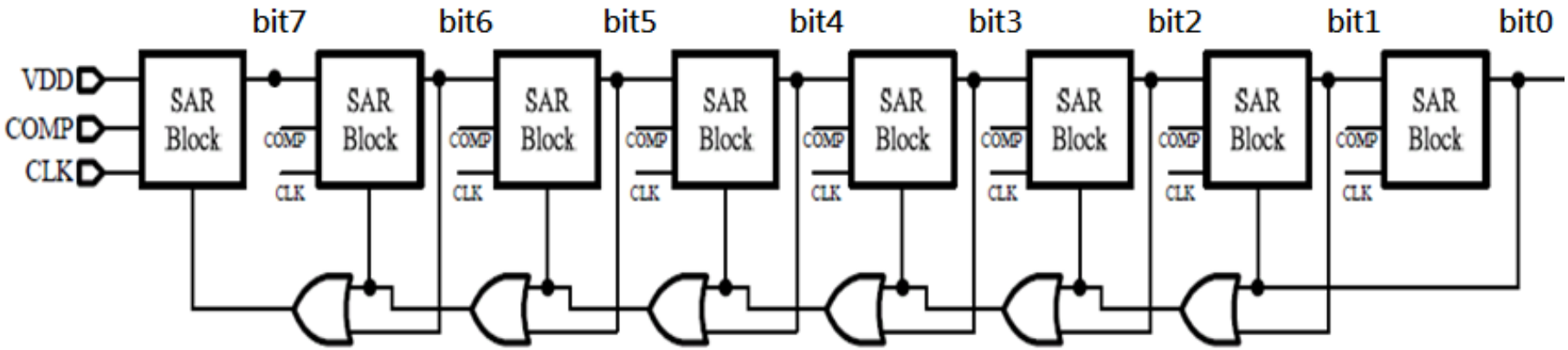


Traditional SAR Logic

- The function of SAR is determined by the value of each bit in a sequential manner, based on the output of comparator.
- Minimized the amount of DFF.



A	B	
1	-	Memorization
0	1	Data load
0	0	Shift right



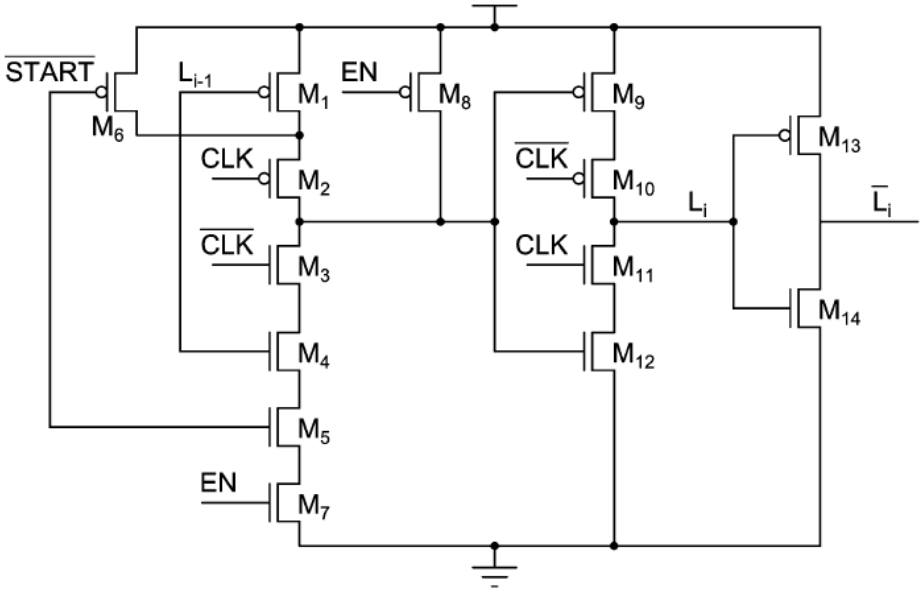
FSM of SAR Logic

Conversion step	Input D/A word								Comparator output
0	1	0	0	0	0	0	0	0	a7
1	a7	1	0	0	0	0	0	0	a6
2	a7	a6	1	0	0	0	0	0	a5
3	a7	a6	a5	1	0	0	0	0	a4
4	a7	a6	a5	a4	1	0	0	0	a3
5	a7	a6	a5	a4	a3	1	0	0	a2
6	a7	a6	a5	a4	a3	a2	1	0	a1
7	a7	a6	a5	a4	a3	a2	a1	1	a0
result	a7	a6	a5	a4	a3	a2	a1	a0	-

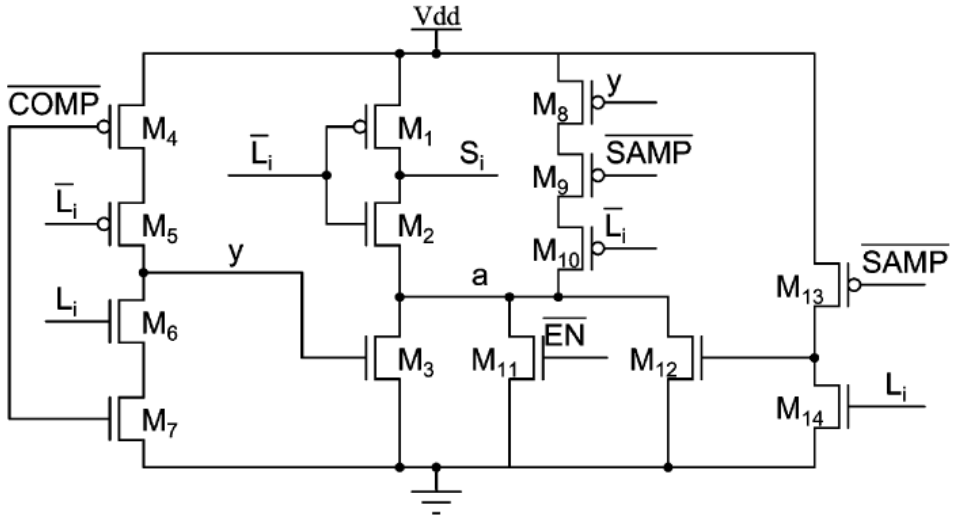
Rossi, A., "Nonredundant successive approximation register for A/D converters," *Electronics Letters* , no.12, pp.1055,1057, 6 Jun 1996

Full Custom Register Logics

Resettable shift register



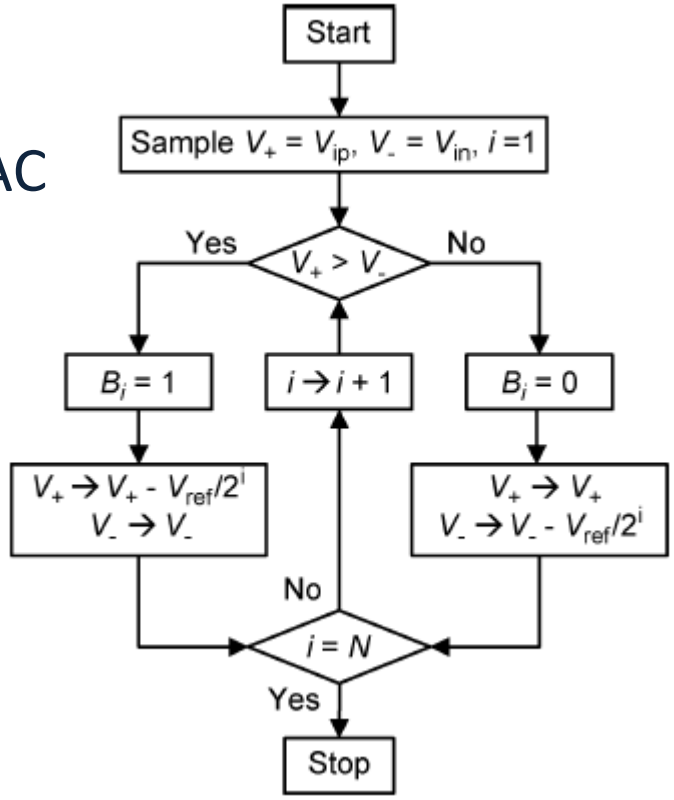
Switch drive register



B.P. Ginsburg, A.P. Chandrakasan, "Dual Time-Interleaved Successive Approximation Register ADCs for an Ultra-Wideband Receiver," *JSSC* , vol.42, no.2, pp.247,257, Feb. 2007.

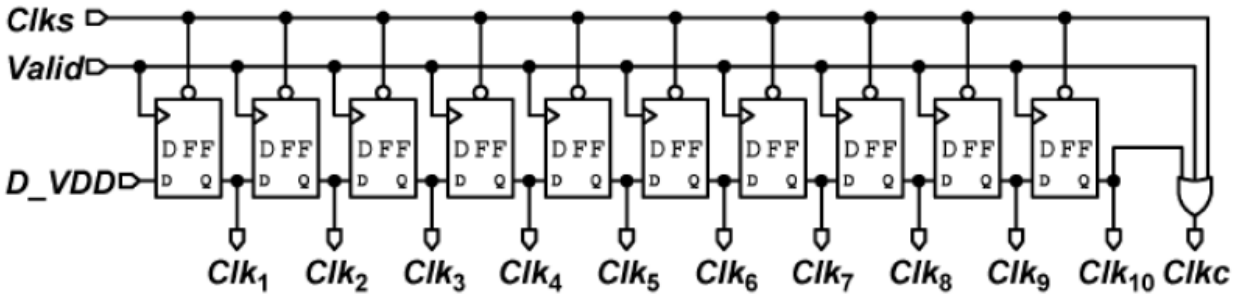
SAR ADC Flow Chart

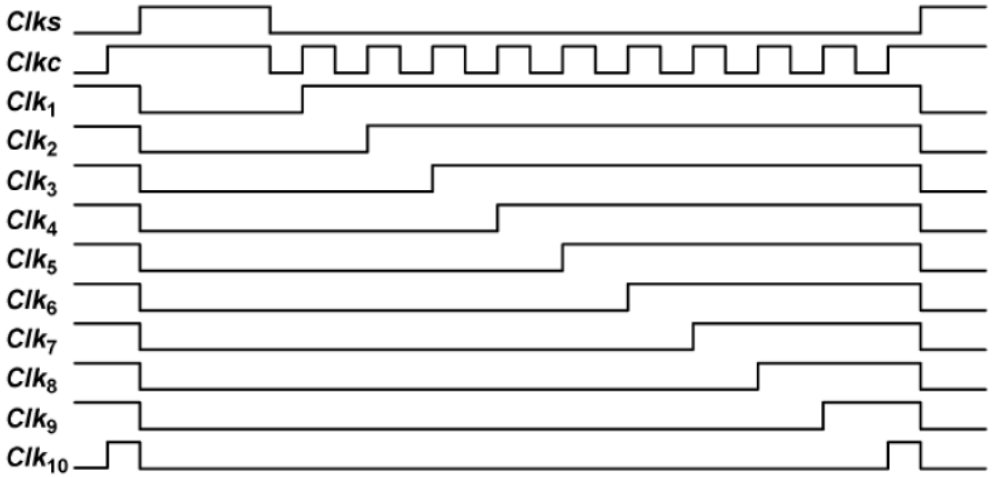
- First, SAR ADC samples input signal on DAC by the S/H.
- Next, after the S/H is turn-off, the comparator directly performs the first comparison.
- According to the comparator output, the digital output B_1 is determined and the DAC voltage is switched to converged.
- The ADC repeats the procedure until the MSB to LSB is decided.



Asynchronous SAR Logic

- To avoid using a high-frequency clock generator, the asynchronous control circuit uses to internally generate necessary clock signals.





CLK_s : sampling clock

CLK_c : control signal of comp.

Valid : NAND of comp. outputs

CLK_i : CLK to store comp. output & control SAR