CHAPTER 8

Analog to Digital Converter

Outline

- 8.1 Introduction
- 8.2 Nyquist Rate ADC
- 8.3 SAR ADC
- 8.4 Integrating ADC
- 8.5 Algorithmic ADC
- 8.6 Pipelined ADC
- 8.7 Subranging ADC

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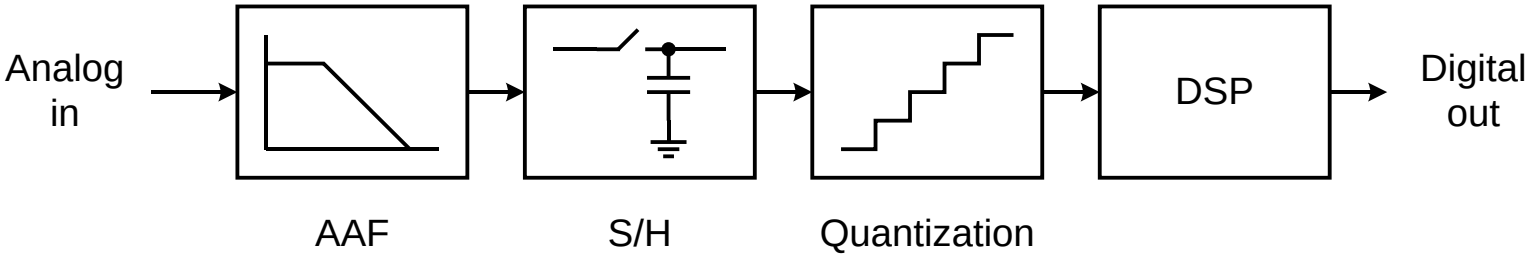
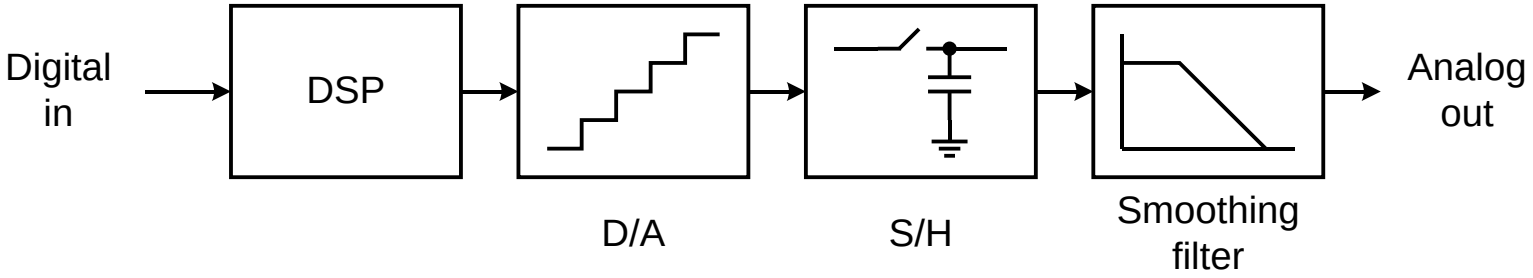
A/D and D/A Conversion

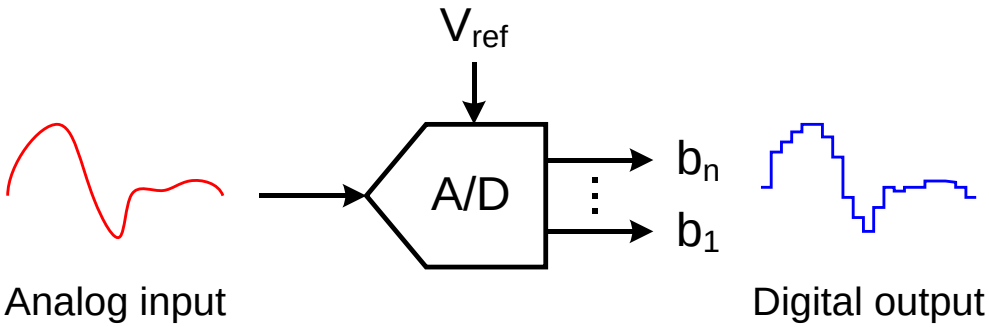
A/D Conversion



D/A Conversion



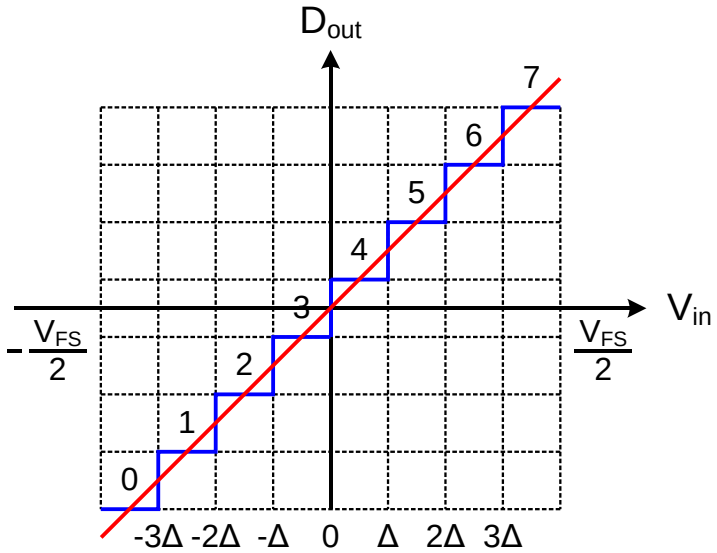
Quantization



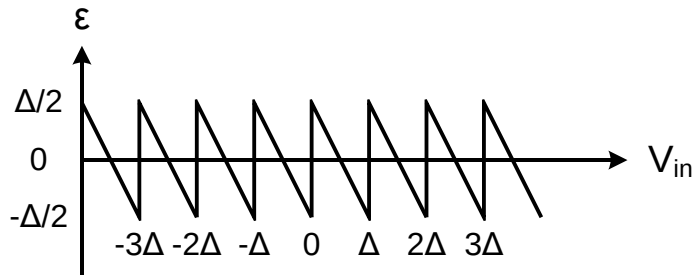
$$\underline{\text{Division}}: \quad D_{out} = \left\lfloor 2^N \cdot \frac{V_{in}}{V_{FS}} \right\rfloor$$

- Quantization = division + normalization + truncation
- Full-scale range (V_{FS}) is determined by V_{ref}

Quantization Error



N = 3



$$\Delta = \frac{V_{FS}}{2^N} = LSB$$

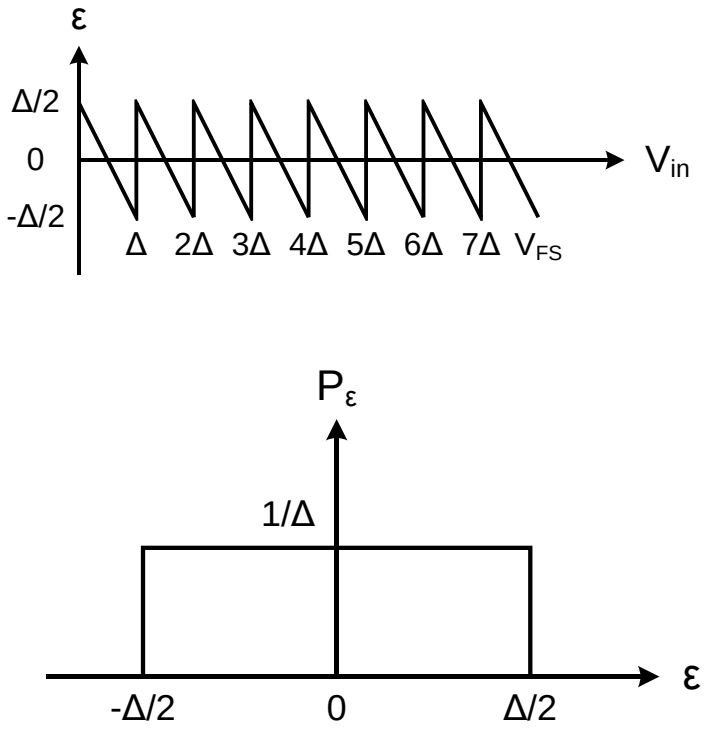
$$V_{in} \in [0, V_{FS}]$$

$$\varepsilon = D_{out}\Delta - V_{in} = D_{out}\left(\frac{V_{FS}}{2^N}\right) - V_{in}$$

$$-\frac{\Delta}{2} \le \varepsilon \le \frac{\Delta}{2}$$

"Random" quantization error is usually regarded as noise

Quantization Noise



Assumptions:

- N is large
- $0 \le V_{in} \le V_{FS}$ and $V_{in} >> \Delta$
- V_{in} is active
- ε is Uniformly distributed
- Spectrum of ε is white

$$\sigma_\varepsilon^2 = \int_{-\Delta/2}^{\Delta/2} \varepsilon^2 \cdot \frac{1}{\Delta} \cdot d\varepsilon = \frac{\Delta^2}{12}$$

Ref: W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446-472, July 1948.

Signal-to-Quantization Noise Ratio

Assume V_{in} is sinusoidal with $V_{p\text{-}p} = V_{FS}$,

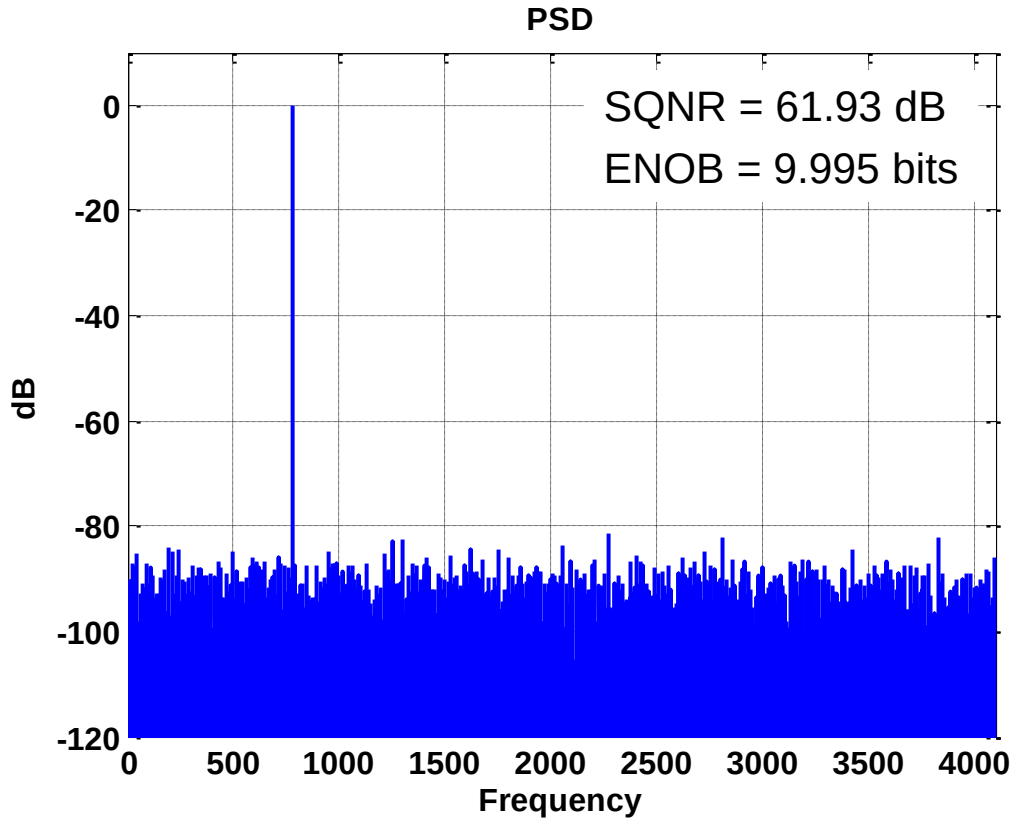
$$SQNR = \frac{V_{FS}^2/8}{\sigma_\varepsilon^2} = \frac{(2^N\Delta)^2/8}{\frac{\Delta^2}{12}} = 1.5\times 2^{2N},$$

N (bits)	SQNR (dB)
8	49.9
10	62.0
12	74.0
14	86.0

$$SQNR = 6.02\times N + 1.76\ dB$$

- SQNR depicts the theoretical performance of an ideal ADC
- In reality, ADC performance is limited by many other factors:
  - Electronic noise (thermal, 1/f, coupling/substrate, etc.)
  - Distortion (measured by THD, SFDR, IM3, etc.)

FFT Spectrum of Quantized Signal

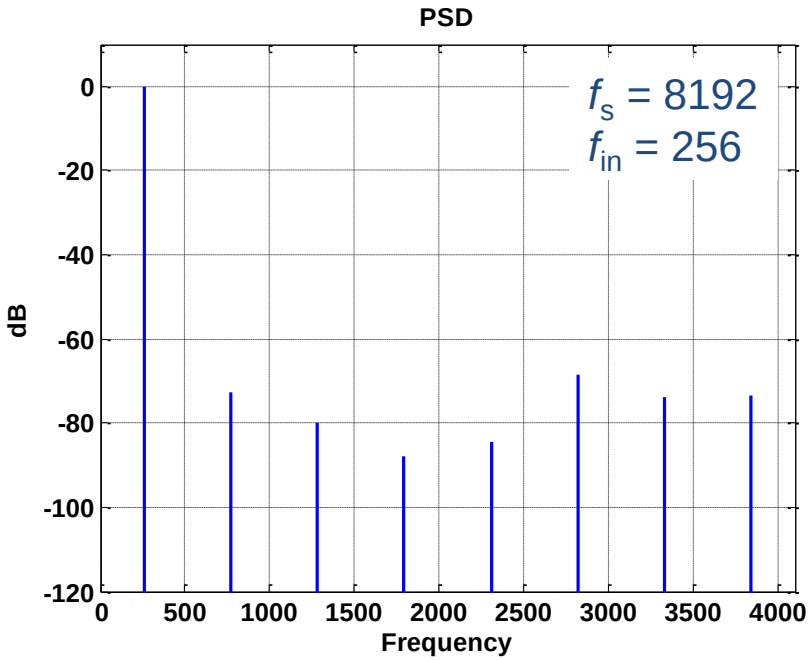


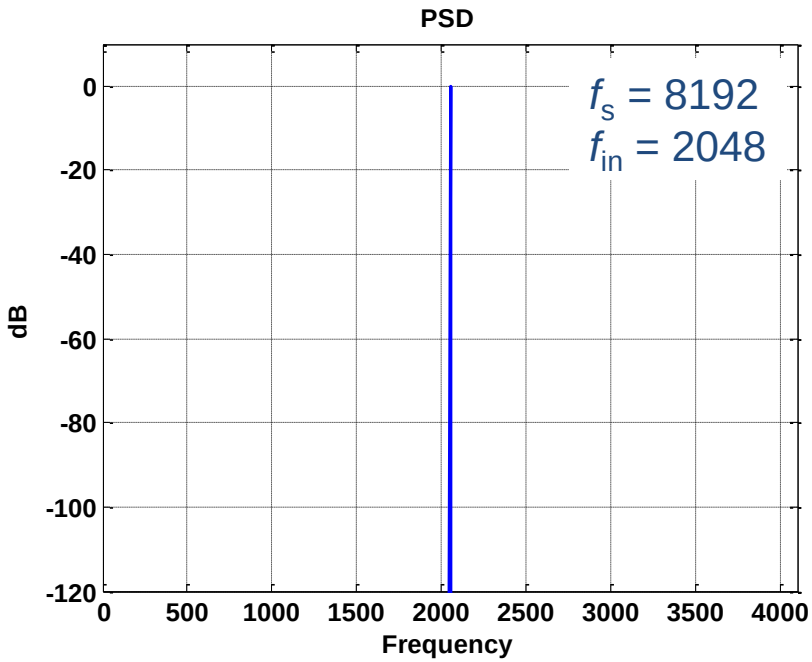
- N = 10 bits
- 8192 samples, only $f = [0, f_s/2]$ shown
- Normalized to V_{in}
- $f_s = 8192$, $f_{in} = 779$
- f_{in} and f_s must be incommensurate

$$\text{ENOB} = \frac{\text{SQNR} - 1.76\,\text{dB}}{6.02\,\text{dB}}$$

Ref: W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446-472, July 1948.

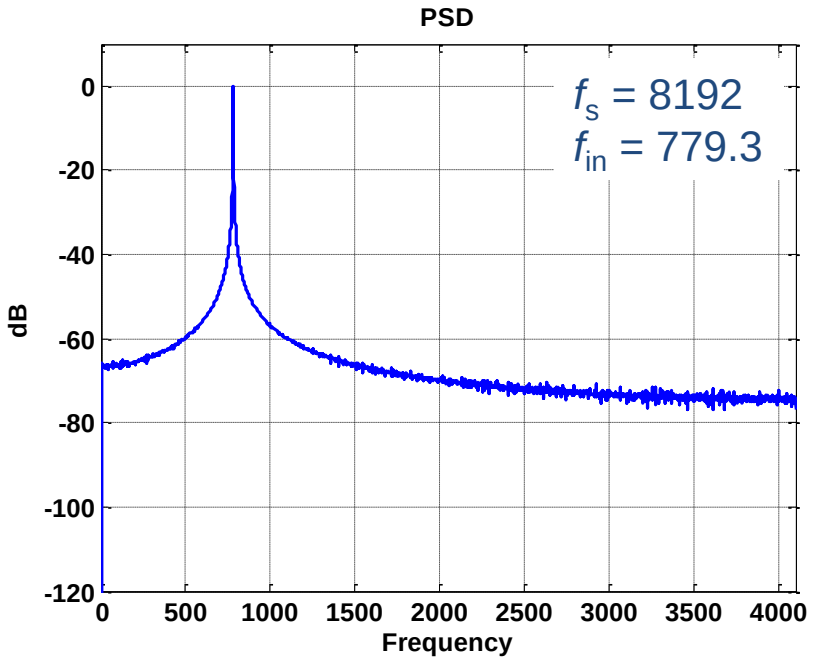
Commensurate f_s and f_{in}

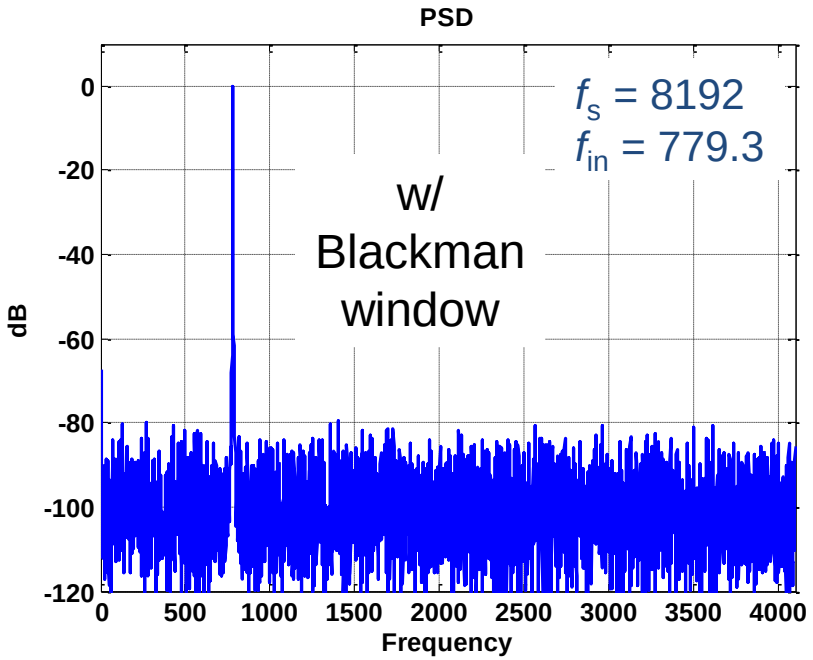




- Periodic sampling points result in periodic quantization errors
- Periodic quantization errors result in harmonic distortion

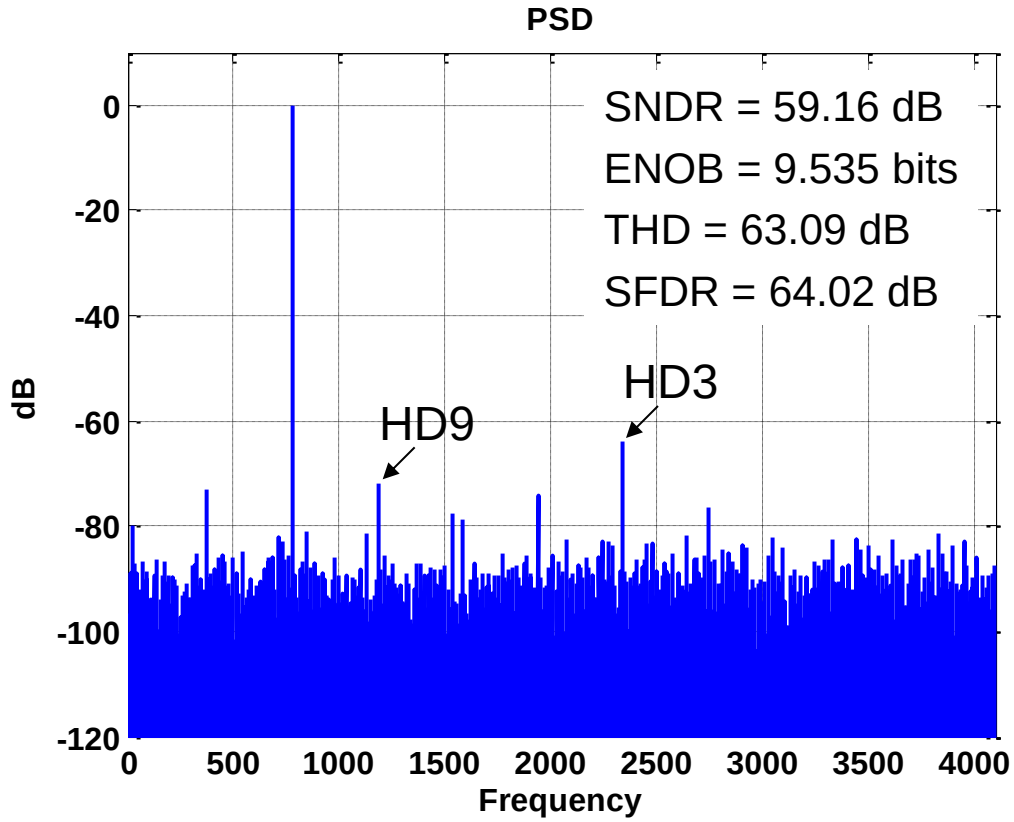
Spectrum Leakage





- TD samples must include integer number of cycles of input signal
- Windowing can be applied to eliminate spectrum leakage
- Trade-off b/t main-lobe width and sideband rejection for different windows

FFT Spectrum with Distortion

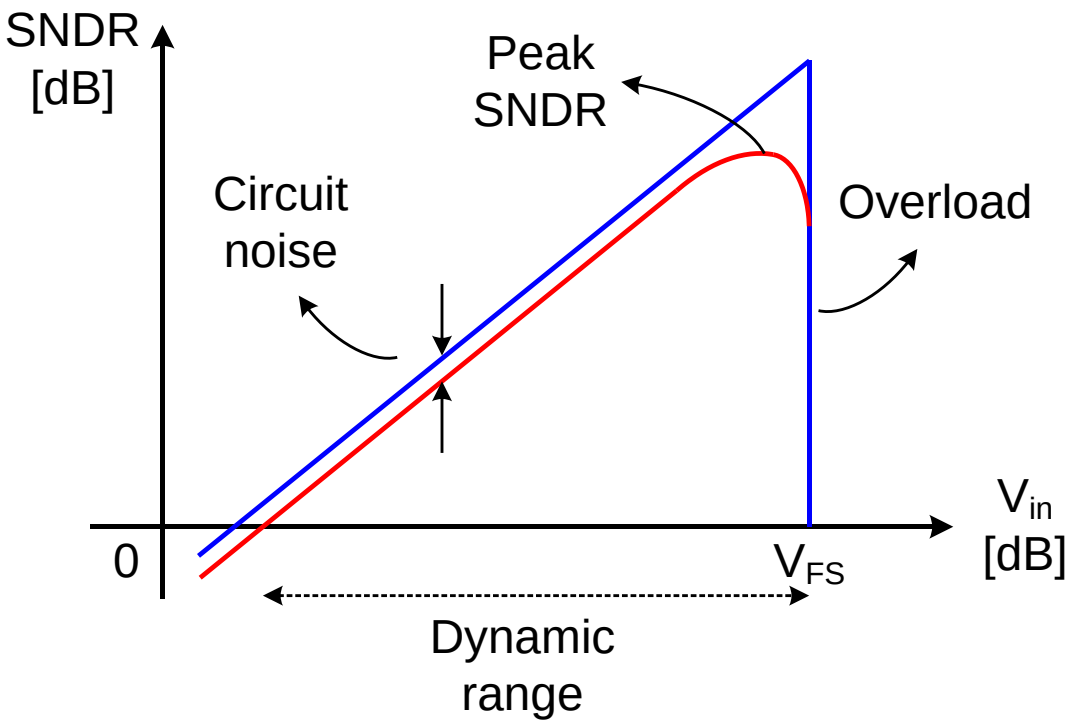


- Signal-to-noise plus distortion ratio (SNDR a.k.a. SINAD)
- Total harmonic distortion (THD)
- Spurious-free dynamic range (SFDR)

$$\text{ENOB} = \frac{\text{SNDR} - 1.76\,\text{dB}}{6.02\,\text{dB}}$$

- High-order harmonics are aliased back, visible in $[0, f_s/2]$ band
- E.g., HD3 @ 779x3+1=2338, HD9 @ 8192-9x779+1=1182

Dynamic Performance



$$\text{SNR} = 10\text{LOG}_{10}\left(\frac{V_{in}^{2}/2}{\Delta^{2}/12+\sigma_{N}^{2}}\right) \propto V_{in}[\text{dB}]$$

- Peak SNDR limited by large-signal distortion of the converter
- Dynamic range implies the “theoretical” SNR of the converter

Dynamic Performance Metrics

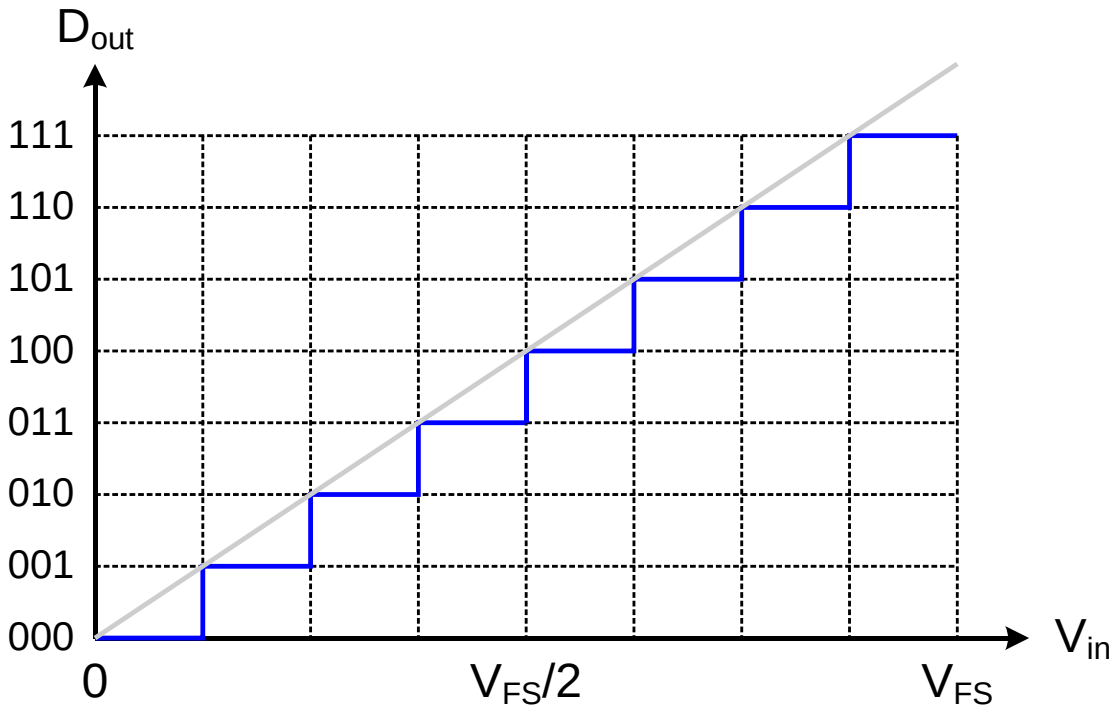
- Signal-to-noise ratio (SNR)
- Total harmonic distortion (THD)
- Signal-to-noise and distortion ratio (SNDR or SINAD)
- Spurious-free dynamic range (SFDR)
- Two-tone intermodulation product (IM3)
- Aperture uncertainty (related to the frontend S/H and clock)

- Dynamic range (DR) – misleading (avoid it if possible!)
- Idle channel noise or pattern noise in oversampled converters

Static Performance Metrics

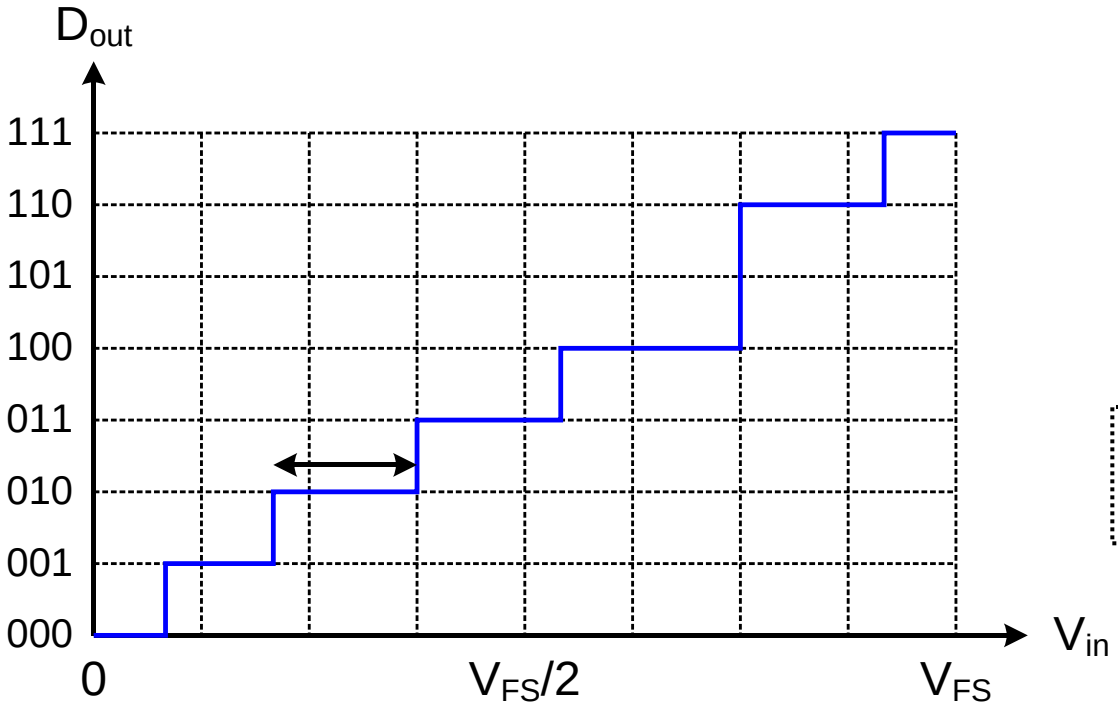
- Offset (OS)
- Gain error (GE)
- Monotonicity
- Linearity
  - Differential nonlinearity (DNL)
  - Integral nonlinearity (INL)

Ideal ADC Transfer Characteristic



Note the systematic offset! (floor, ceiling, and round)

DNL and Missing Code

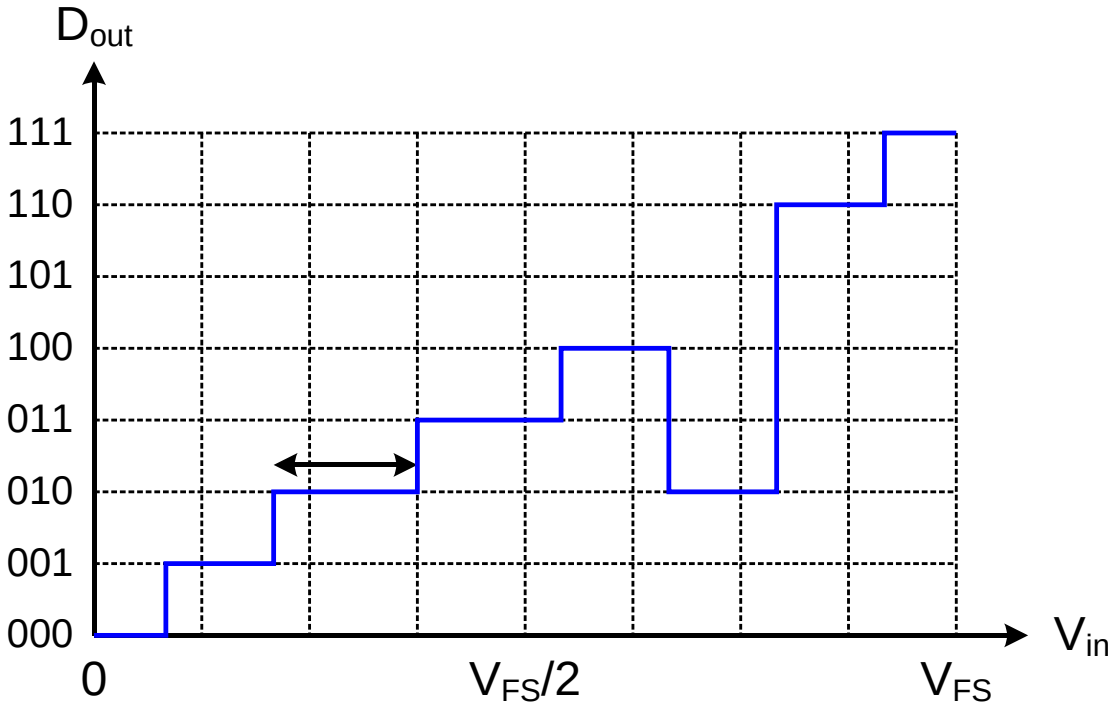


- DNL = ?
- Can DNL < -1?

$$DNL_i = \frac{i^{th}\ \text{Step Size} - \Delta}{\Delta}$$

DNL = deviation of an input step width from 1 LSB (= $V_{FS}/2^N = \Delta$)

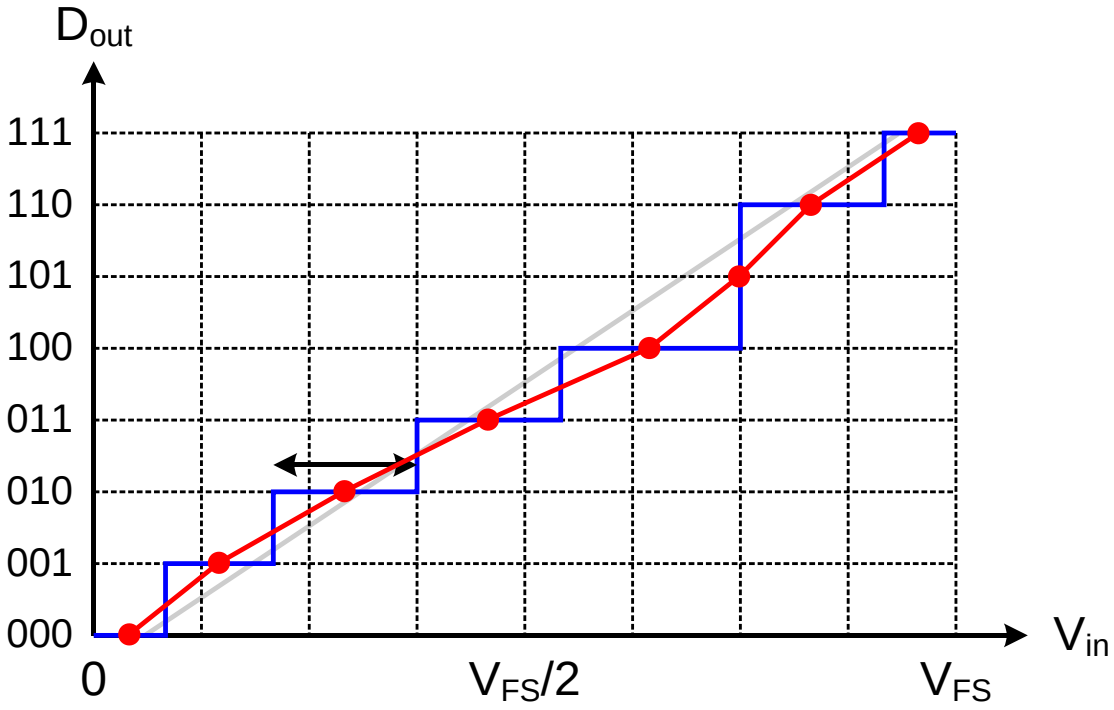
DNL and Nonmonotonicity



- DNL = ?
- How can we even measure this?

DNL = deviation of an input step width from 1 LSB (= $V_{FS}/2^N = \Delta$)

INL



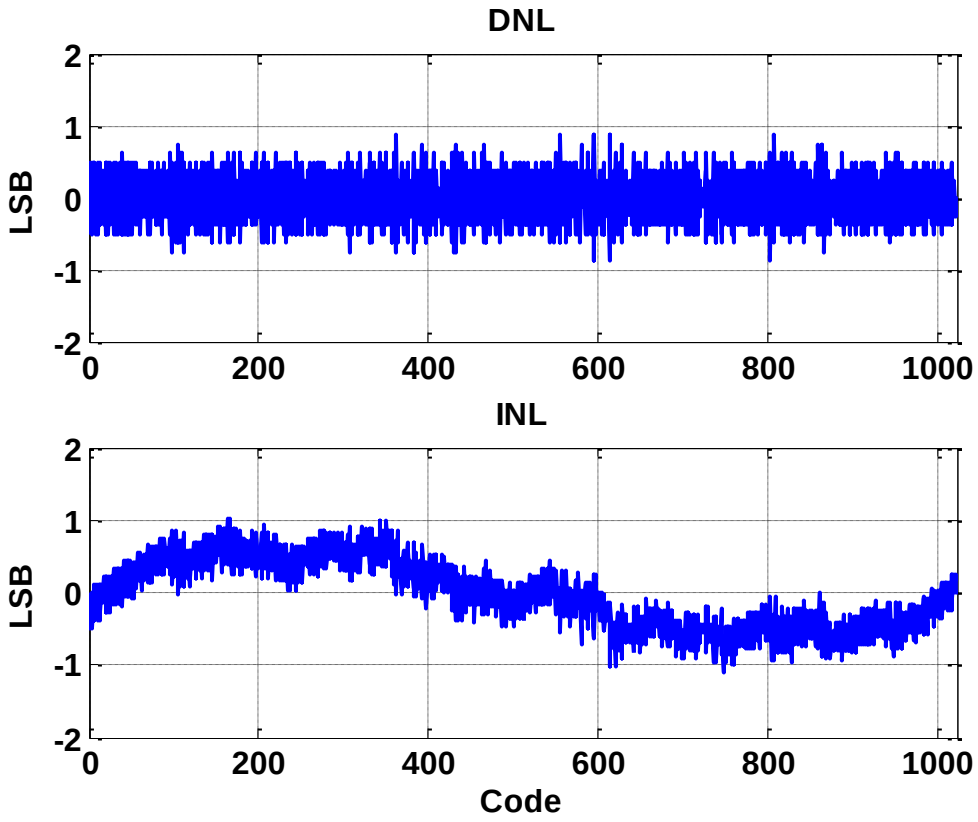
Any code

- Missing?
- Nonmonotonic?

INL = deviation of the step midpoint from the ideal step midpoint

(method I and II …)

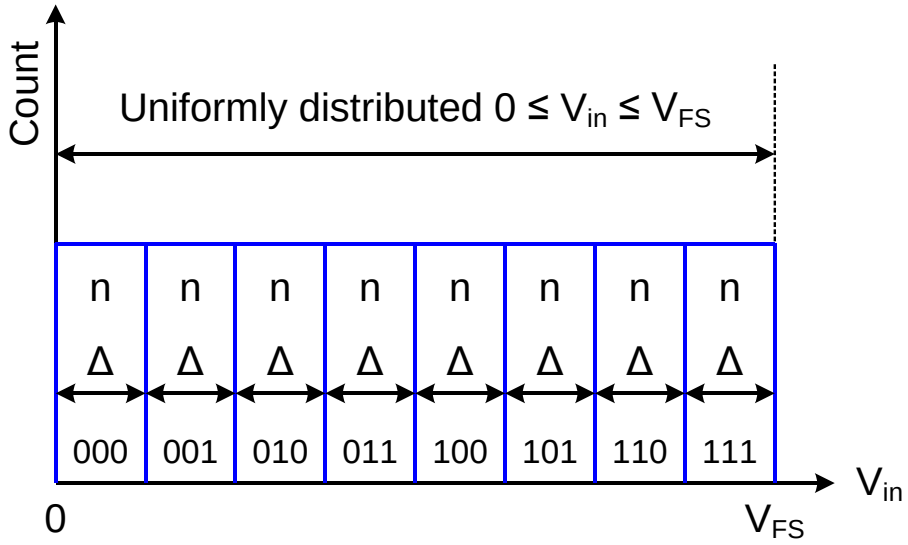
10-bit ADC Example

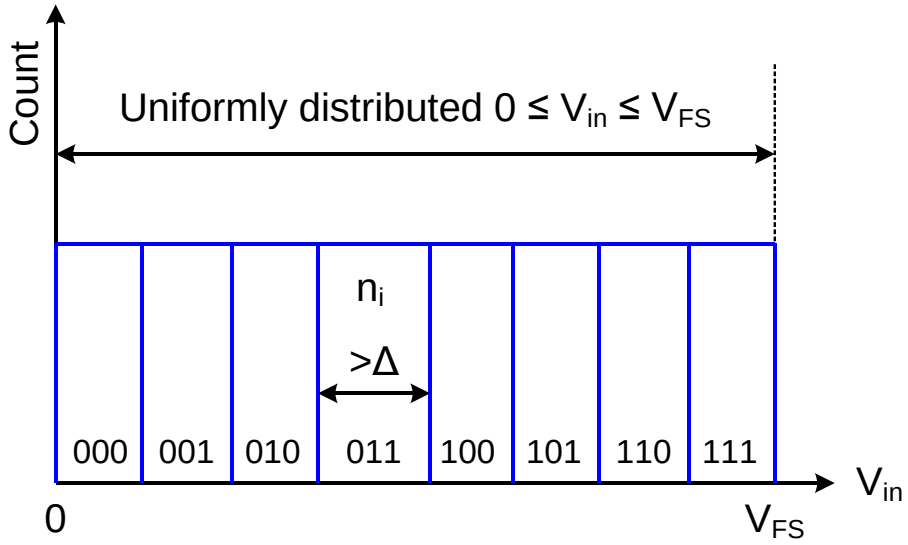


- 1024 codes
- No missing code!
- Plotted against the digital code, not V_{in}
- Code density test (CDT)

DNL must always be greater or equal to -1 LSB!

Code Density Test

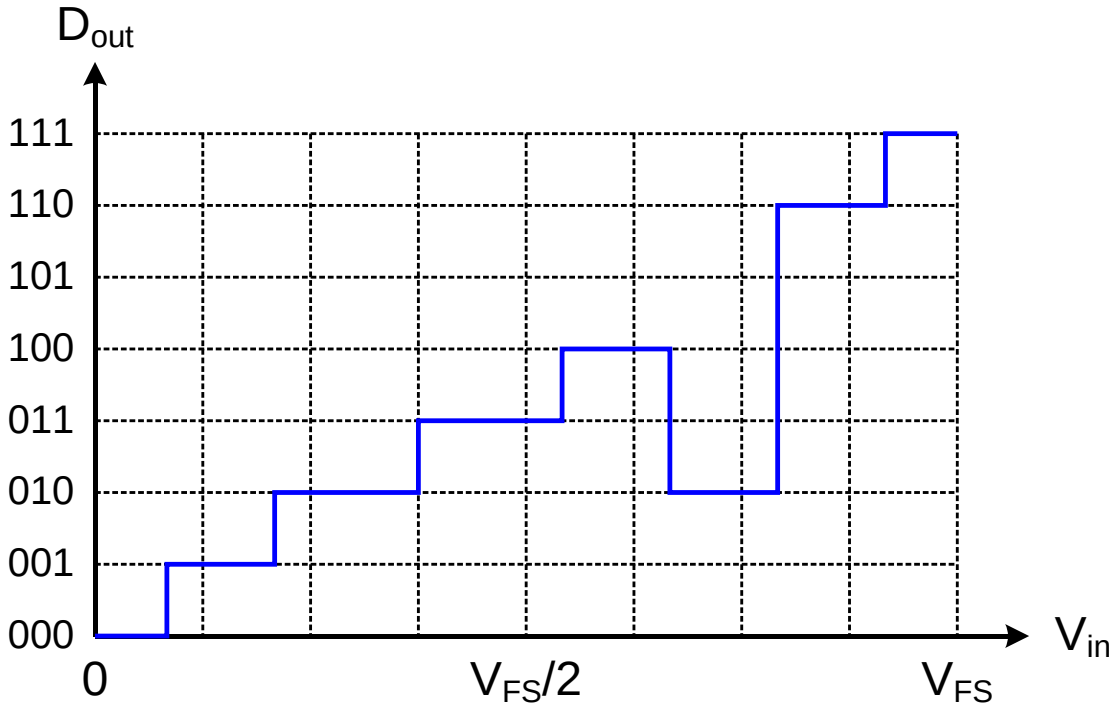




$$DNL_i = \frac{i^{th}\ \text{Step Size} - \Delta}{\Delta} \approx \frac{n_i - \langle n_i \rangle}{\langle n_i \rangle}$$

Ball casting problem: # of balls collected by each bin (n_i) is proportional to the bin size (converter step size)

CDT and Nonmonotonicity



- Two transition steps for one code?! How to plot INL/DNL?
- CDT can be misleading in determining the static nonlinearity

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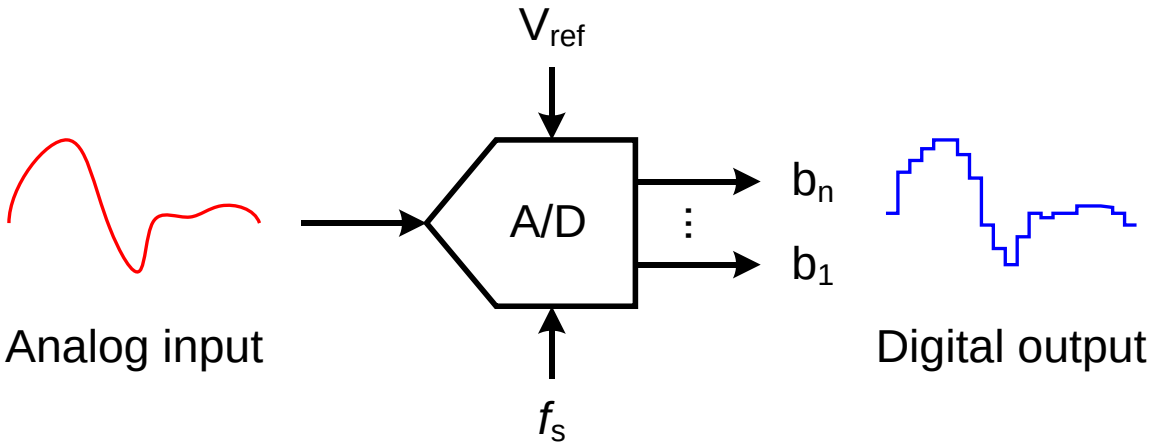
Nyquist-Rate ADC

- Digitizes input signal up to Nyquist frequency ($f_N=f_s/2$)
- Minimum sample rate (f_s) for a given input bandwidth
- Each sample is digitized to the maximum resolution of converter
- Often referred to as the “black box” version of digitization



Nyquist-Rate ADC (N-Bit, Binary)

- Word-at-a-time (1 step)† ← fast
  - Flash
- Level-at-a-time (2^N steps) ← slowest
  - Integrating (Serial)
- Bit-at-a-time (N steps) ← slow
  - Successive approximation
  - Algorithmic (Cyclic)
- Partial word-at-a-time ($1 < M \leq N$ steps) ← medium
  - Subranging
  - Pipeline
- Others ($1 \leq M \leq N$ step)
  - Folding ← relatively fast
  - Interleaving (of flash, pipeline, or SA) ← fastest

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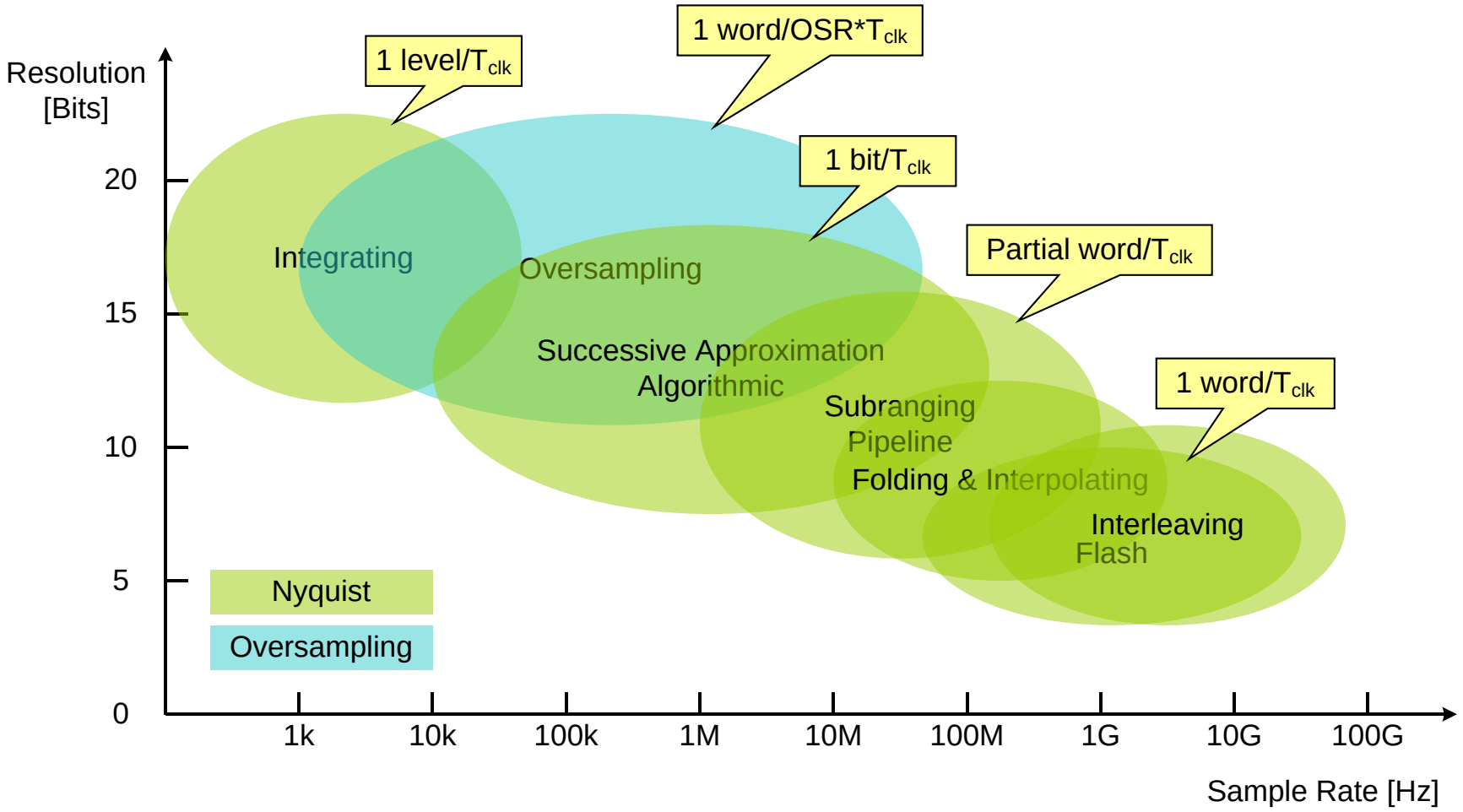
† the number in the parentheses is the "latency" of conversion, not "throughput"

Accuracy-Speed Tradeoff



Building Blocks for Data Converters

- Sample-and-Hold (Track-and-Hold) Amplifier
- Switched-Capacitor Amplifiers, Integrators, and Filters
- Operational Amplifier
- Comparators (Preamplifier and Latch)
- Voltage and Current DAC's
- Current Sources
- Voltage/Current/Bandgap References

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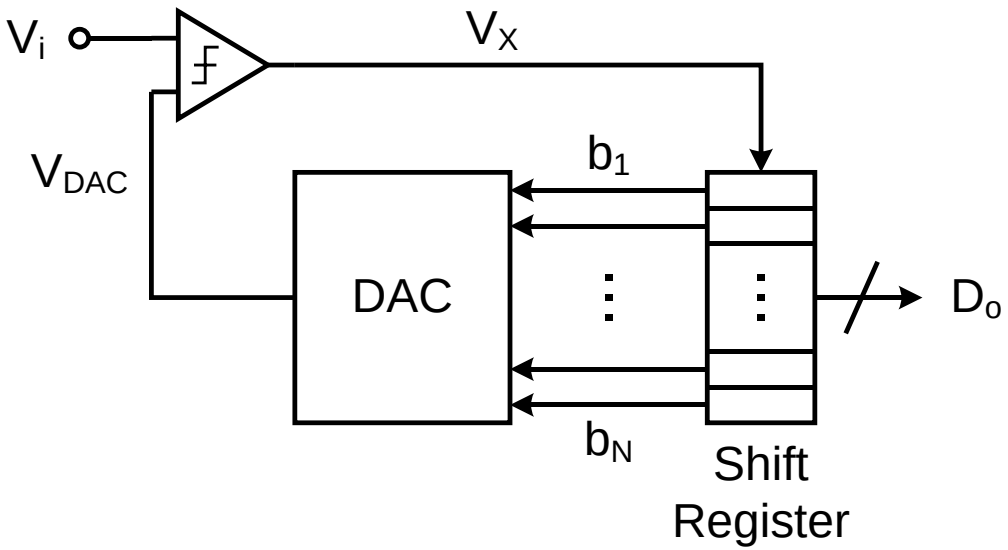
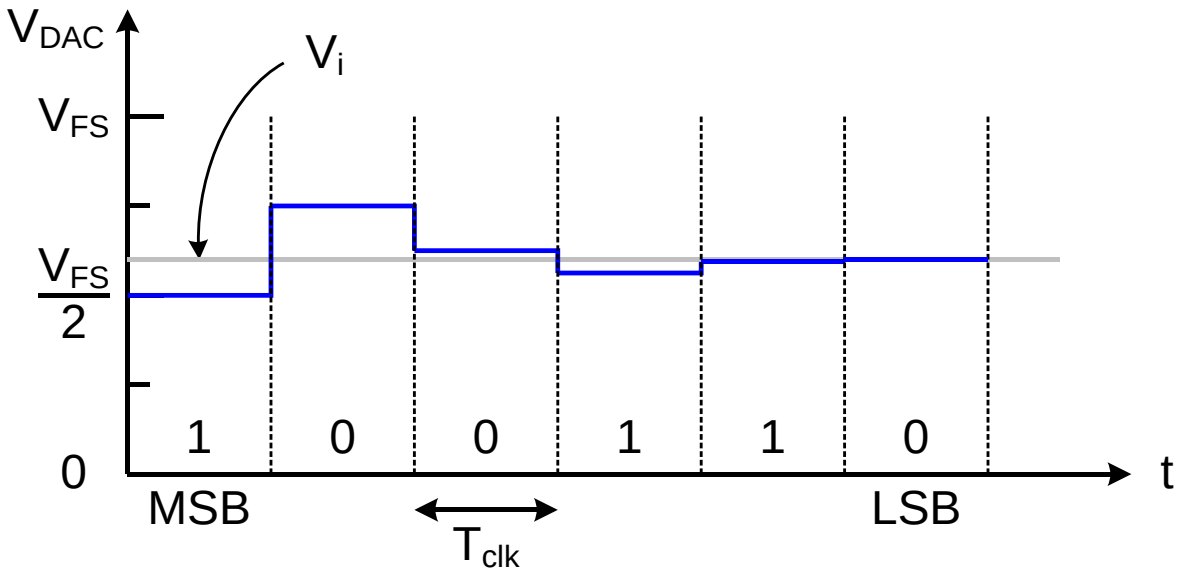
Successive Approximation ADC



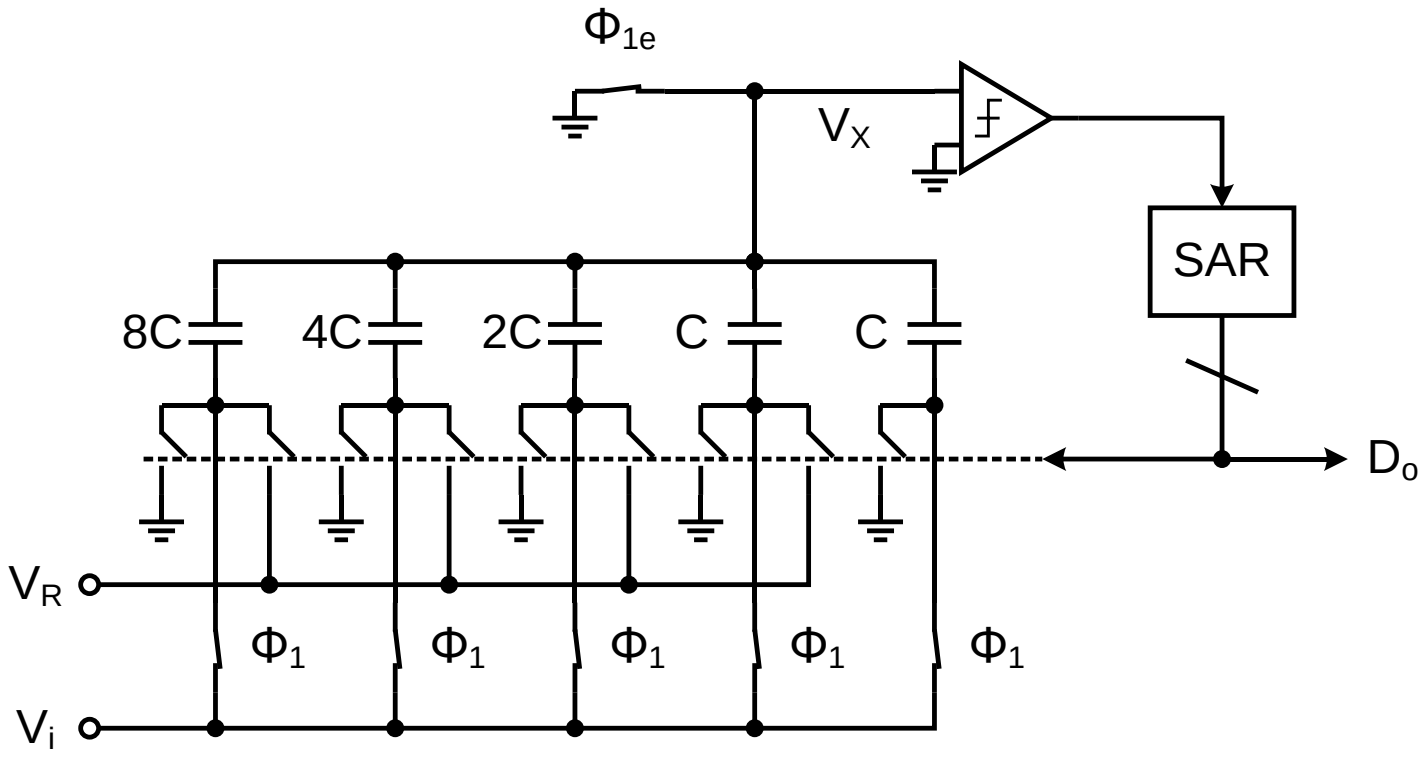
- Binary search algorithm → $N*T_{clk}$ to complete N bits
- Conversion speed is limited by comparator, DAC, and digital logic (successive approximation register or SAR)

Binary Search Algorithm



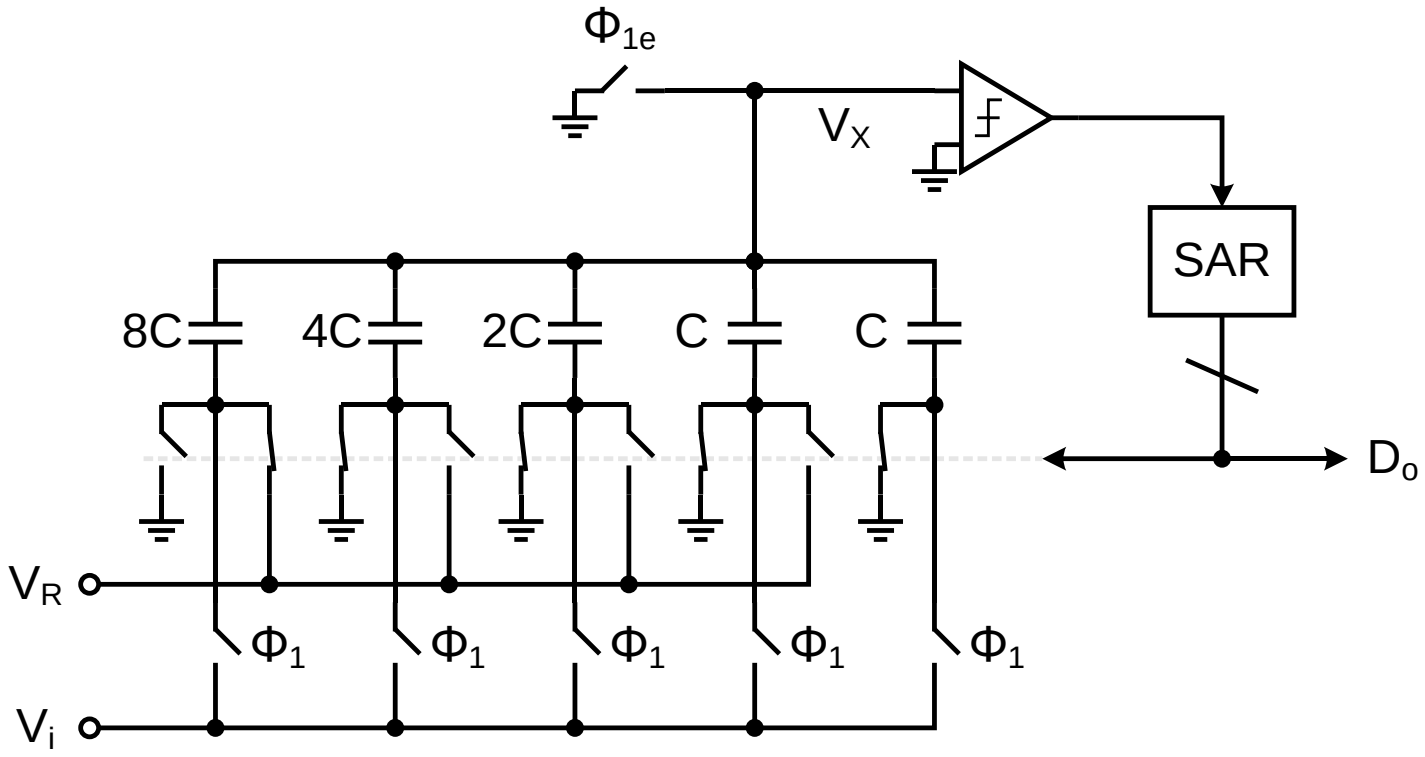
- DAC output gradually approaches the input voltage
- Comparator differential input gradually approaches zero

Charge Redistribution SA ADC



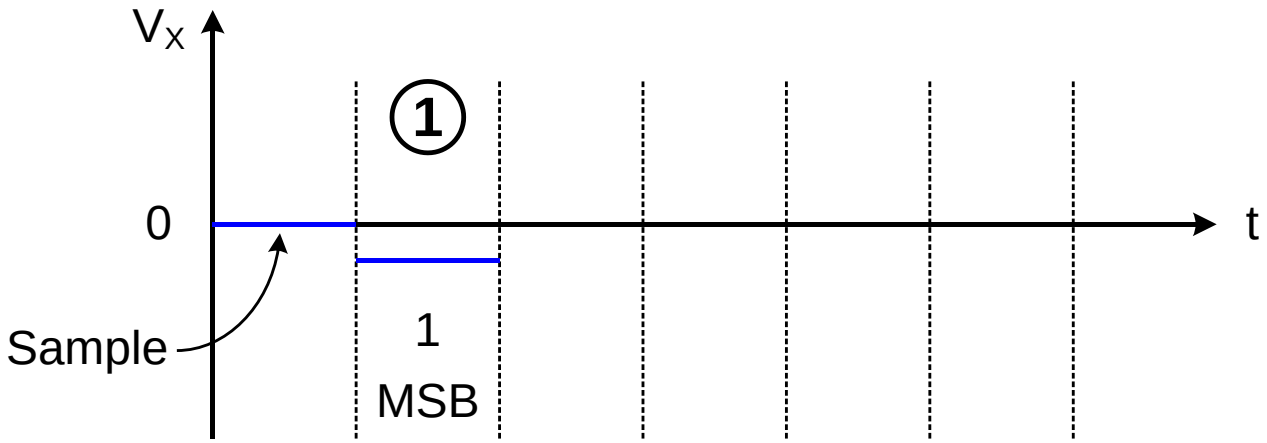
- 4-bit binary-weighted capacitor array DAC
- Capacitor array samples input when Φ_1 is asserted (bottom-plate)

Charge Redistribution (MSB)



$$V_i \cdot \sum_{j=0}^{4} C_j = (V_R - V_X) \cdot C_4 - V_X \cdot \sum_{j=0}^{3} C_j \Rightarrow V_X = \left(V_R \cdot C_4 - V_i \cdot \sum_{j=0}^{4} C_j \right) \Big/ \sum_{j=0}^{4} C_j = \frac{V_R}{2} - V_i$$

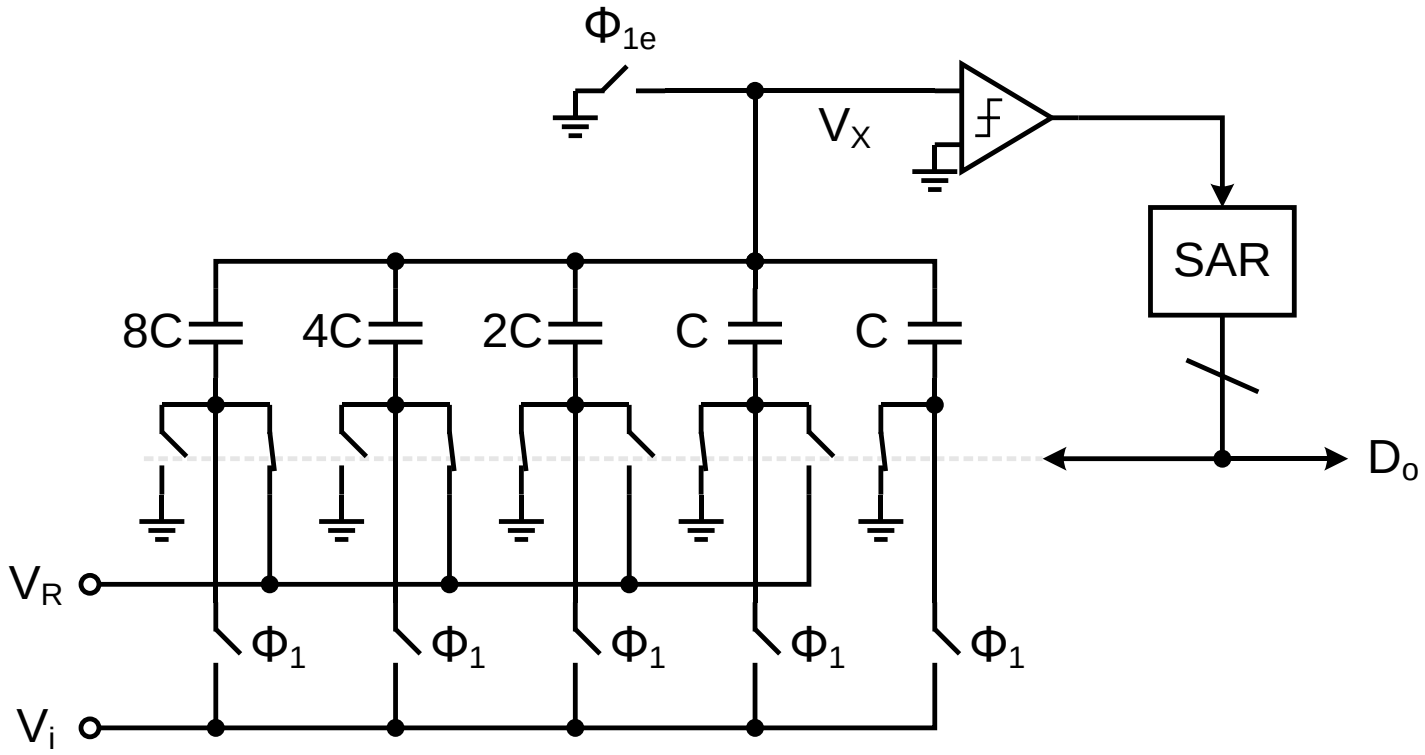
Comparison (MSB)



$$\text{MSB TEST}: V_X = \frac{V_R}{2} - V_i$$

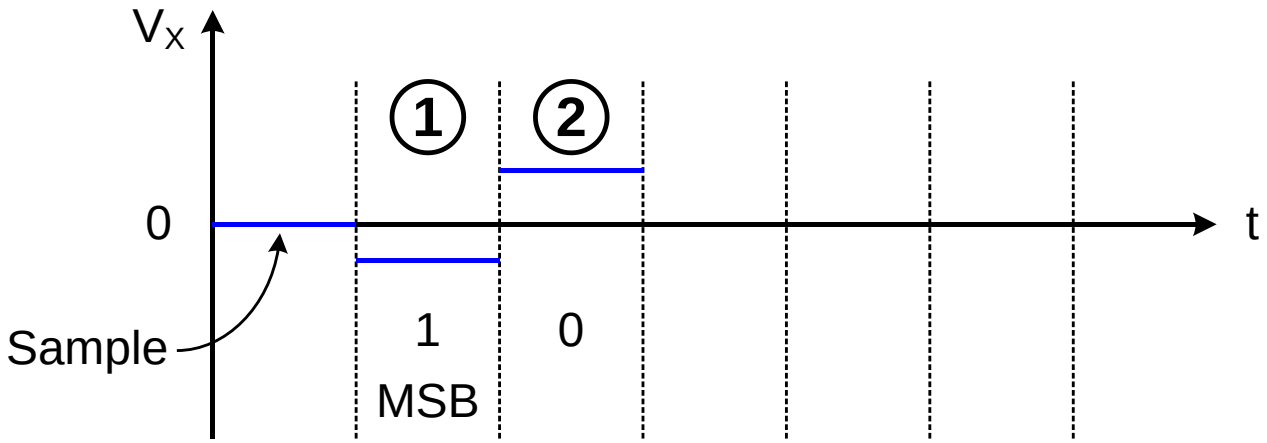
- If $V_X < 0$, then $V_i > V_R/2$, and MSB = 1, C_4 remains connected to V_R
- If $V_X > 0$, then $V_i < V_R/2$, and MSB = 0, C_4 is switched to ground

Charge Redistribution (MSB-1)



$$V_i \cdot 16C = (V_R - V_X) \cdot 12C - V_X \cdot 4C \Rightarrow V_X = (V_R \cdot 12C - V_i \cdot 16C)/16C = \frac{3}{4}V_R - V_i$$

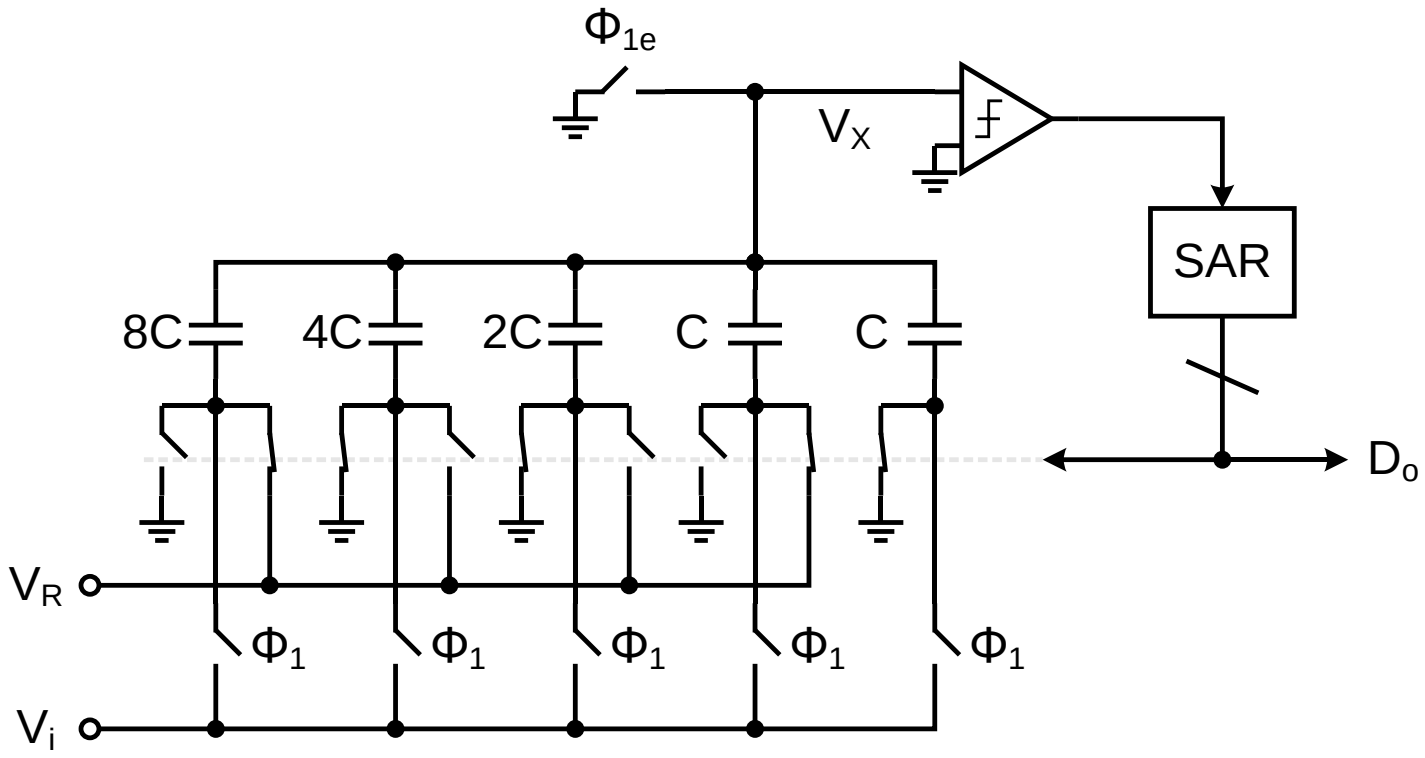
Comparison (MSB-1)



$$(\text{MSB-1})\ \text{TEST}:\ V_X = \frac{3}{4}V_R - V_i$$

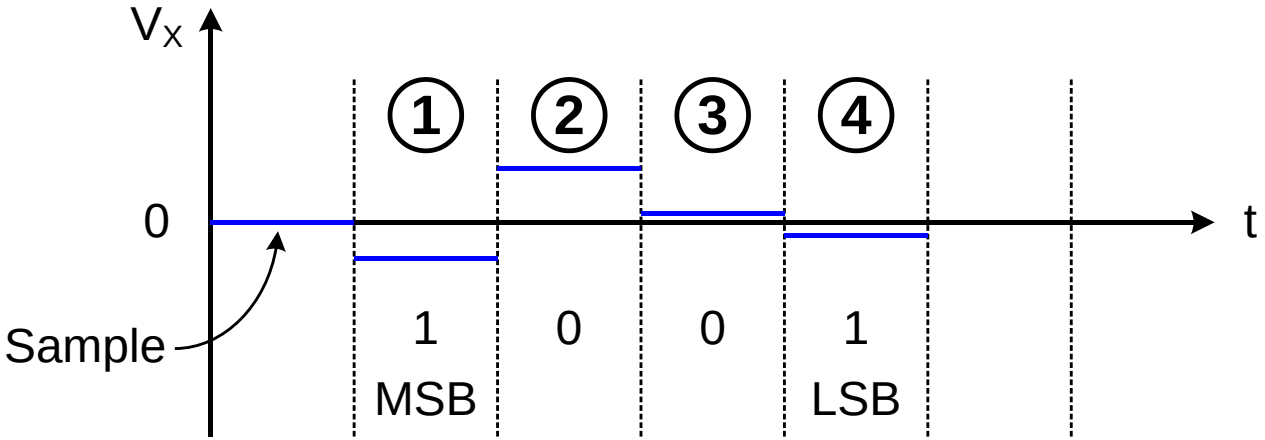
- If $V_X < 0$, then $V_i > 3V_R/4$, and MSB-1 = 1, C_3 remains connected to V_R
- If $V_X > 0$, then $V_i < 3V_R/4$, and MSB-1 = 0, C_3 is switched to ground

Charge Redistribution (Other Bits)



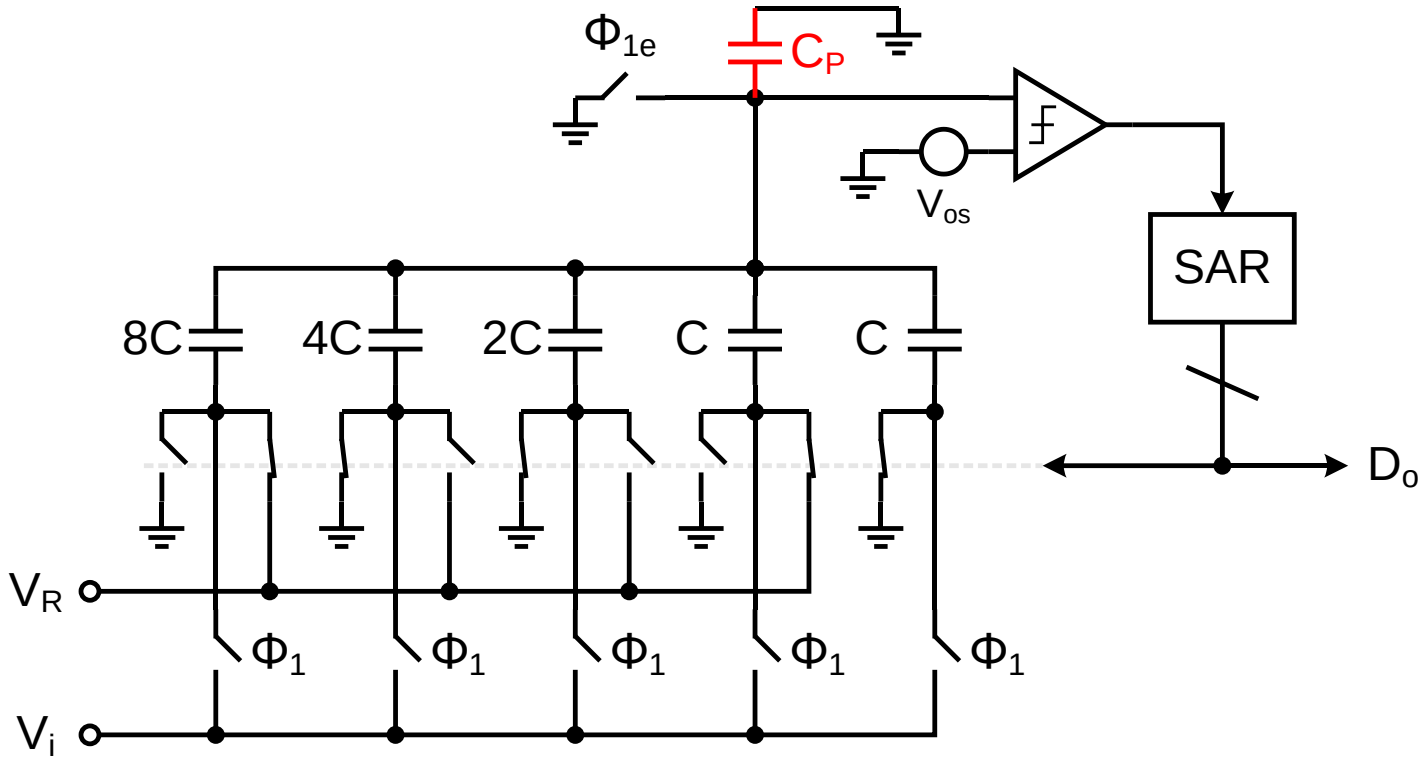
Test completes when all four bits are determined w/ four charge redistributions and comparisons

After Four Clock Cycles…



- Usually, half T_{clk} is allocated for charge redistribution and half for comparison + digital logic
- V_X always converges to 0 (V_{os} if comparator has nonzero offset)

Summing-Node Parasitics



- If V_{os} = 0, C_P has no effect eventually; otherwise, C_P attenuates V_X
- AZ can be applied to the comparator to reduce offset

Summary of SA ADC

- Power efficiency – only comparator consumes DC power
- DAC nonlinearity limits the INL and DNL of the SA ADC
  - N-bit precision requires N-bit matching from the cap array
  - Calibration can be performed to remove mismatch errors (Lee, JSSC'84)
- If $C_P = 0$, comparator offset V_{os} introduces a same input-referred offset V_{os}; if $C_P \neq 0$, input-referred offset is larger than $V_{os} \sim (1+C_P/\Sigma C_j)*V_{os}$
- If $V_{os} = 0$, C_P has no effect eventually ($V_X \rightarrow 0$ at the end of search); otherwise, V_X is always attenuated due to charge sharing
- Binary search is sensitive to intermediate errors made during search – if an intermediate decision is wrong, the digitization process cannot recover
  - DAC must settle into $\pm$½ LSB bound within the time allowed
  - Comparator offset must be constant (no hysteresis or time-dependent offset)
  - Non-binary search algorithm can be used (Kuttner, ISSCC'02)

References

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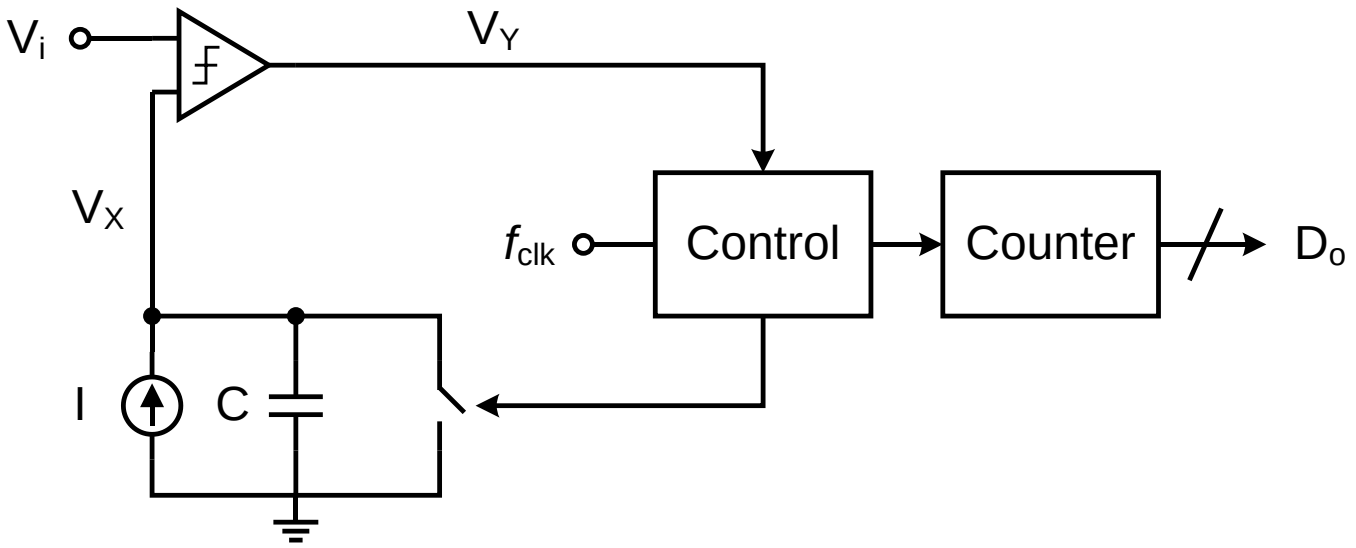
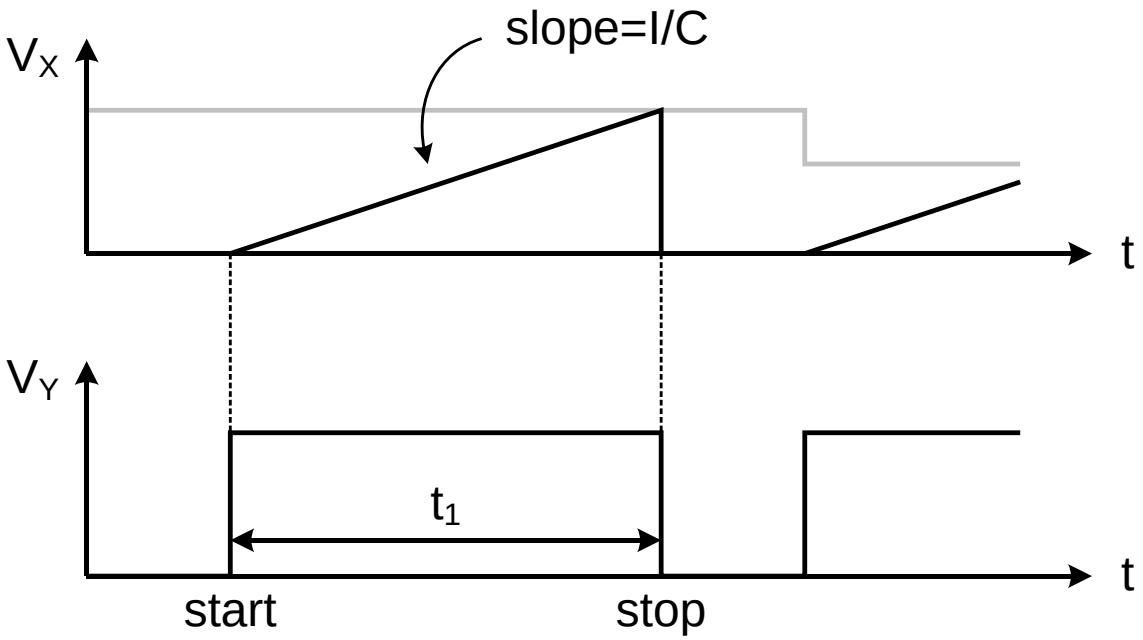
Single-Slope Integrating ADC



- Sampled-and-hold input (V_i)
- Counter keeps counting until comparator output toggles
- Simple, inherently monotonic, but very slow (2^N*T_{clk}/sample)

Single-Slope Integrating ADC



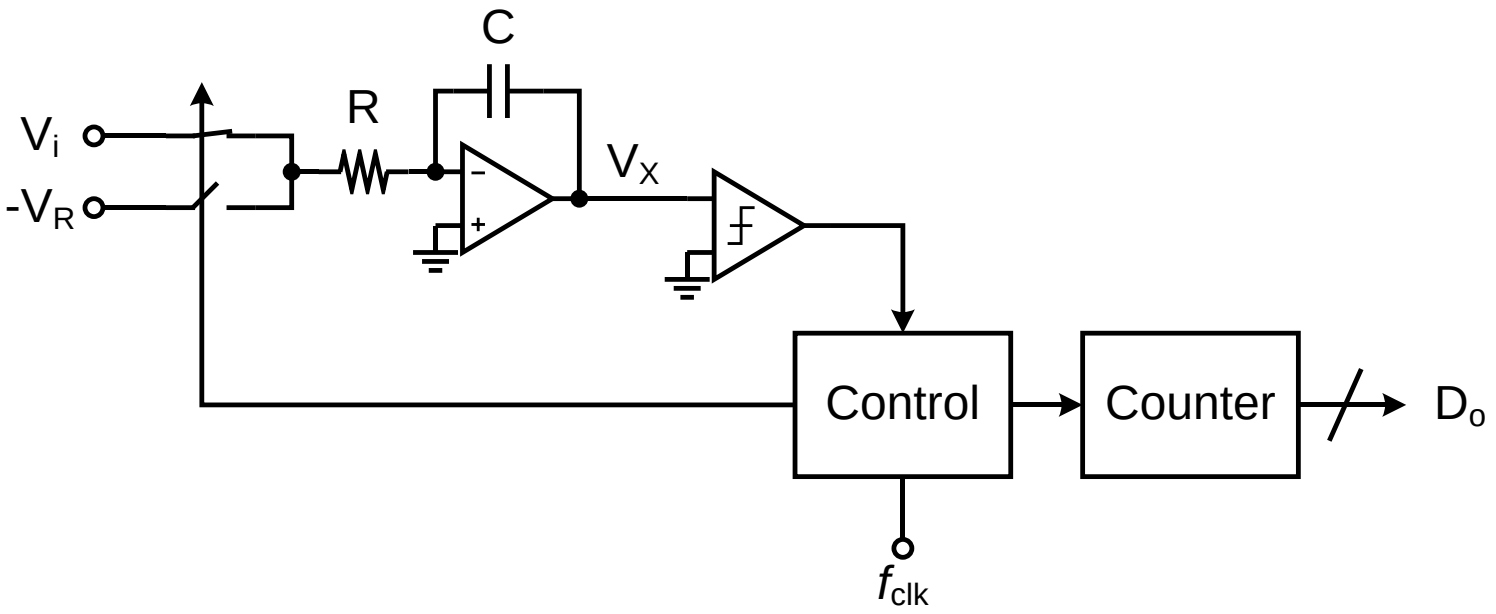
$$V_i = \frac{I}{C} \cdot t_1, \quad D_o = \left\lfloor \frac{t_1}{T_{clk}} \right\rfloor$$

$$\Rightarrow D_o = \left\lfloor \frac{V_i}{\left(\frac{I \cdot T_{clk}}{C} \right)} \right\rfloor,$$

$$LSB = \frac{I \cdot T_{clk}}{C}$$

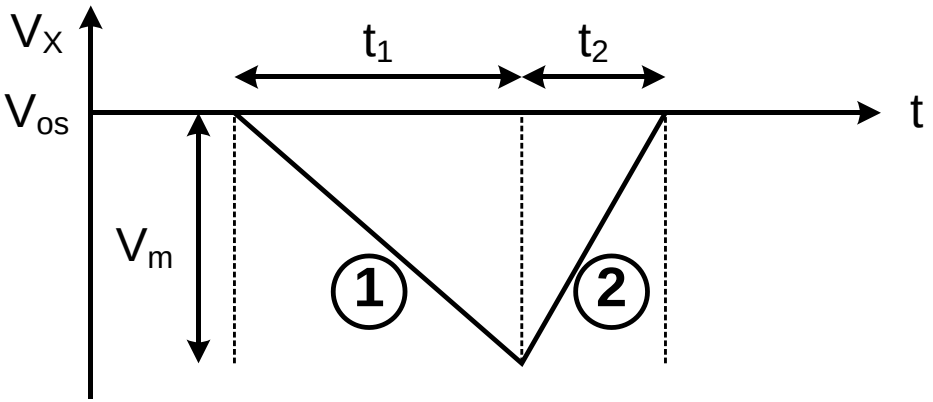
- INL depends on the linearity of the ramp signal
- Precision capacitor (C), current source (I), and clock (T_{clk}) required
- Comparator must handle wide input range of [0, V_{FS}]

Dual-Slope Integrating ADC



- RC integrator replaces the I-C integrator
- Input and reference voltages undergo the same signal path
- Comparator only detects zero crossing

Dual-Slope Integrating ADC



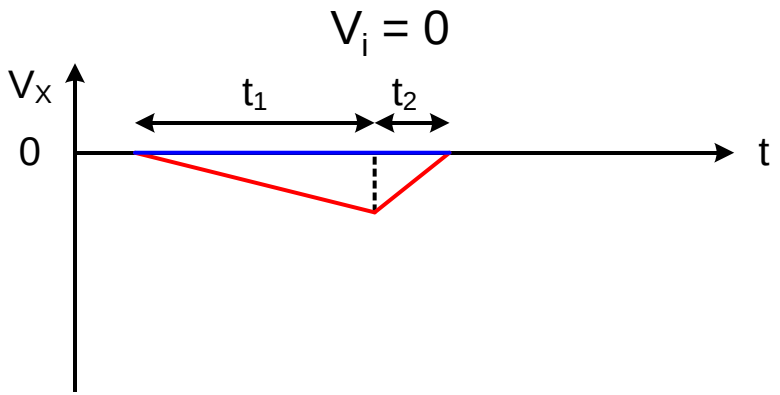
$$V_m = \frac{V_i}{RC} \cdot t_1 = \frac{V_R}{RC} \cdot t_2$$

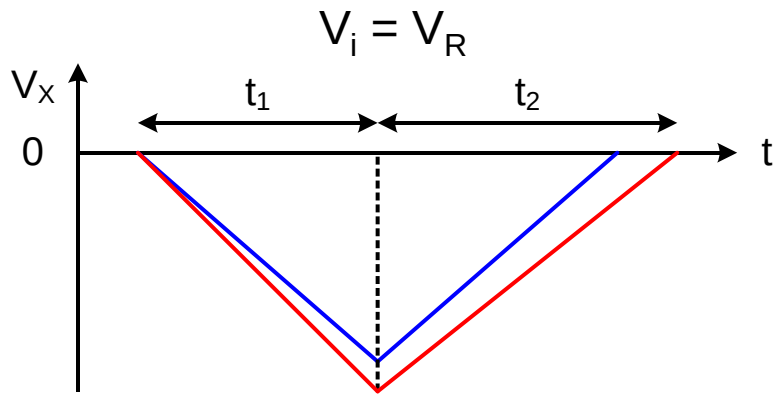
$$\Rightarrow D_o = \left\lfloor \frac{V_i}{V_R} \right\rfloor = \left\lfloor \frac{t_2}{t_1} \right\rfloor = \frac{N_2}{N_1}$$

or $D_o = N_2$ for fixed N_1

- Exact values of R, C, and T_{clk} are not required
- Comparator offset doesn't matter (what about its delay?)
- Op-amp offset introduces gain error and offset (why?)
- Op-amp nonlinearity introduces INL error

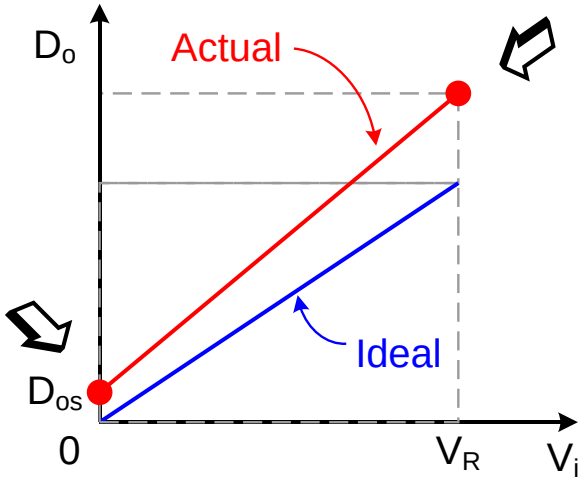
Op-Amp Offset



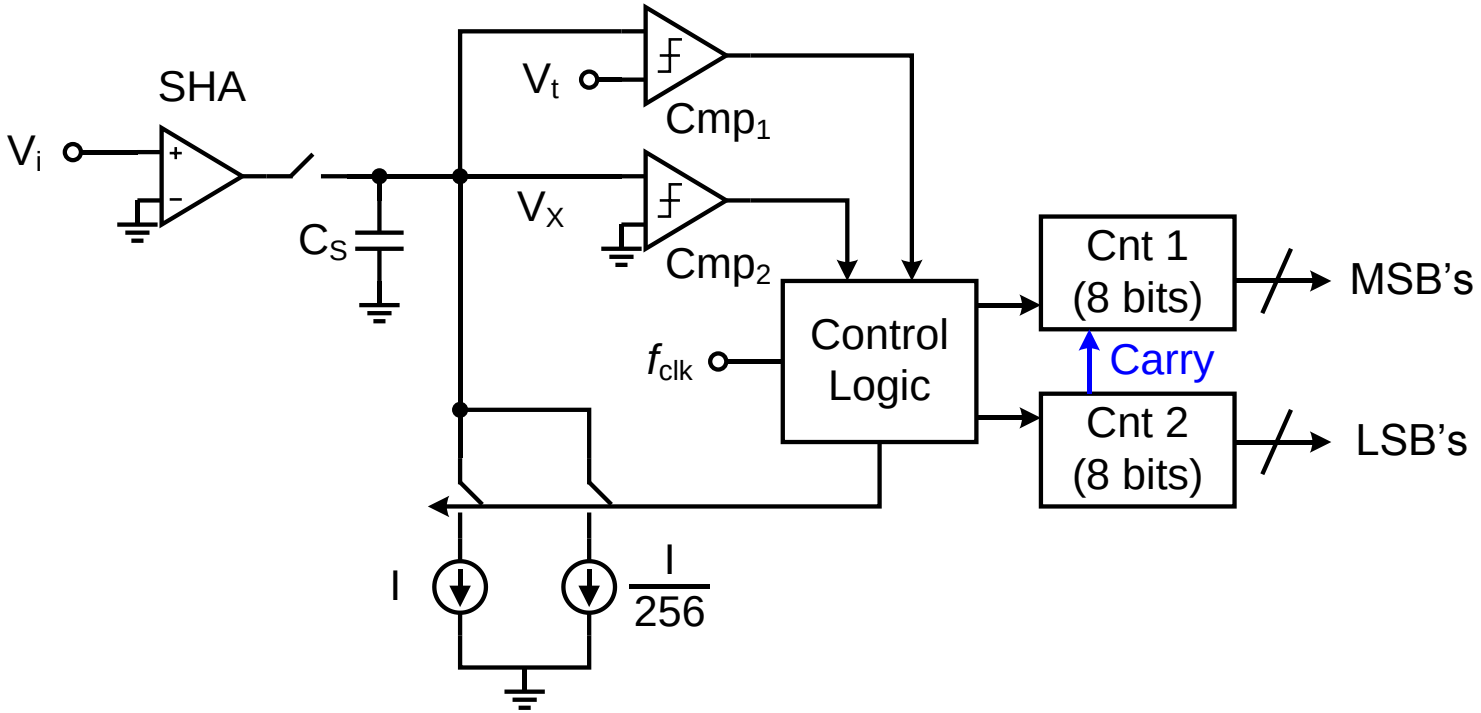


$N_2 \neq 0 \rightarrow$ Offset

Longer integration time!

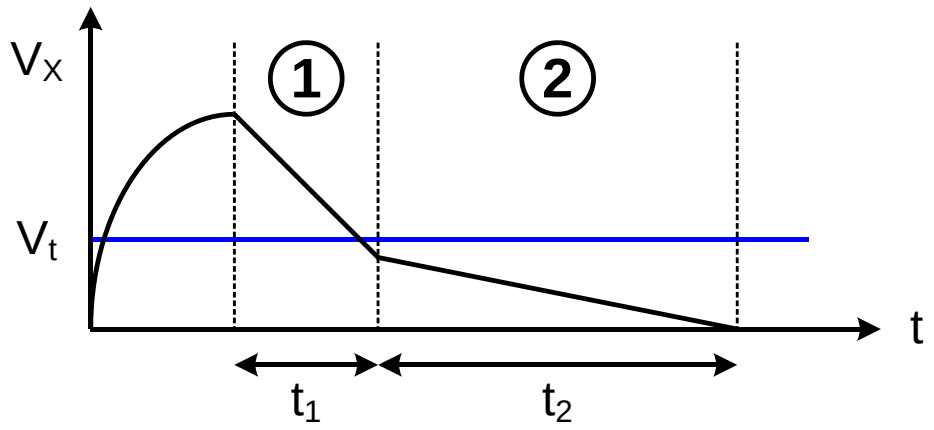


Subranging Dual-Slope ADC



- MSB discharging stops at the immediate next integer count past V_t
- Much faster conversion speed compared to dual-slope
- Two current sources (matched) and two comparators required

Subranging Dual-Slope ADC



$$\frac{dV_X(1)}{dt} = \frac{I}{C},$$

$$\frac{dV_X(2)}{dt} = \frac{I}{256C}$$

$$D_o = N_1 \cdot W + N_2$$

- Precise V_t is not required if carry is propagated
- Matching between the current sources is critical

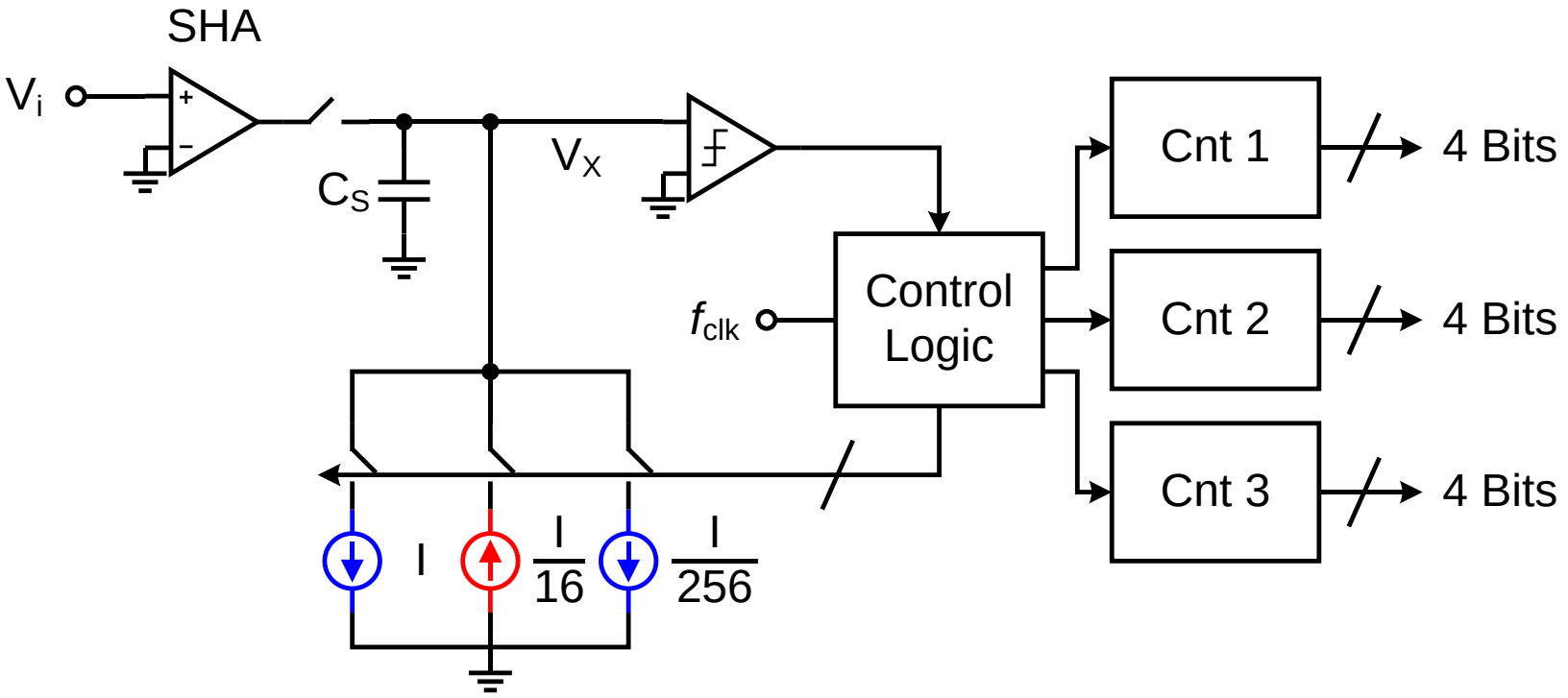
  → if $I_1 = I$, $I_2 = (1+\delta)\cdot I/256$, then $|\delta| \le 0.5/256$
- It'd be nice if CMP 1 can be eliminated → ZX detector!

Subranging Dual-Slope ADC

- CMP 1 response time is not critical
- Delay from CNT 1 to MSB current shut-off is not critical

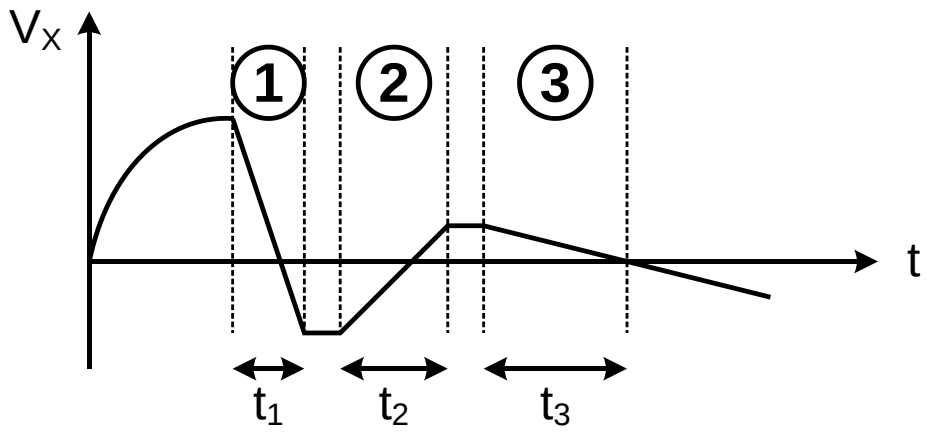
  → constant delay results in an offset
- CMP 2 response time is critical

Subranging Multi-Slope ADC



Ref: J.-G. Chern and A. A. Abidi, "An 11 bit, 50 kSample/s CMOS A/D converter cell using a multislope integration technique," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 1989, pp. 6.2/1-6.2/4.

Subranging Multi-Slope ADC



$$\frac{dV_X(1)}{dt} = \frac{I}{C},$$

$$\frac{dV_X(2)}{dt} = -\frac{I}{16C},$$

$$\frac{dV_X(3)}{dt} = \frac{I}{256C}$$

$$D_o = N_1 \cdot W_1 - N_2 \cdot W_2 + N_3$$

- Single comparator detects zero-crossing
- Comparator response time greatly relaxed
- Matching between the current sources still critical

Subranging Multi-Slope ADC

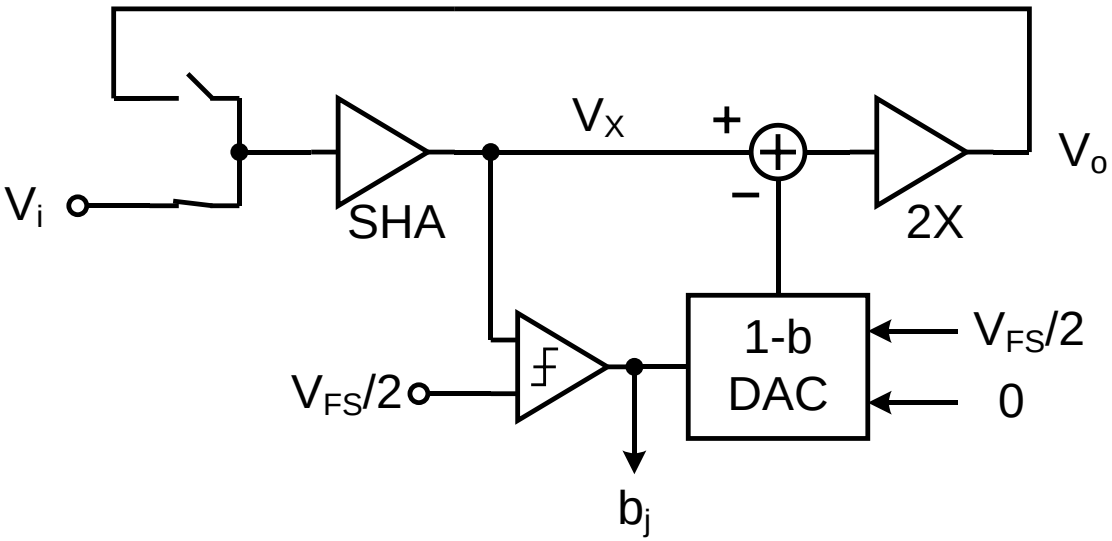
- Comparator response time is not critical except the last one
- Delays from CNTs to current sources shut-off are not critical

  → constant delay results in an offset
- Last comparator response time is critical

Outline

- 8.1 Introduction
- 8.2 Nyquist Rate ADC
- 8.3 SAR ADC
- 8.4 Integrating ADC
- 8.5 Algorithmic ADC
- 8.6 Pipelined ADC
- 8.7 Subranging ADC

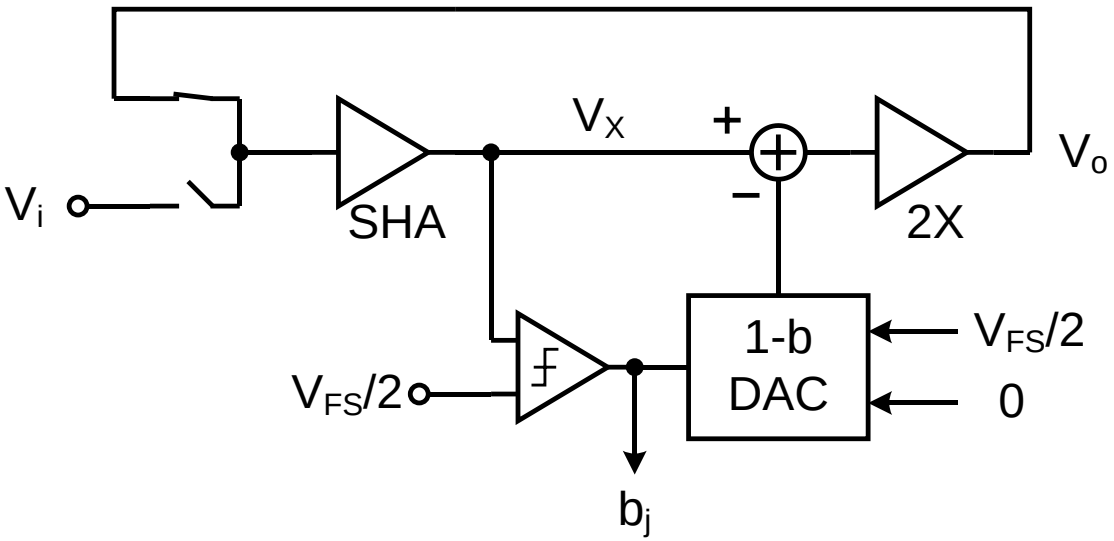
Algorithmic (Cyclic) ADC



Sample mode

- Input is sampled first, then circulates in the loop for N clock cycles
- Conversion takes N cycles with one bit resolved in each T_{clk}

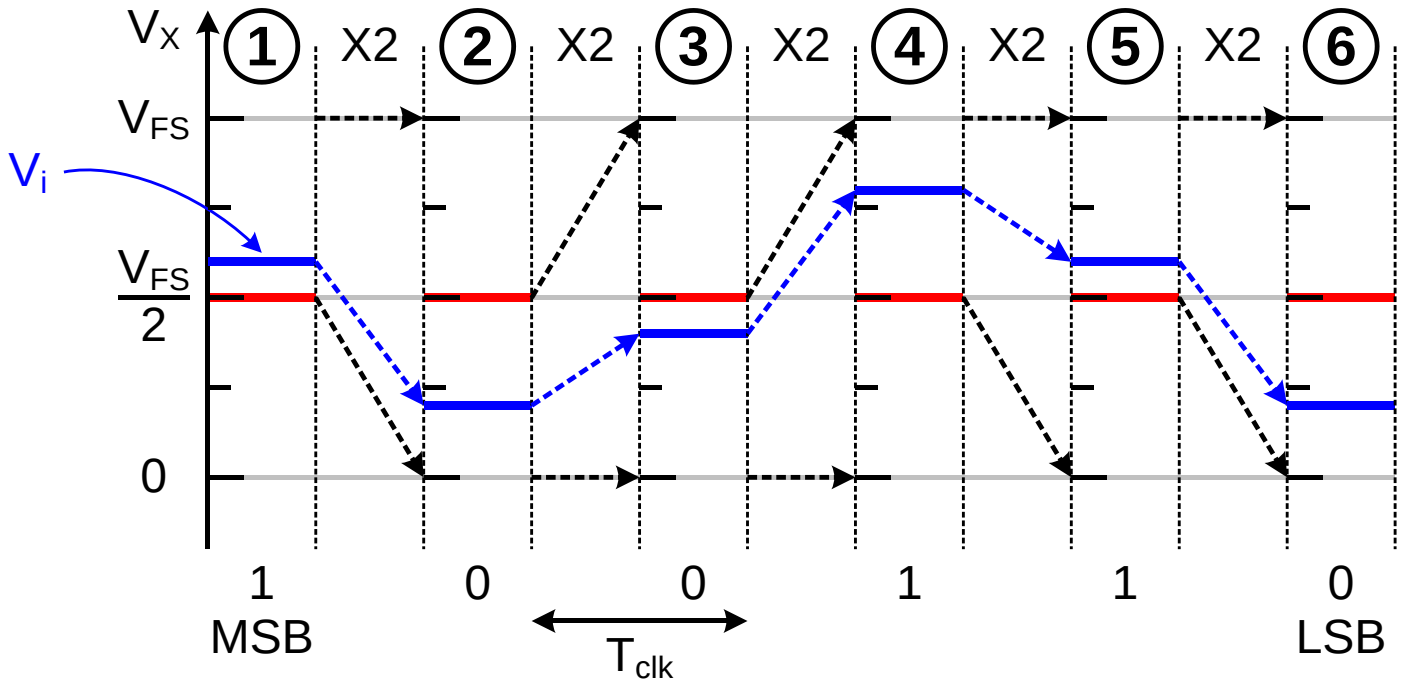
Modified Binary Search



Conversion mode

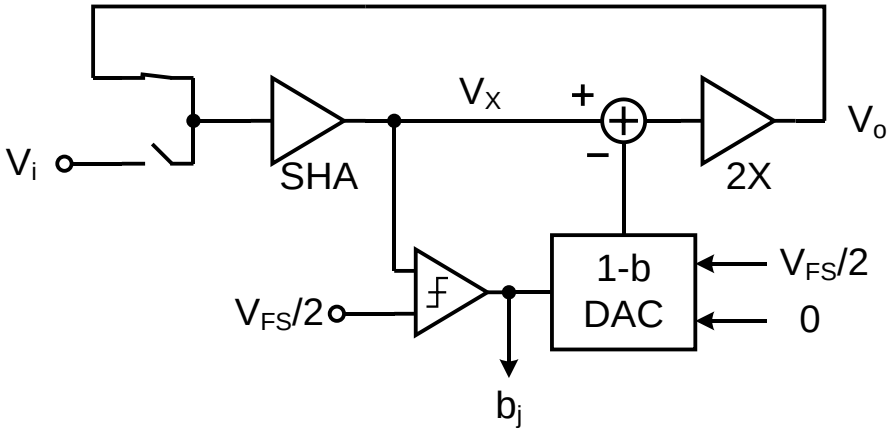
- If $V_X < V_{FS}/2$, then $b_j = 0$, and $V_o = 2*V_X$
- If $V_X > V_{FS}/2$, then $b_j = 1$, and $V_o = 2*(V_X - V_{FS}/2)$
- V_o is called conversion "**residue**"

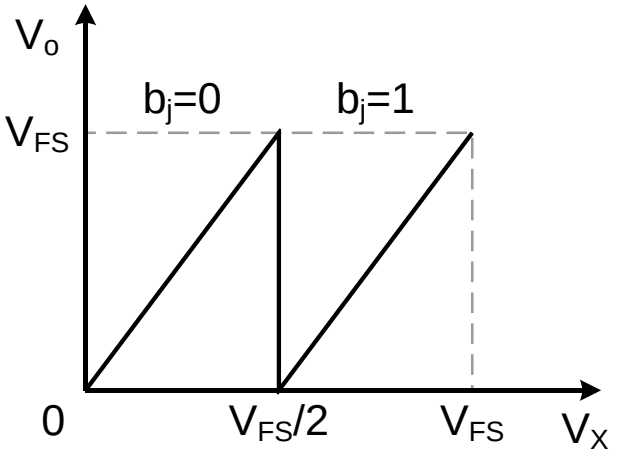
Modified Binary Search



- Constant threshold ($V_{FS}/2$) is used for each comparison
- Residue experiences 2X gain each time it circulates the loop

Loop Transfer Function



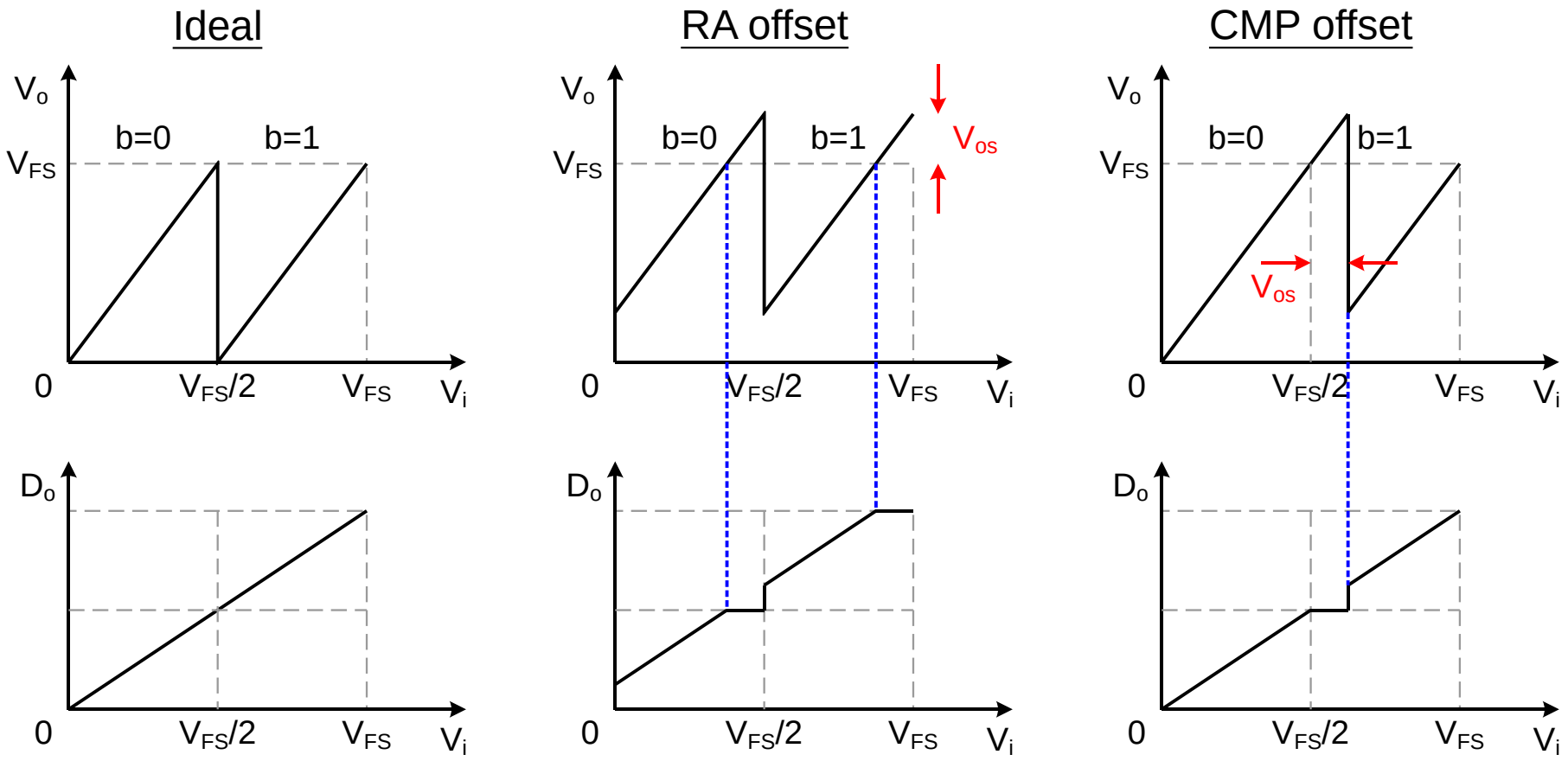


- Comparison → if $V_X < V_{FS}/2$, then $b_j = 0$; otherwise, $b_j = 1$
- Residue generation → $V_o = 2*(V_X - b_j*V_{FS}/2)$

Algorithmic ADC

- Hardware-efficient, but relatively low conversion speed (bit-per-step)
- Modified binary search algorithm
- Loop-gain (2X) requires the use of a residue amplifier (RA), but greatly simplifies the DAC → 1-bit, inherently linear (why?)
- Residue gets amplified in each circulation; the gain accumulated makes the later conversion steps insensitive to circuit noise and distortion
- Conversion errors (residue error due to comparator offset and/or loop-gain nonidealities) made in earlier conversion cycles also get amplified again and again – overall accuracy is usually limited by the MSB conversion step
- Digital redundancy is often employed to tolerate comparator/loop offsets
- Trimming/calibration/ratio-independent techniques are often used to treat loop-gain error, nonlinearity, etc.

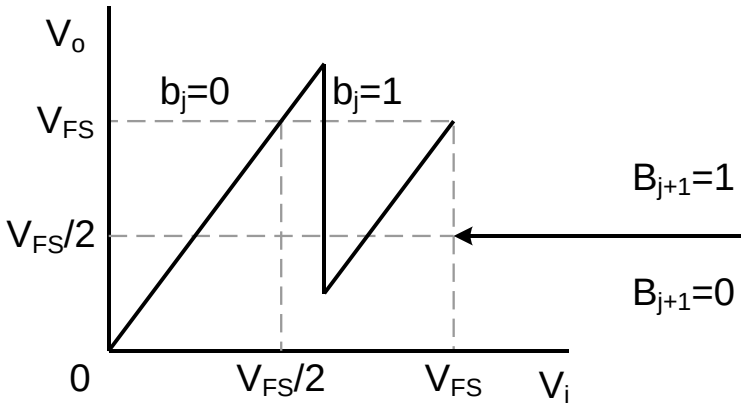
Offset Errors

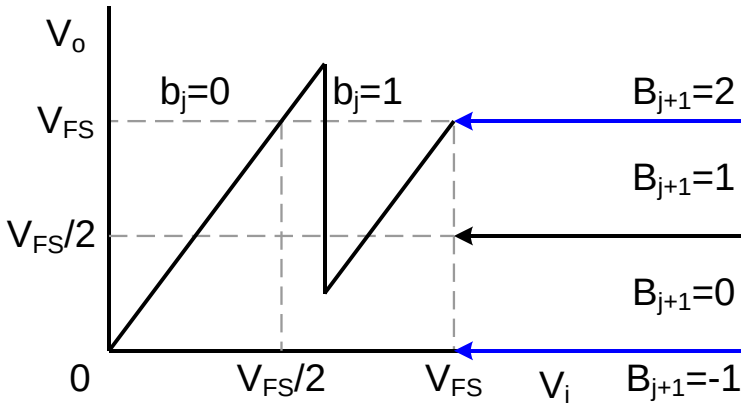


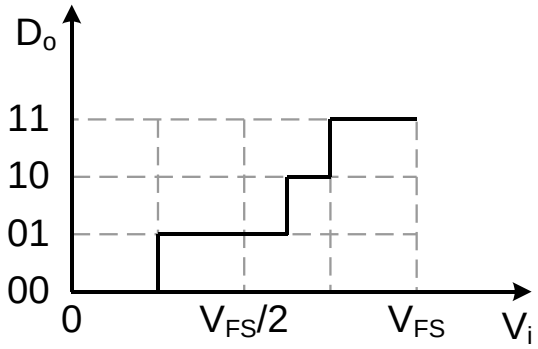
$$V_o = 2*(V_i - b_j*V_{FS}/2) \rightarrow \mathbf{V_i = b_j*V_{FS}/2 + V_o/2}$$

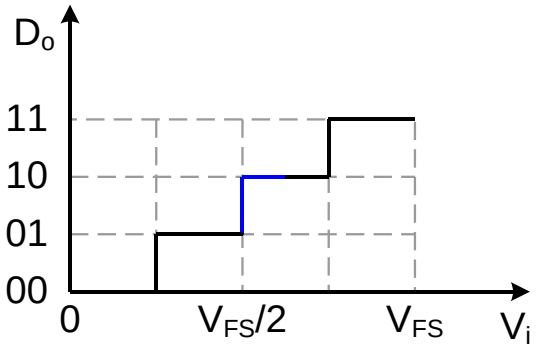
Digital Redundancy (DEC, RSD)

DEC: Digital Error Correction, RSD: Redundant Signed Digit







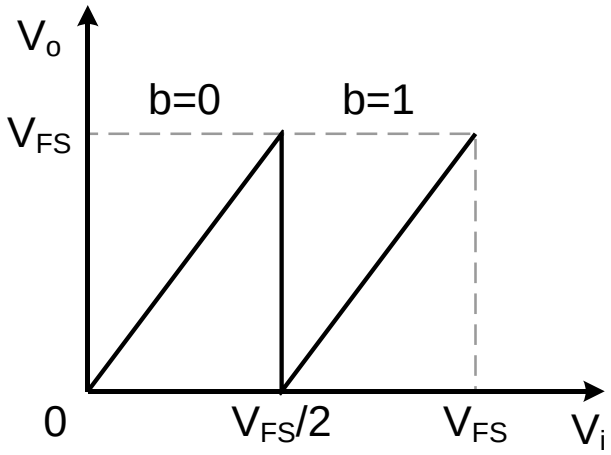


1 CMP

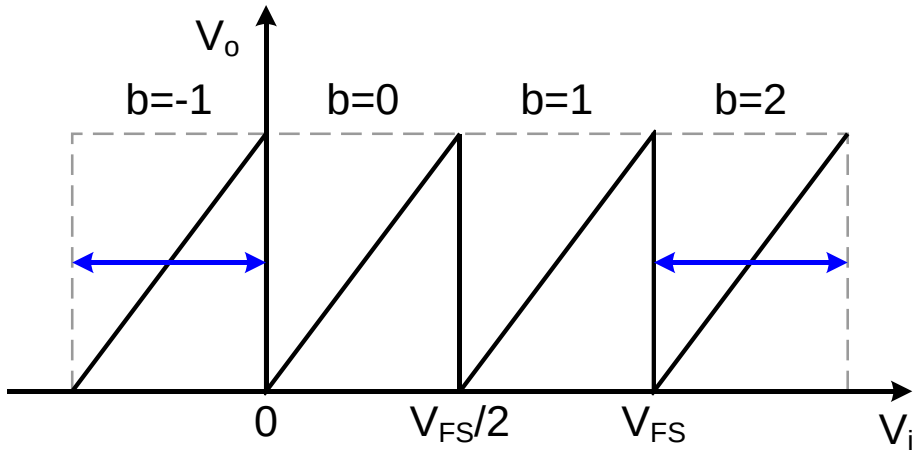
3 CMPs

Loop Transfer Function

Original

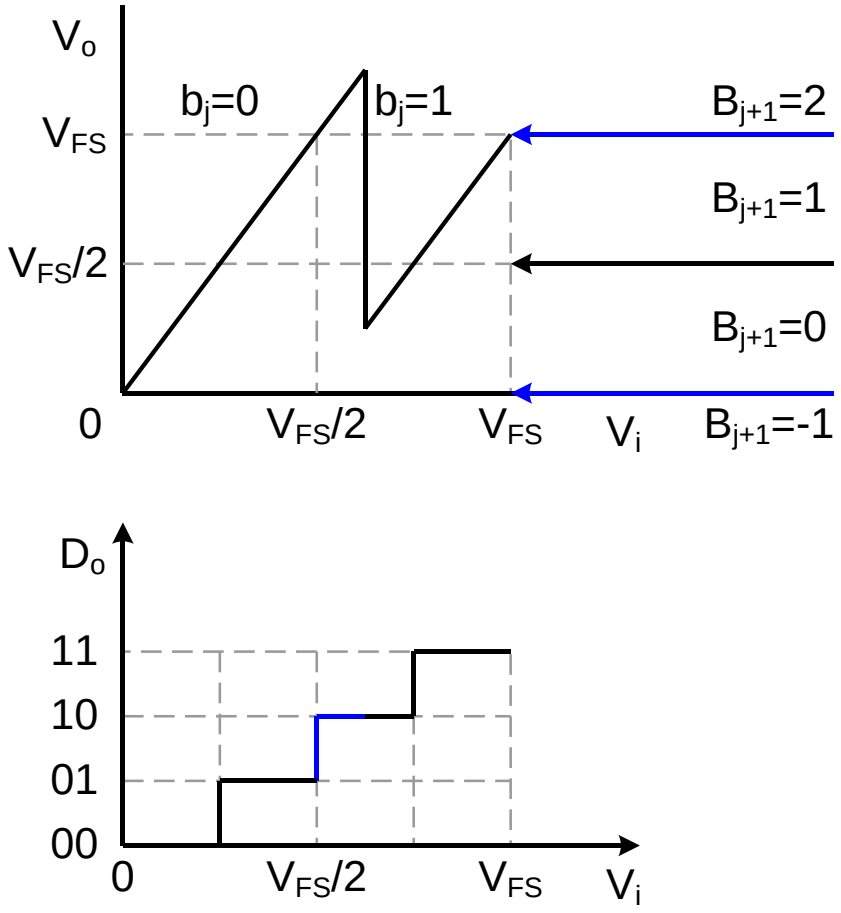


w/ Redundancy



- Subtraction/addition both required to compute final sum
- 4-level (2-bit) DAC required instead of 2-level (1-bit) DAC

Comparator Offset

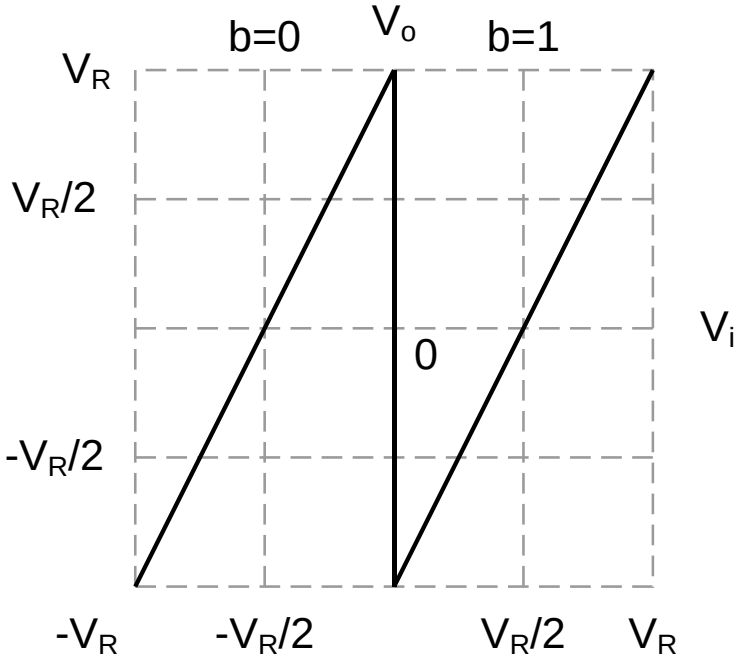


- Max tolerance of comparator offset is $\pm V_{FS}/4$ → simple comparators
- Similar tolerance also applies to RA offset
- Key to understand digital redundancy:

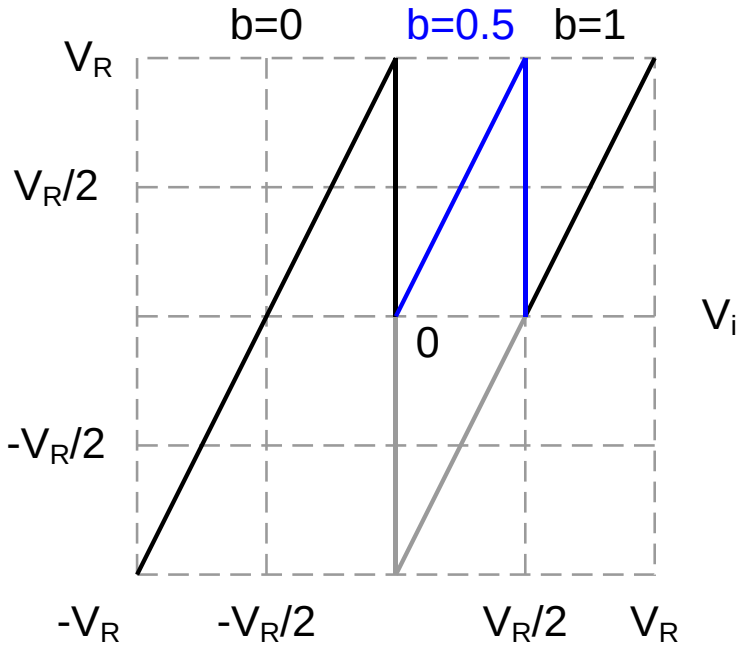
$$V_i = b_j \cdot \frac{V_{FS}}{2} + \frac{V_o}{2}$$

$$b_j \Leftrightarrow V_o$$

Modified 1-Bit Architecture

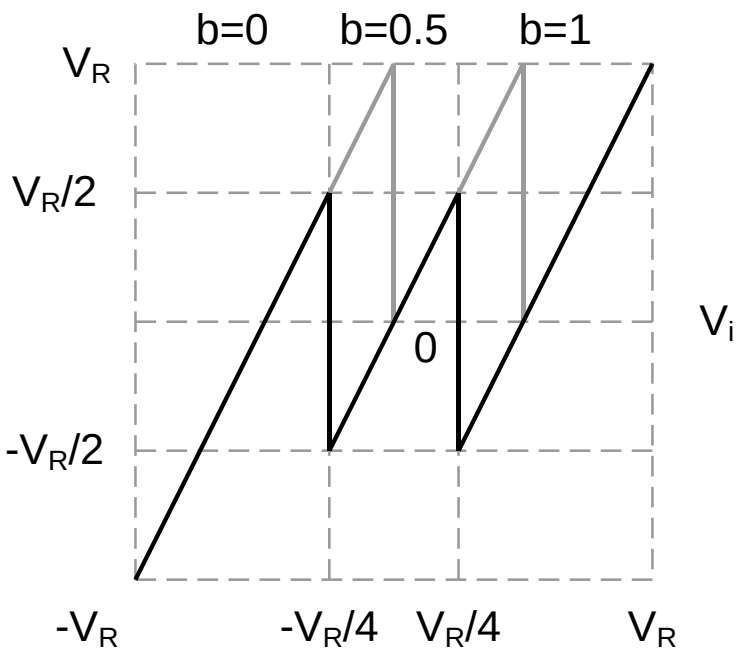


1-b/s RA transfer curve
w/ no redundancy

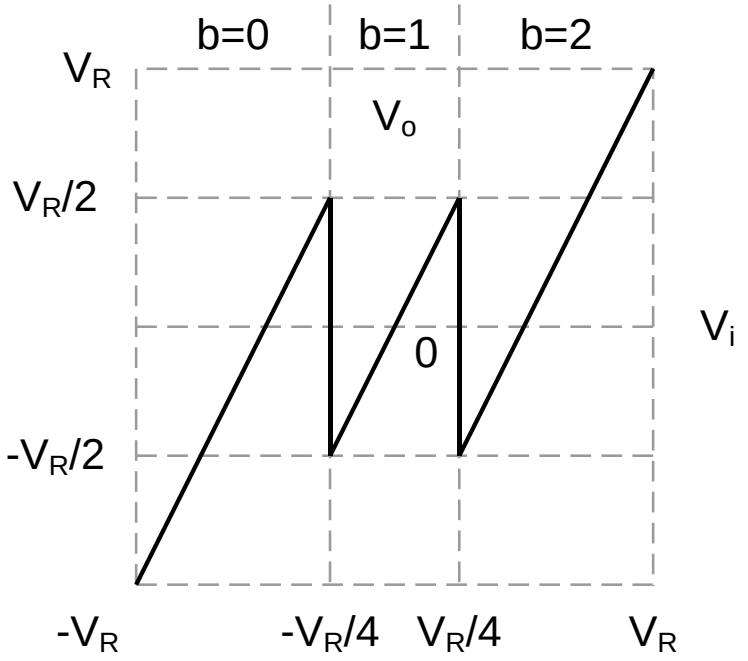


One extra CMP
added at $V_R/2$

From 1-Bit to 1.5-Bit Architecture

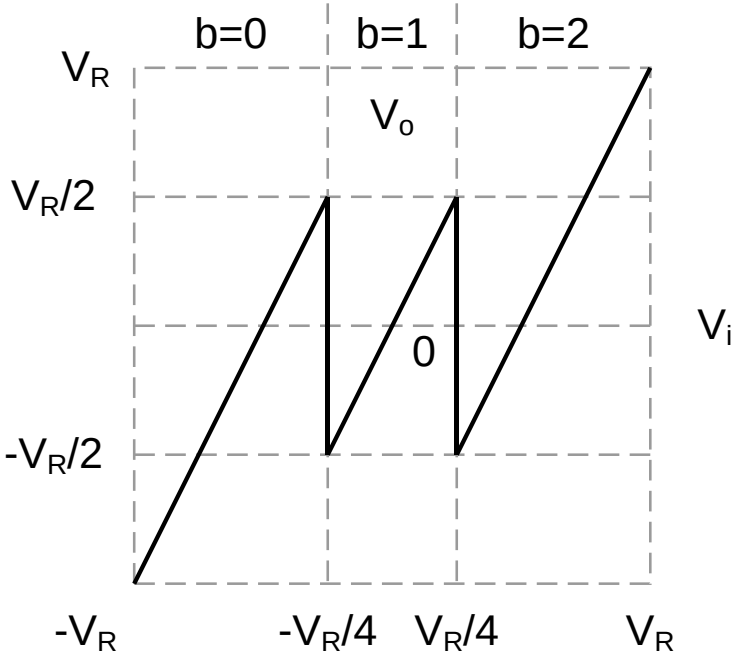


A systematic offset $-V_R/4$ introduced to both CMPs



A 2X scaling is performed on all output bits

The 1.5-Bit Architecture

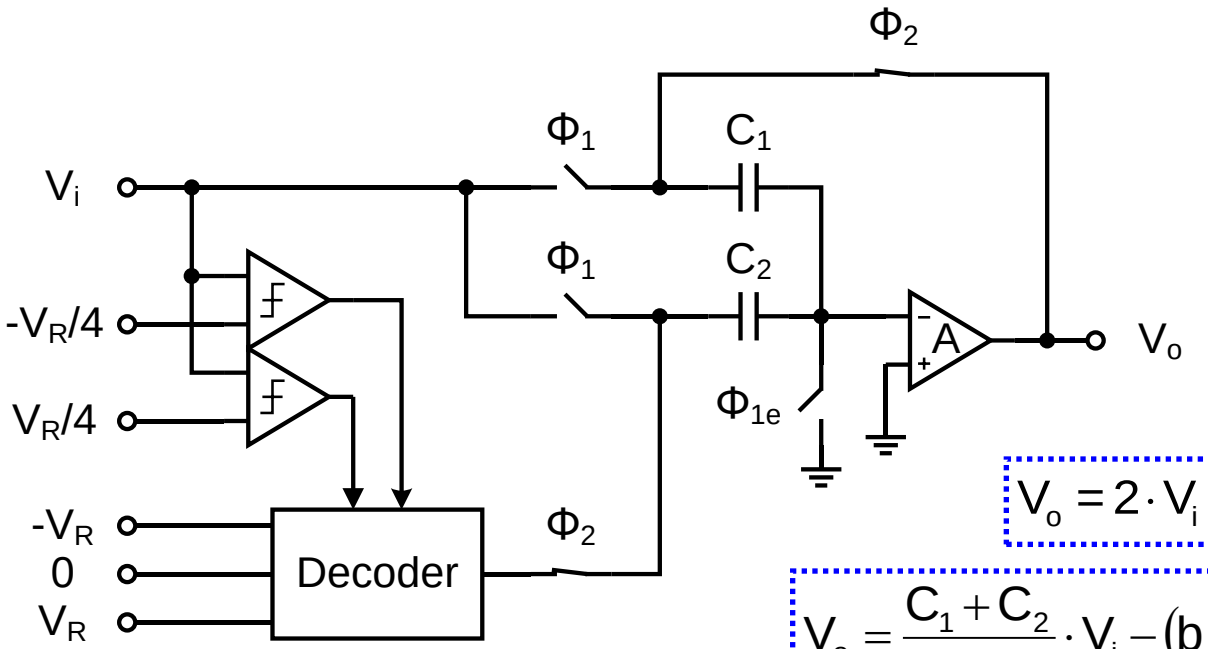


$$V_o = 2 \cdot V_i - (b-1) \cdot V_R$$

- 3 decision levels
  → ENOB = $\log_2 3 = 1.58$
- Max tolerance of comparator offset is $\pm V_R/4$
- An implementation of the Sweeney-Robertson-Tocher (SRT) division principle
- The conversion accuracy solely relies on the loop-gain error, i.e., the gain error and nonlinearity
- A 3-level DAC is required

Can this technique be applied to SA ADC?

The Multiplier DAC (MDAC)



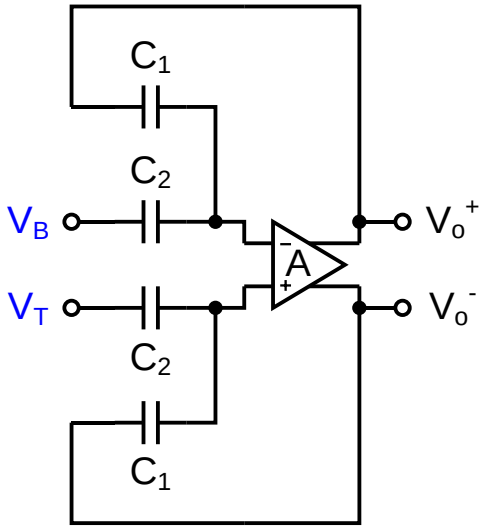
$$V_o = 2 \cdot V_i - (b-1) \cdot V_R$$

$$V_o = \frac{C_1 + C_2}{C_1} \cdot V_i - (b-1)\frac{C_2}{C_1} \cdot V_R$$

- 2X gain + 3-level DAC + subtraction all integrated
- A 3-level DAC is perfectly linear in fully-differential form
- Can be generalized to n.5-b/stage architectures

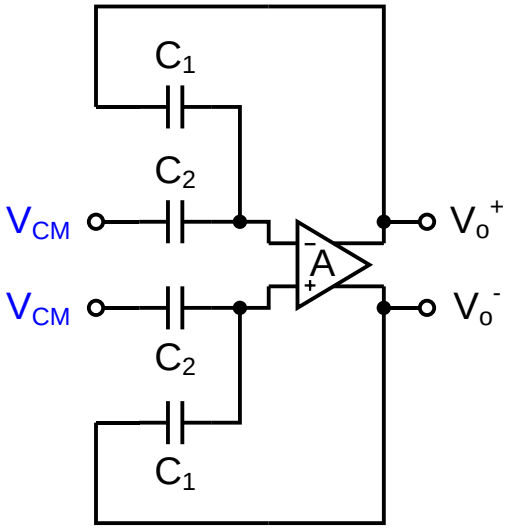
A Linear 3-Level DAC

b = 0



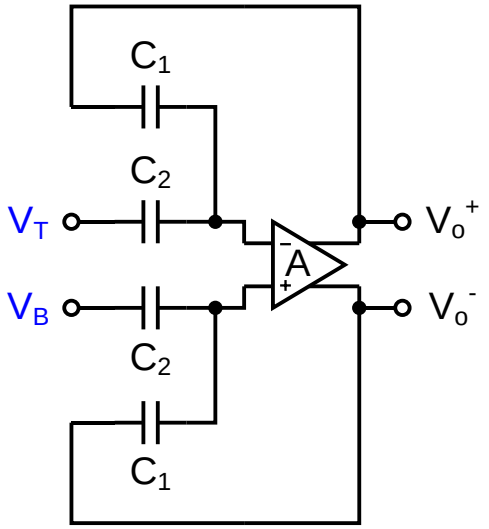
$$V_o = V_o^+ - V_o^-$$
$$= \frac{C_1 + C_2}{C_1} \cdot V_i - \frac{C_2}{C_1} \cdot (V_B - V_T)$$
$$= 2 \cdot V_i + V_R$$

b = 1



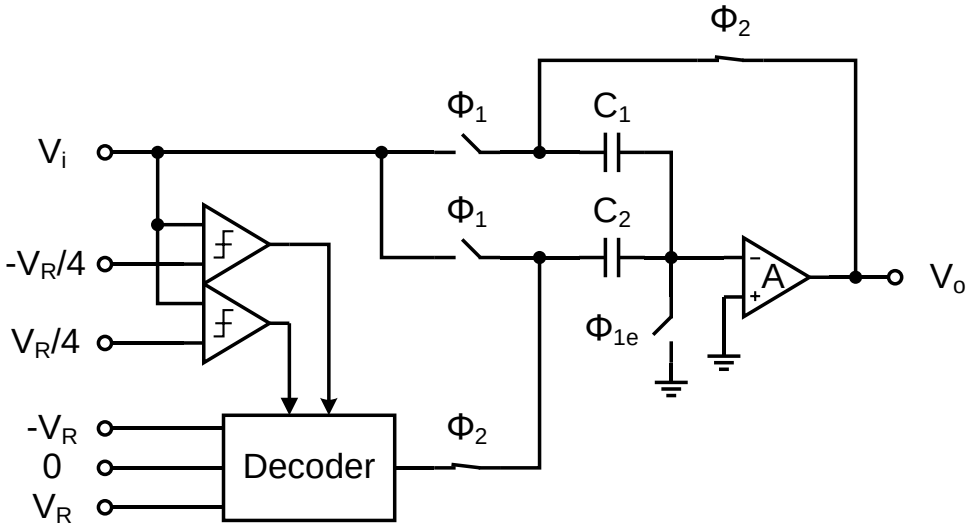
$$V_o = V_o^+ - V_o^-$$
$$= \frac{C_1 + C_2}{C_1} \cdot V_i + \frac{C_2}{C_1} \cdot (V_{CM} - V_{CM})$$
$$= 2 \cdot V_i$$

b = 2



$$V_o = V_o^+ - V_o^-$$
$$= \frac{C_1 + C_2}{C_1} \cdot V_i - \frac{C_2}{C_1} \cdot (V_T - V_B)$$
$$= 2 \cdot V_i - V_R$$

Error Mechanisms of RA

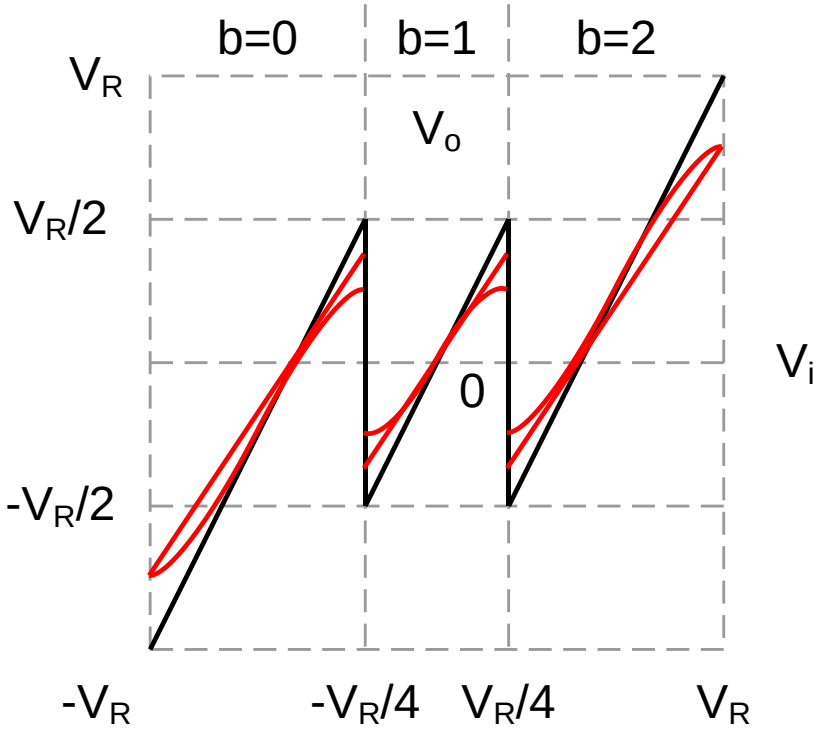


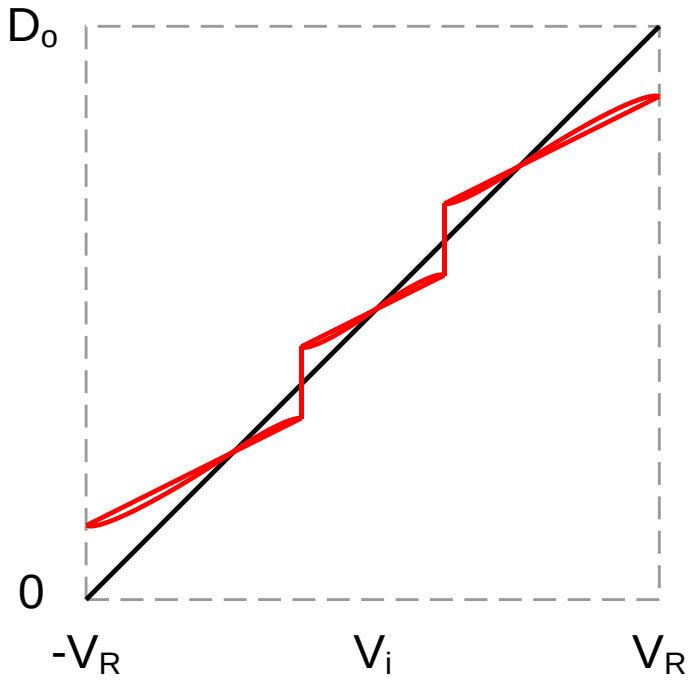
- Capacitor mismatch
- Op-amp finite-gain error and nonlinearity
- Charge injection and clock feedthrough (S/H)
- Finite circuit bandwidth

$$V_o = 2 \cdot V_i - (b-1) \cdot V_R$$

$$V_o(t=\infty) = \frac{C_1 + C_2}{C_1 + \frac{C_1 + C_2}{A(V_o)}} \cdot f_{S/H}(V_i) - (b-1) \frac{C_2}{C_1 + \frac{C_1 + C_2}{A(V_o)}} \cdot V_R$$

RA Gain Error and Nonlinearity





Raw accuracy is usually limited to 10-12 bits w/o error correction

Static Gain-Error Correction

Analog-domain method:

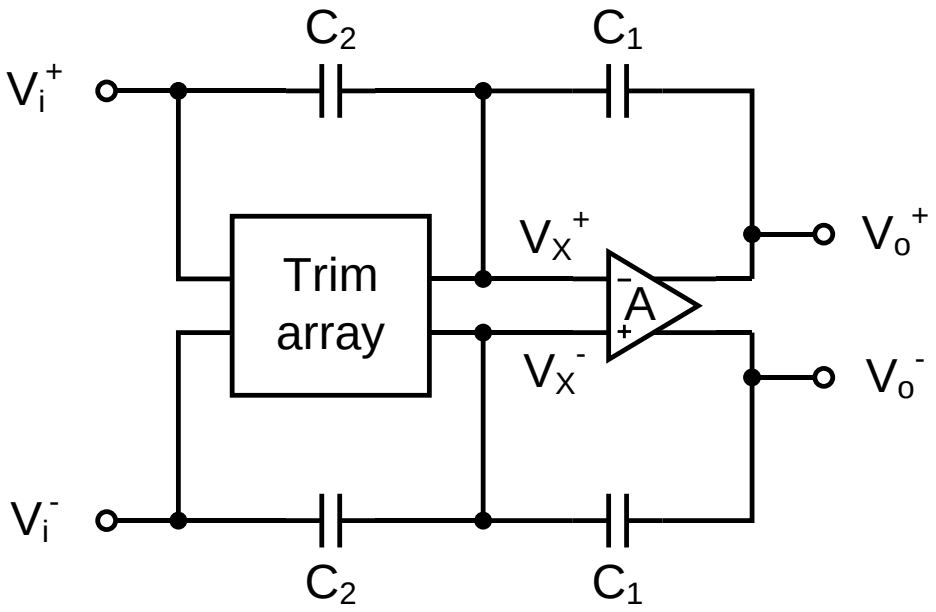
$$V_o = \frac{C_1 + C_2}{C_1 + \frac{C_1 + C_2}{A}} \cdot V_i - b \cdot \frac{C_2}{C_1 + \frac{C_1 + C_2}{A}} \cdot V_R = ka_1 \cdot V_i - b \cdot (ka_2 \cdot V_R)$$

Digital-domain method:

$$\left(\frac{V_i}{V_R}\right) = \frac{C_1 + \frac{C_1 + C_2}{A}}{C_1 + C_2} \cdot \left(\frac{V_o}{V_R}\right) + \frac{C_2}{C_1 + C_2} \cdot b \Rightarrow D_i = kd_1 \cdot D_o + kd_2 \cdot b$$

Do we need to correct for kd_2 error?

RA Gain Trimming

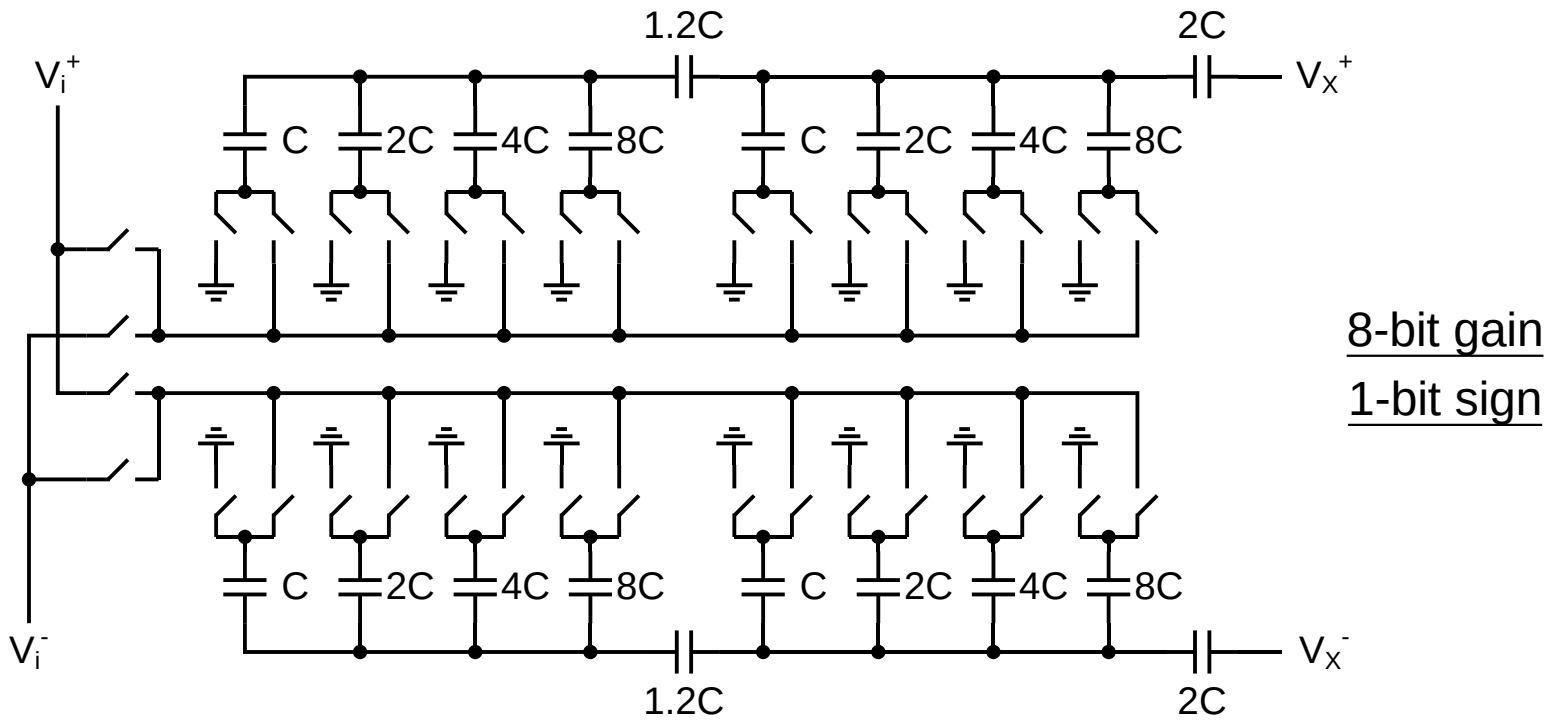


$C_1/C_2 = 1$ nominally

$$V_o = \frac{(C_1 + C_2)}{C_1 + \frac{C_1 + C_2}{A}} \cdot V_i - \frac{C_2}{C_1 + \frac{C_1 + C_2}{A}} \cdot (b-1) V_R$$

- Precise gain-of-two is achieved by adjustment of the trim array
- Finite-gain error of op-amp is also compensated (**not nonlinearity**)

Split-Array Trimming DAC



- Successive approximation utilized to find the correct gain setting
- Coupling cap is slightly increased to ensure segmental overlap

Digital Radix Correction

$$\left(\frac{V_i}{V_R}\right)=\frac{C_1+\frac{C_1+C_2}{A}}{C_1+C_2}\cdot\left(\frac{V_o}{V_R}\right)+\frac{C_2}{C_1+C_2}\cdot b \quad\Rightarrow\quad \boxed{D_i=kd_1\cdot D_o+kd_2\cdot b}$$

Unroll this:

$$\begin{aligned}
D_j &= kd_2\cdot b_j + kd_1\cdot D_{j+1}\\
&= kd_2\cdot b_j + kd_1\cdot\left(kd_2\cdot b_{j+1}+kd_1\cdot D_{j+2}\right)\\
&= \left(kd_2\cdot b_j\right)+kd_1\cdot\left(kd_2\cdot b_{j+1}\right)+kd_1^{\,2}\cdot D_{j+2}\\
&= \left(kd_2\cdot b_j\right)+kd_1\cdot\left(kd_2\cdot b_{j+1}\right)+kd_1^{\,2}\cdot\left(kd_2\cdot b_{j+2}\right)+kd_1^{\,3}\cdot D_{j+3}\\
&= \left(kd_2\cdot b_j\right)+kd_1\cdot\left(kd_2\cdot b_{j+1}\right)+kd_1^{\,2}\cdot\left(kd_2\cdot b_{j+2}\right)+kd_1^{\,3}\cdot\left(kd_2\cdot b_{j+3}\right)+\ldots
\end{aligned}$$

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- 8.1 Introduction
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- 8.5 Algorithmic ADC
- 8.6 Pipelined ADC
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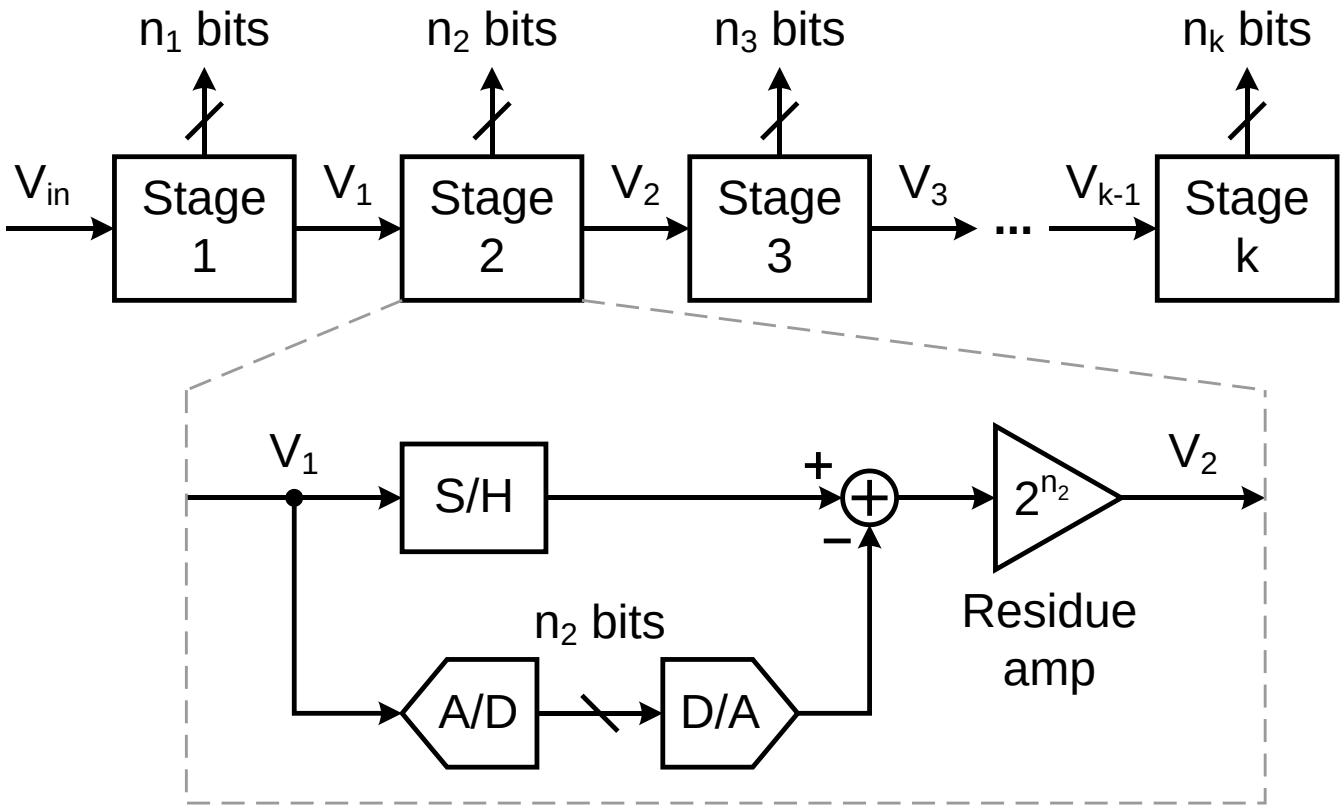
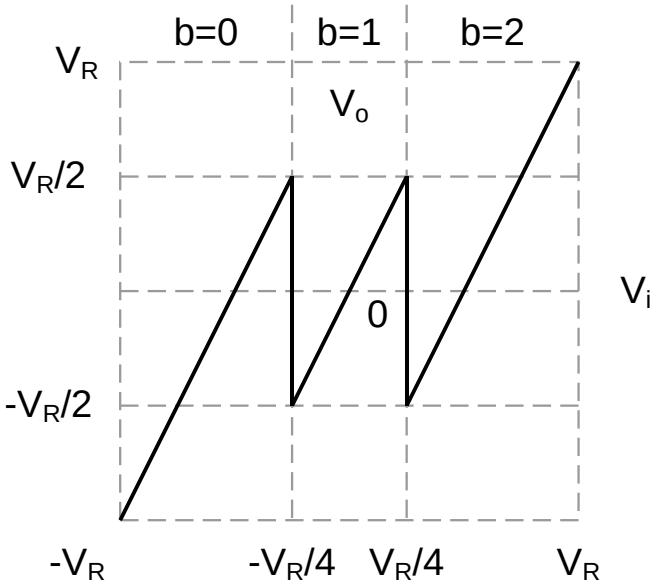
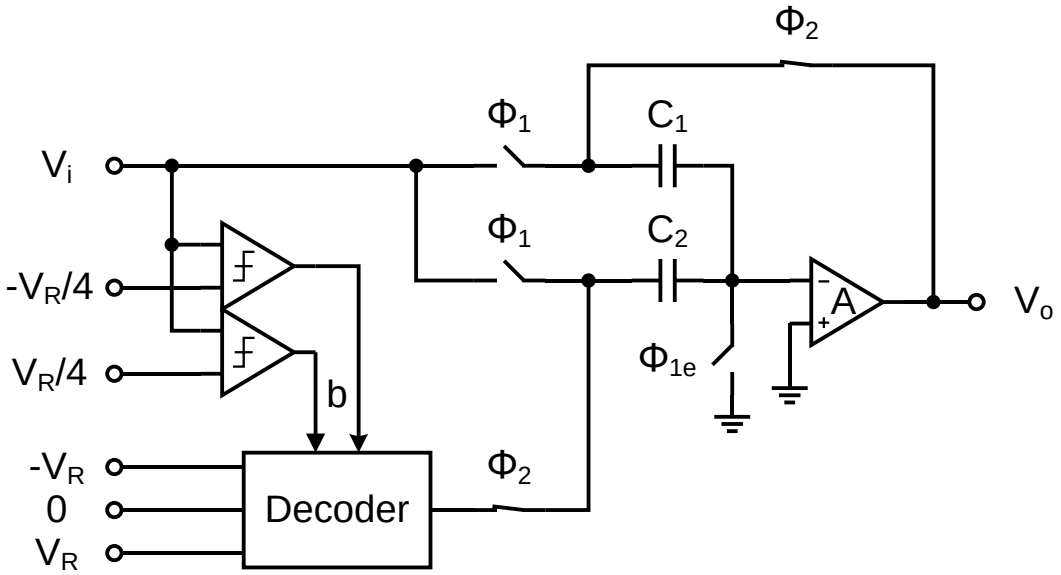
Pipelined ADC Architecture



A bucket brigade of algorithmic ADC w/ concurrent operation of all stages

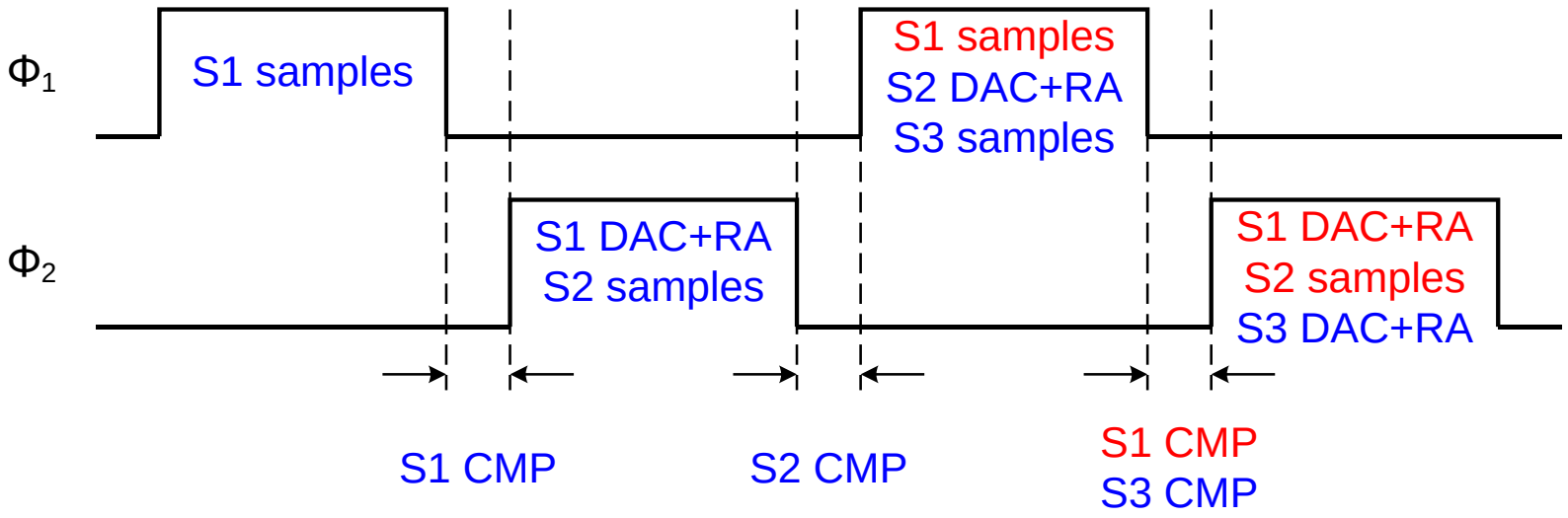
A 1.5-Bit Stage





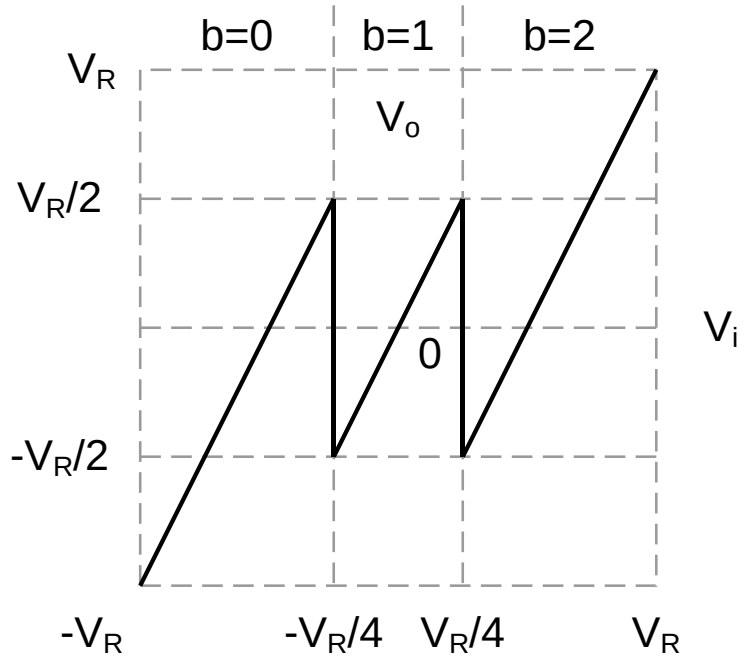
- 2X gain + 3-level DAC + subtraction all integrated
- Digital redundancy relaxes the tolerance on CMP/RA offsets

Timing Diagram of Pipelining



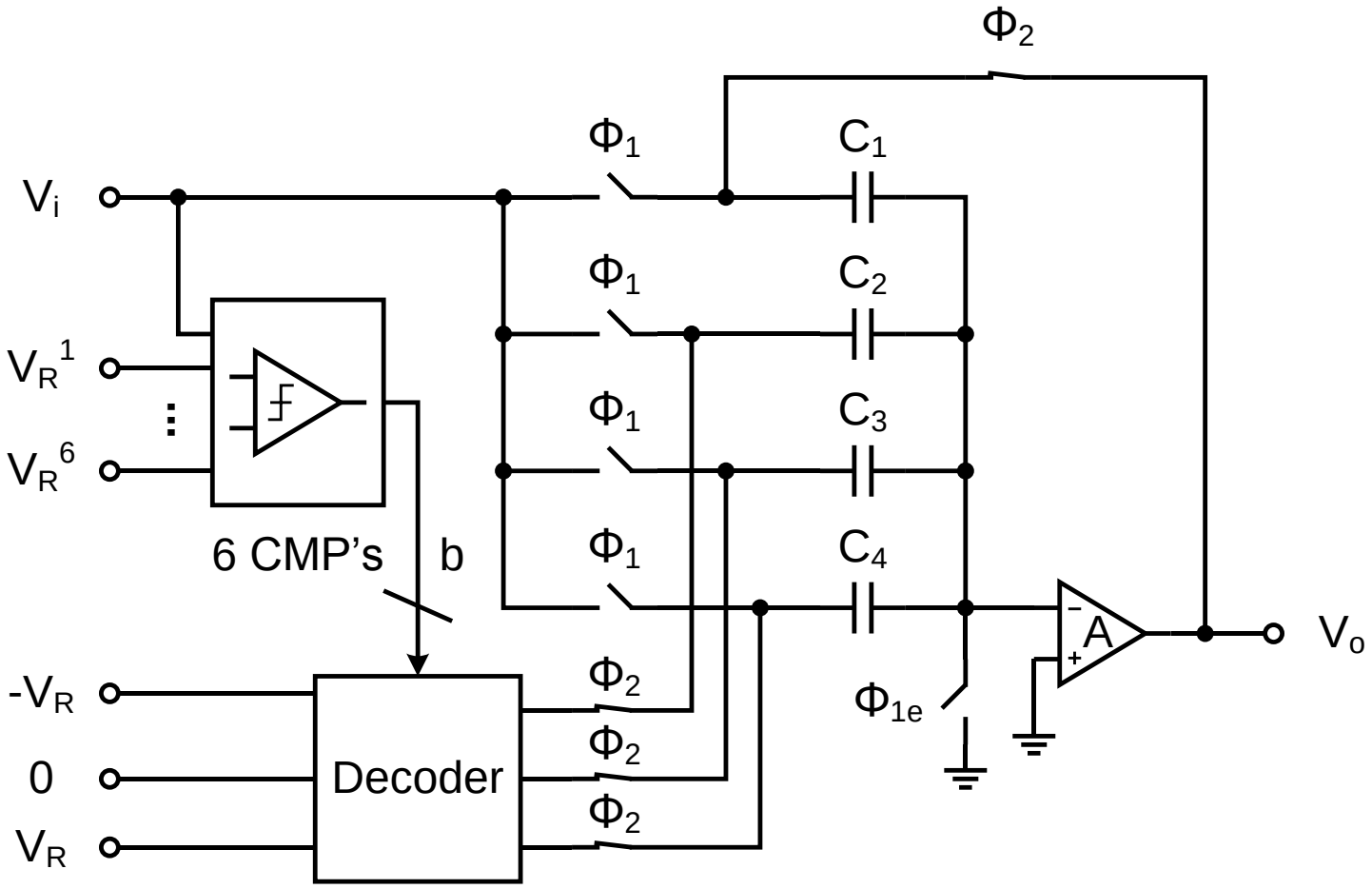
- Two-phase nonoverlapping clock is typically used, with the coarse ADCs operating within the nonoverlapping times
- All pipelined stages operate simultaneously, increasing throughput at the cost of latency (what is the latency of pipeline? 1 T?)

1.5-Bit Decoding Scheme

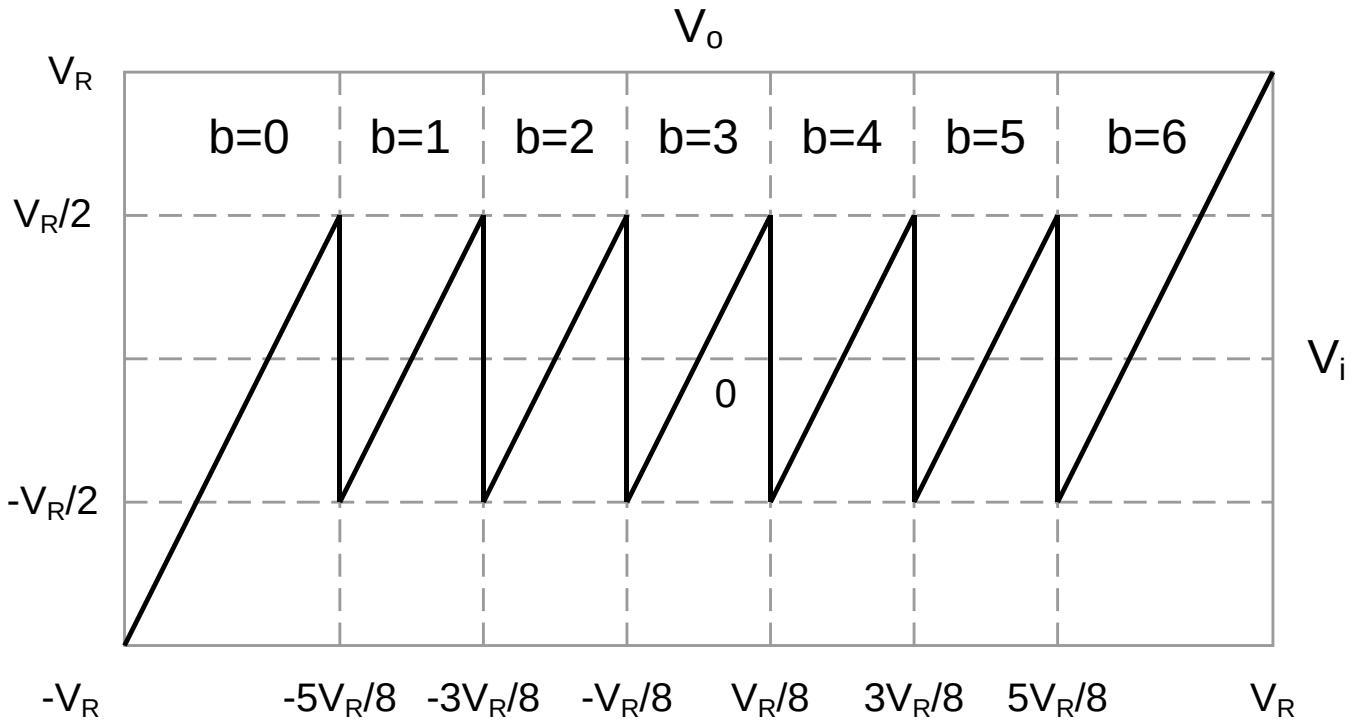


b	0	1	2
b-1	-1	0	+1
C_2	$+V_R$	0	$-V_R$

A 2.5-Bit Stage



2.5-Bit RA Transfer Curve



- 6 comparators + 7-level DAC are required
- Max tolerance on comparator offset is $\pm V_R/8$

2.5-Bit Decoding Scheme

b	0	1	2	3	4	5	6
b-3	-3	-2	-1	0	+1	+2	+3
b_1	-1	-1	-1	0	+1	+1	+1
b_2	-1	-1	0	0	0	+1	+1
b_3	-1	0	0	0	0	0	+1
C_2	$+V_R$	$+V_R$	$+V_R$	0	$-V_R$	$-V_R$	$-V_R$
C_3	$+V_R$	$+V_R$	0	0	0	$-V_R$	$-V_R$
C_4	$+V_R$	0	0	0	0	0	$-V_R$

- 7-level DAC, 3×3×3 = 27 permutations of potential configurations → multiple choices of decoding schemes!
- Choose the scheme to minimize decoding effort, balance loading for reference lines, etc.

Pipelined ADC

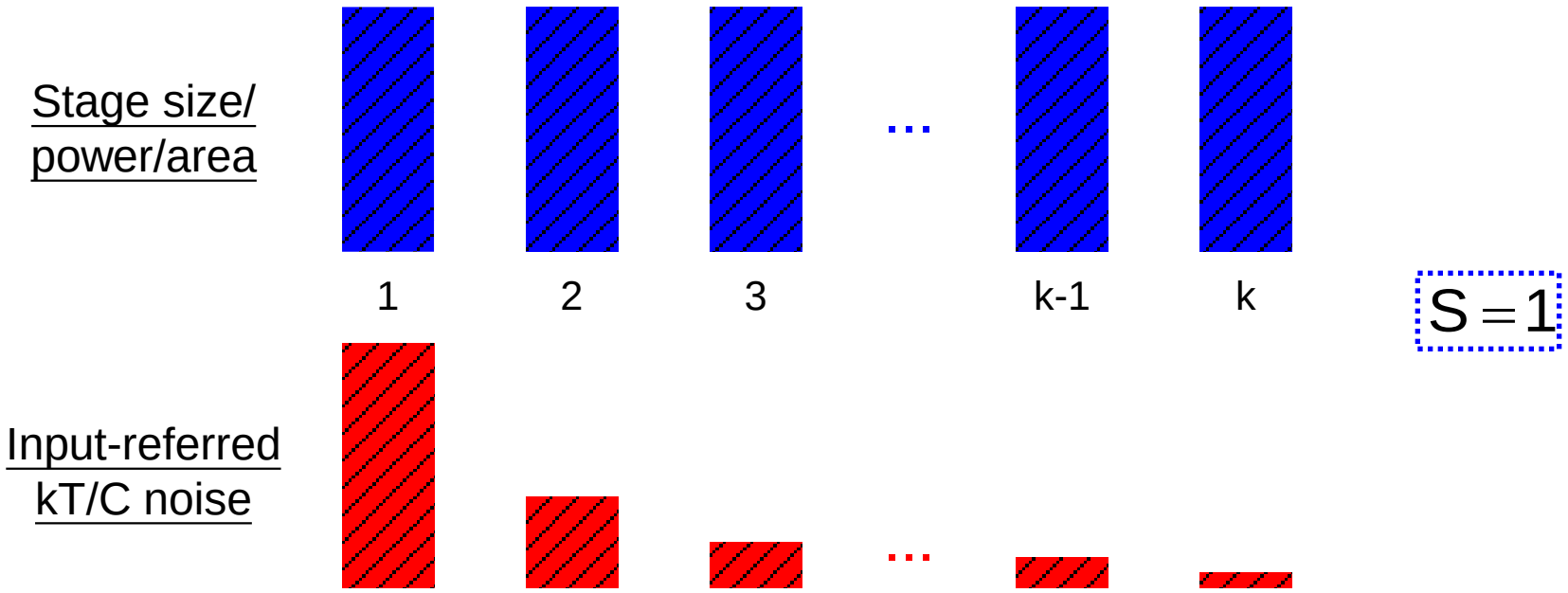
Features

- Architecture complexity is proportional to the resolution $N = \Sigma n_j$
- Throughput is significantly improved relative to algorithmic or SAR
- Digital redundancy works the same way as algorithmic
- Inter-stage gain enables stage scaling to save power and area

Limitations

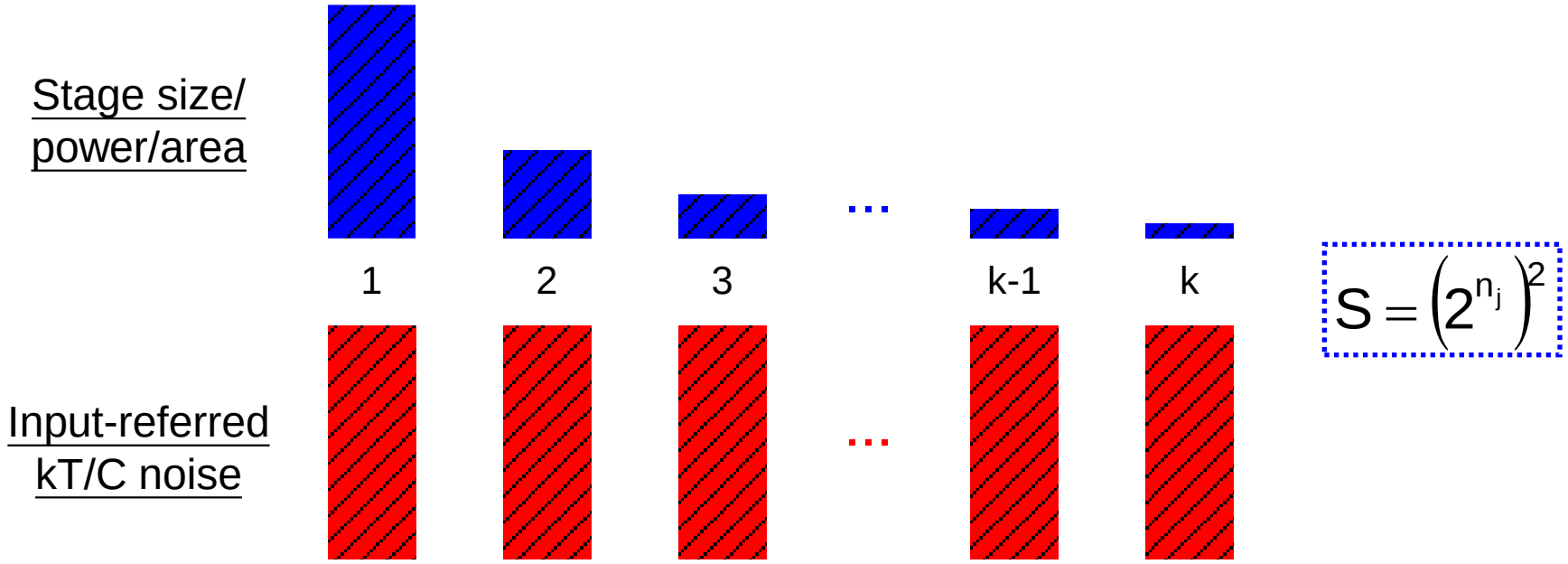
- Typically 3 conversion operations are involved
  - Sample-and-hold
  - Sub-ADC comparison
  - Sub-DAC and residue generation
- High-gain op-amps are required to produce residue signals with certain accuracy, which limits the conversion speed
- Long latency may be problematic for certain applications

No Stage Scaling



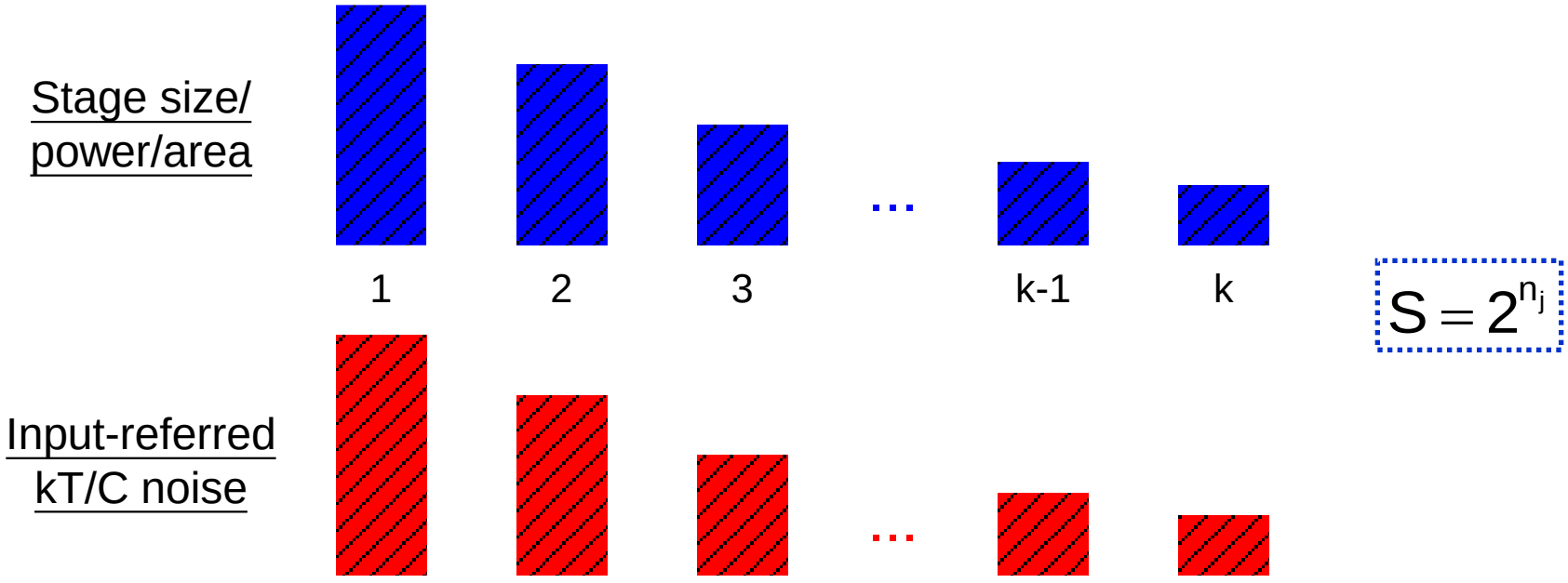
- All stages identically sized – same capacitors, op-amps, comparators
- Later stages are clearly oversized due to inter-stage gains

Aggressive Stage Scaling



- Stages sized such that the input-referred noises are identical
- Later stages are clearly downsized too aggressively

Optimum Stage Scaling



Optimum scaling lies in between the two extremes → $S \approx 2^{n_j}$

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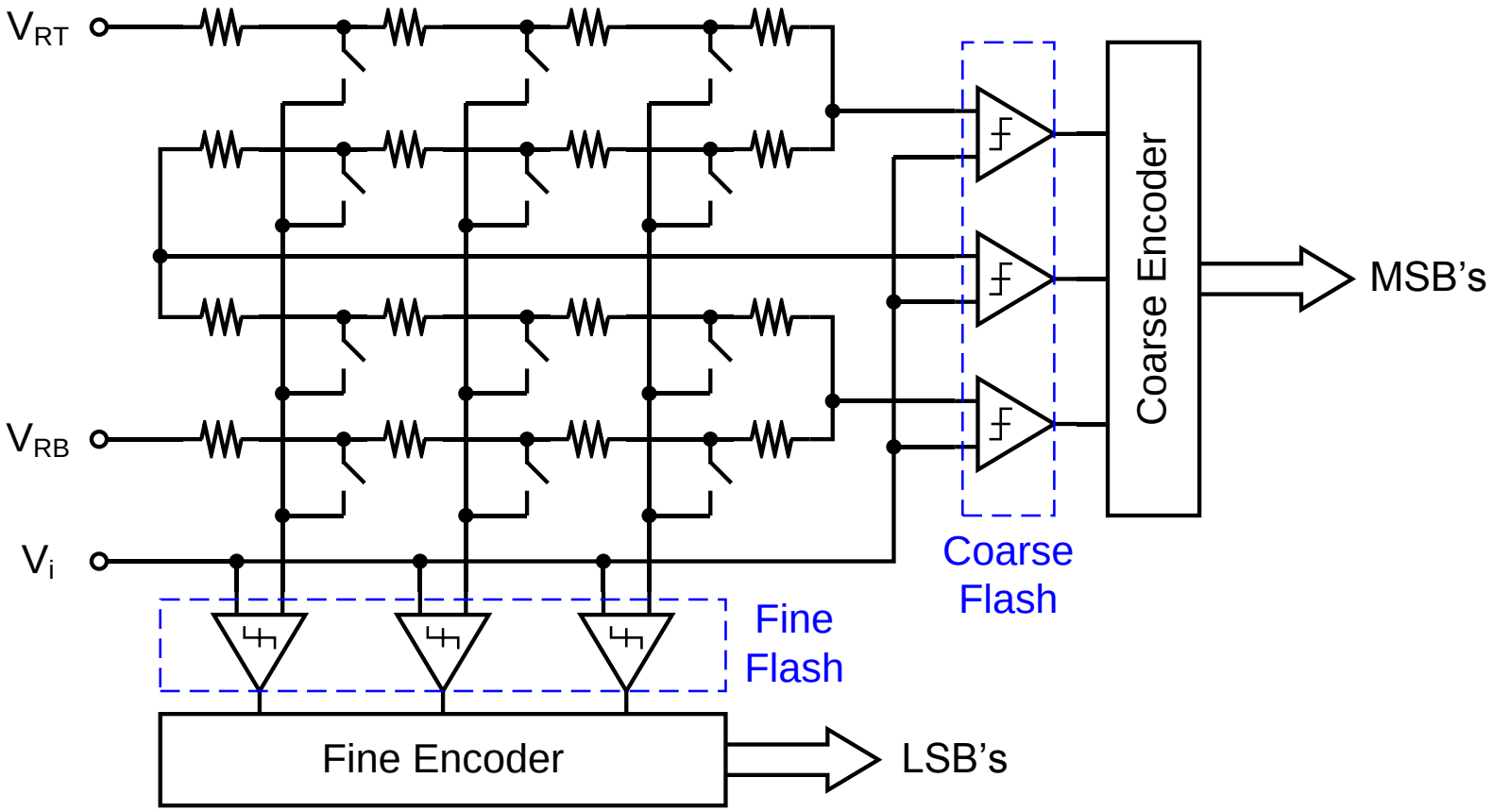
Subranging ADC Architecture



Subranging ADC

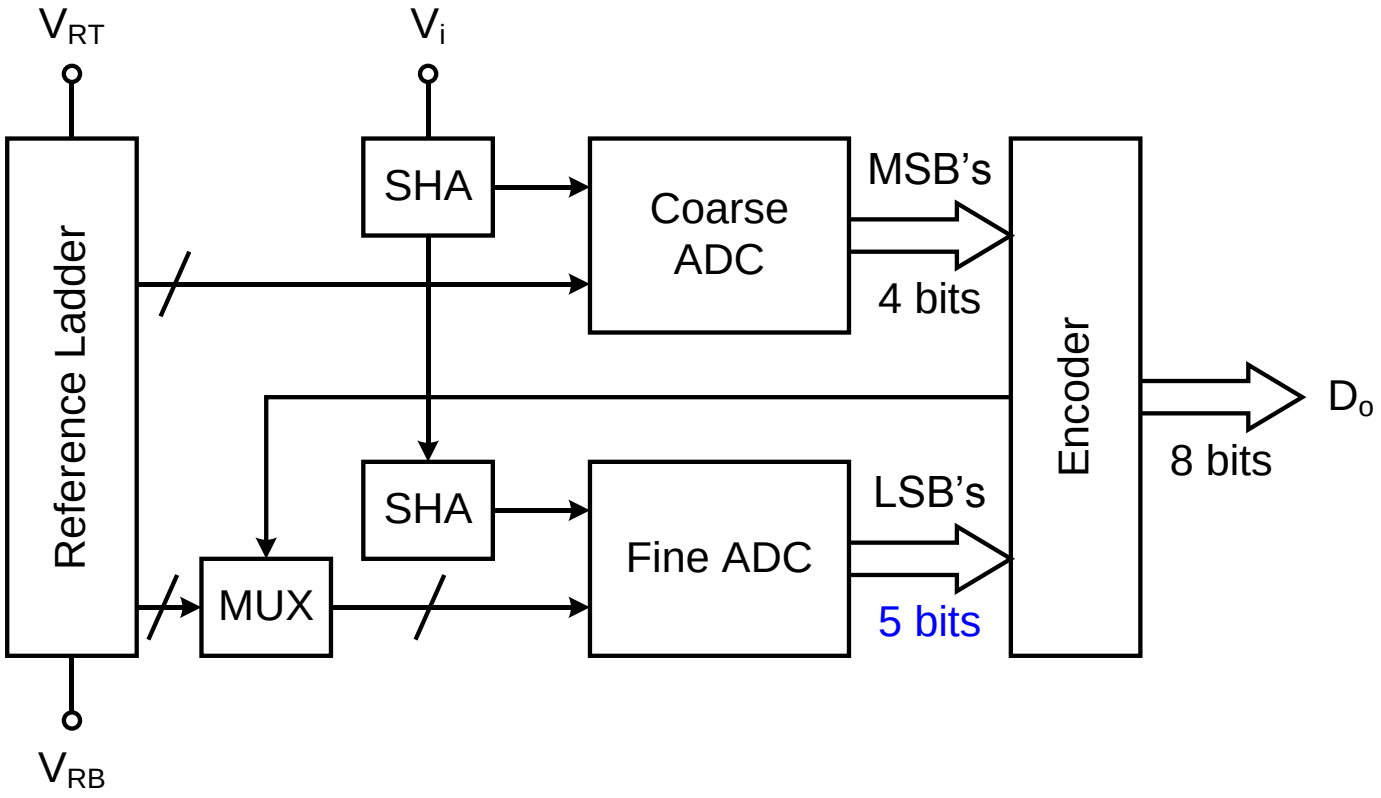
Features

- Reduced complexity – $2 \cdot (2^{N/2}-1)$ comparators – relative to flash
- Reduced C_{in}, area, and power consumption
- No residue amplifier required (compare to pipelined ADC)

Limitations

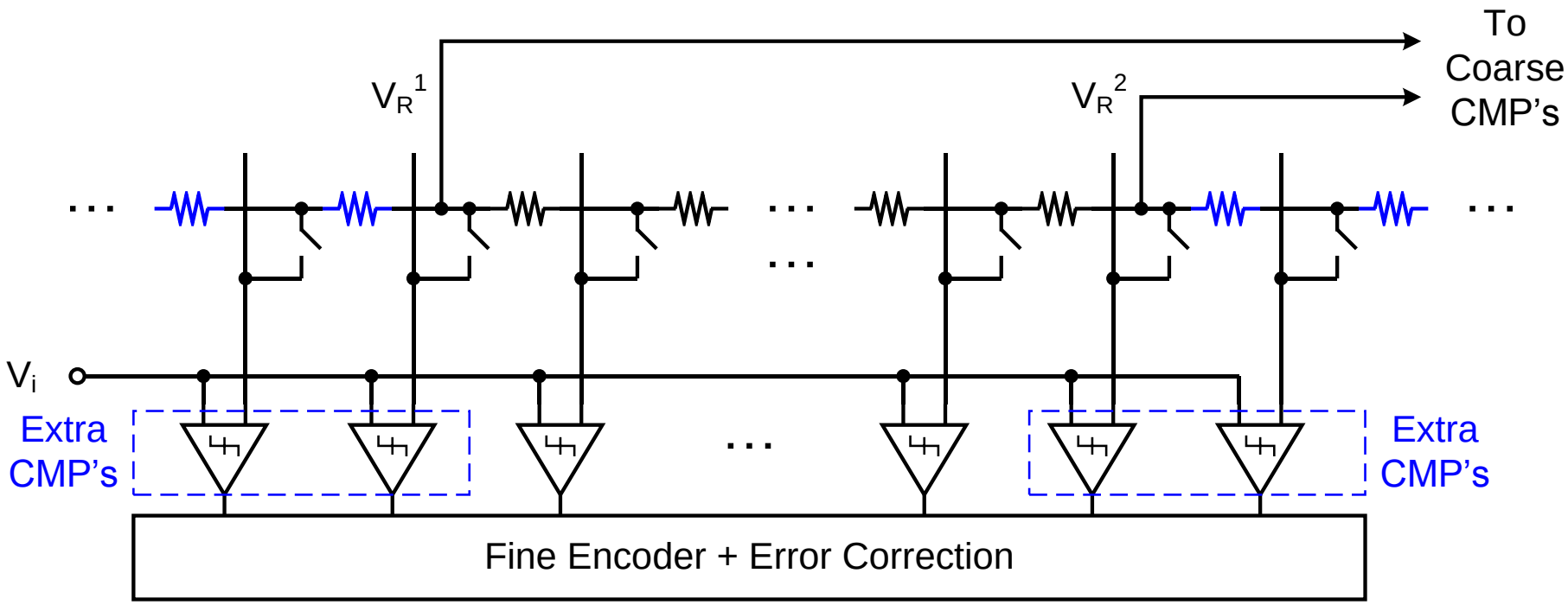
- Typically 3 clock phases per conversion
  - Sample
  - Coarse comparison
  - Fine comparison
- Typically two SHAs are required for the coarse and fine ADCs
- Fine comparator offset must be controlled to N-bit level
- Offset tolerance on coarse comparators can be relaxed with digital redundancy

Typical Subranging Block Diagram



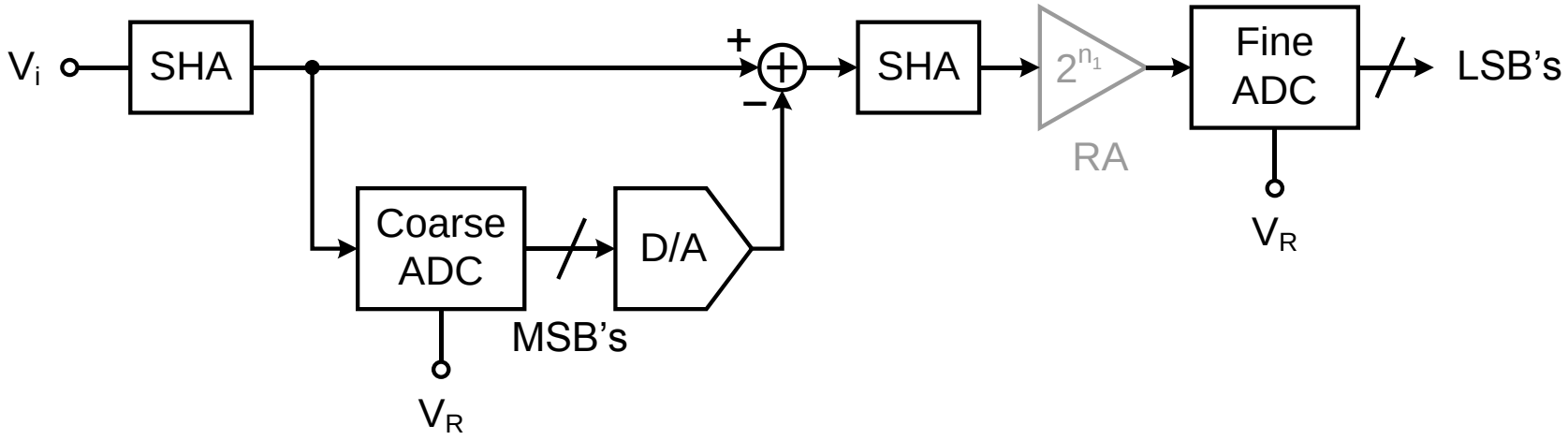
Redundancy in fine ADC provided by over- and under-range comparators

Digital Redundancy in Fine ADC



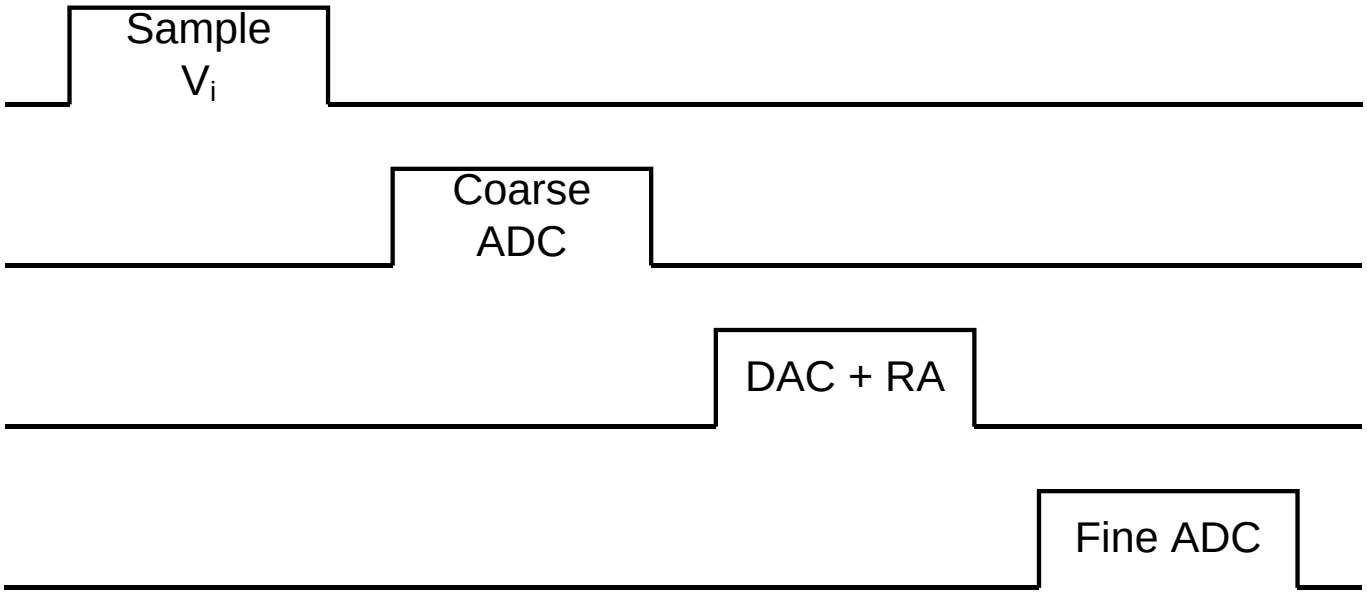
The range of fine search extended on both sides

Two-Step Subranging/Pipelined ADC



- Coarse-fine two-step subranging architecture
- Conversion residue produced instead of switching reference taps
- Residue gain can be provided to relax offset tolerance in fine ADC
- Very similar to the pipelined architecture

Timing Diagram



- Four conversion steps can be pipelined (needs op-amp)
- Usually DAC + RA settling consumes most of the conversion time
- Residue gain of unity is often used to speed up conversion

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