CHAPTER 7

Digital to Analog Converter

Outline

- 7.1 Introduction
- 7.2 DAC Characteristic
- 7.3 Binary-Weighted DAC
- 7.4 Unit-Element DAC
- 7.5 Segmented DAC

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DAC Architecture

- Nyquist DAC architectures
  - Binary-weighted DAC
  - Unit-element (thermometer-coded) DAC
  - Segmented DAC
  - Resistor-string, current-steering, charge-redistribution DACs
- Oversampling DAC
  - Oversampling performed in digital domain (zero stuffing)
  - Digital noise shaping ($\Sigma\Delta$ modulator)
  - 1-bit DAC can be used
  - Analog reconstruction/smoothing filter

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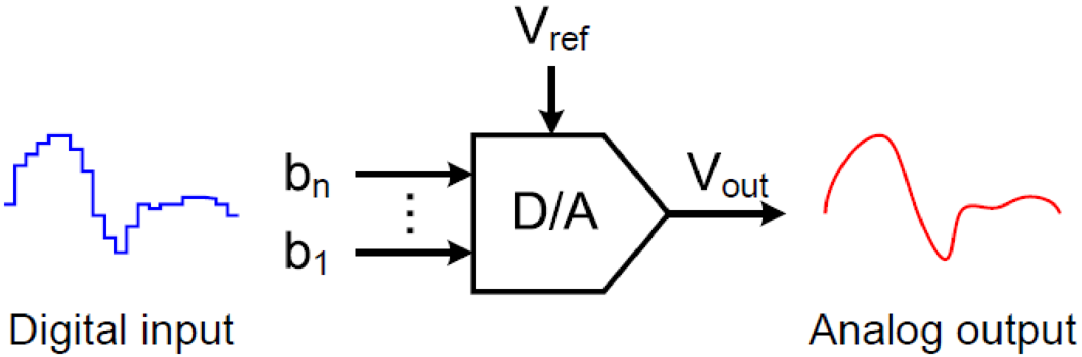
DAC Characteristics

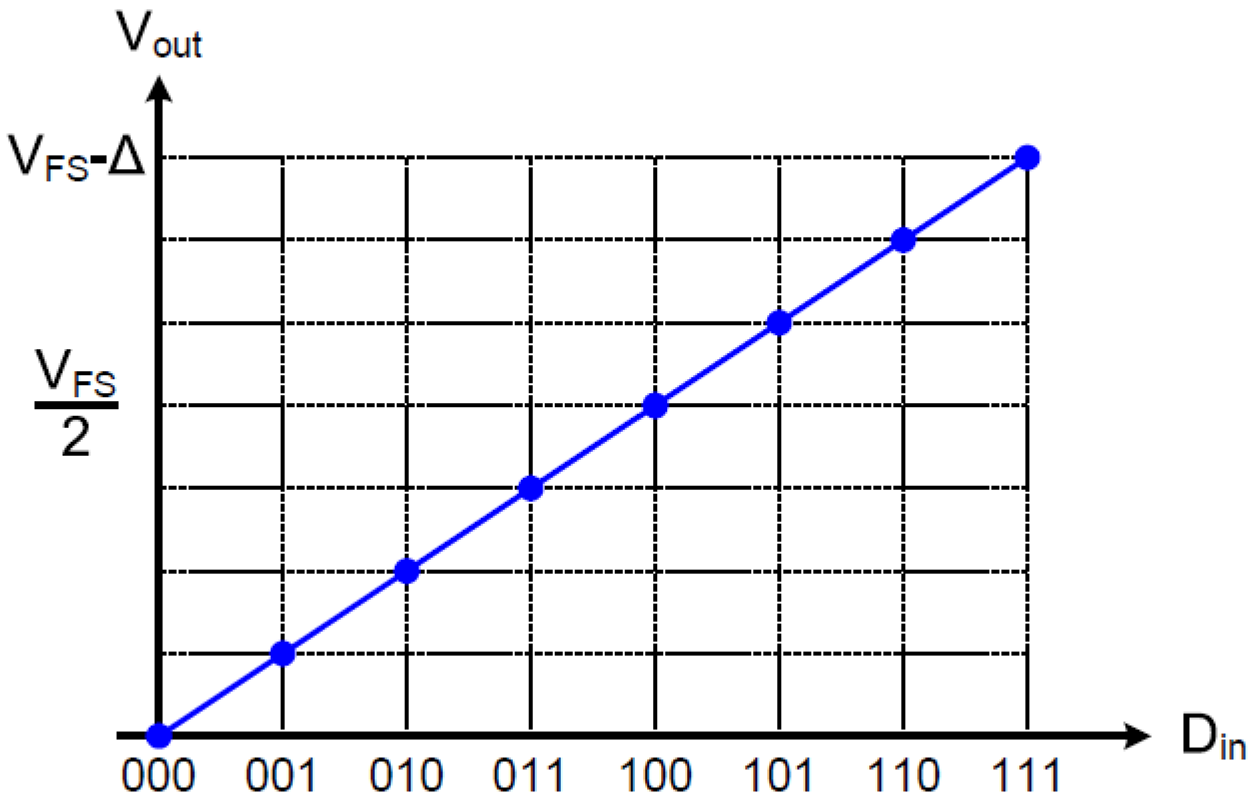


- N = # of bits
- V_{FS} = Full-scale range
- $\Delta = V_{FS}/2^N$ = 1LSB
- b_i = 0 or 1

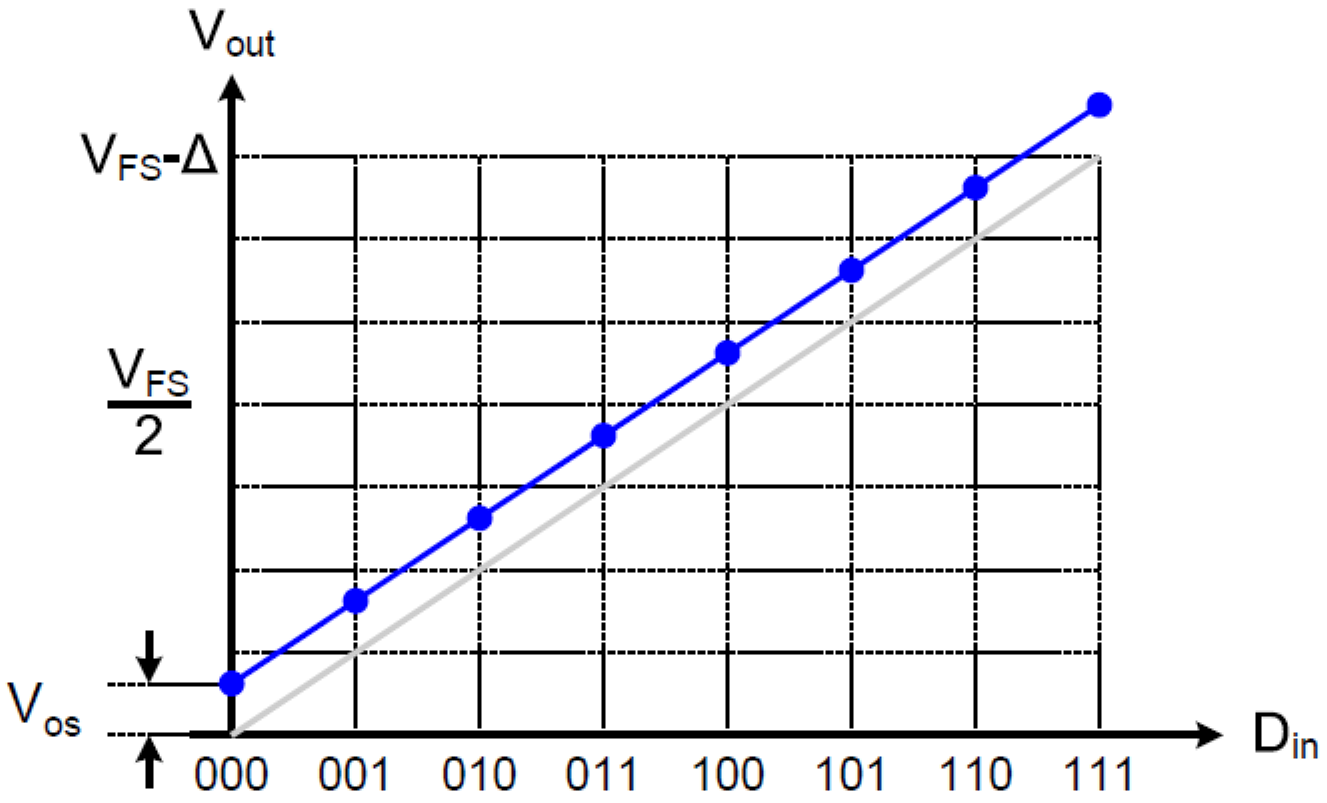
$$\boxed{V_{out} = V_{FS} \cdot \sum_{i=0}^{N-1} \frac{b_i}{2^{N-i}} = \Delta \cdot \sum_{i=0}^{N-1} b_i \cdot 2^{-i}}$$

<u>Note</u>: V_{out} ($b_i = 1$, for all i) $= V_{FS} - \Delta = V_{FS}(1-2^{-N}) \neq V_{FS}$

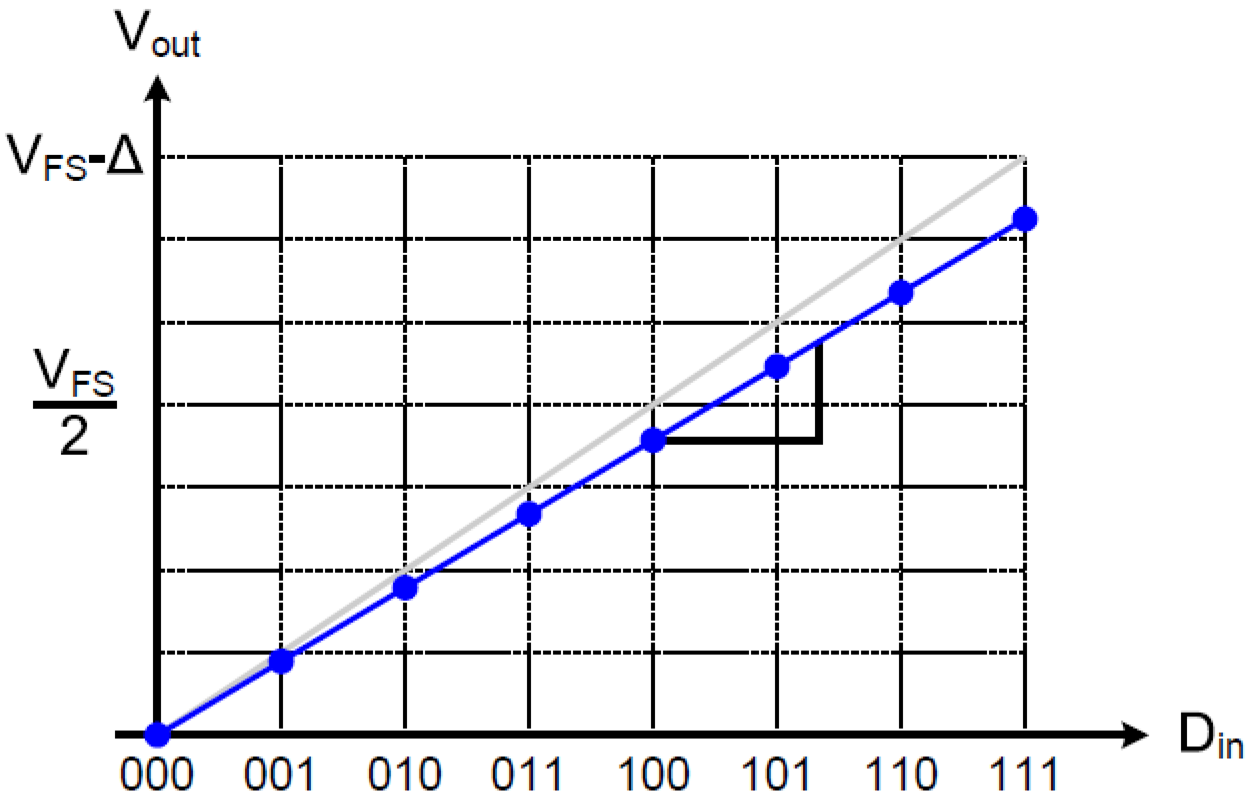
Ideal DAC Transfer Curve



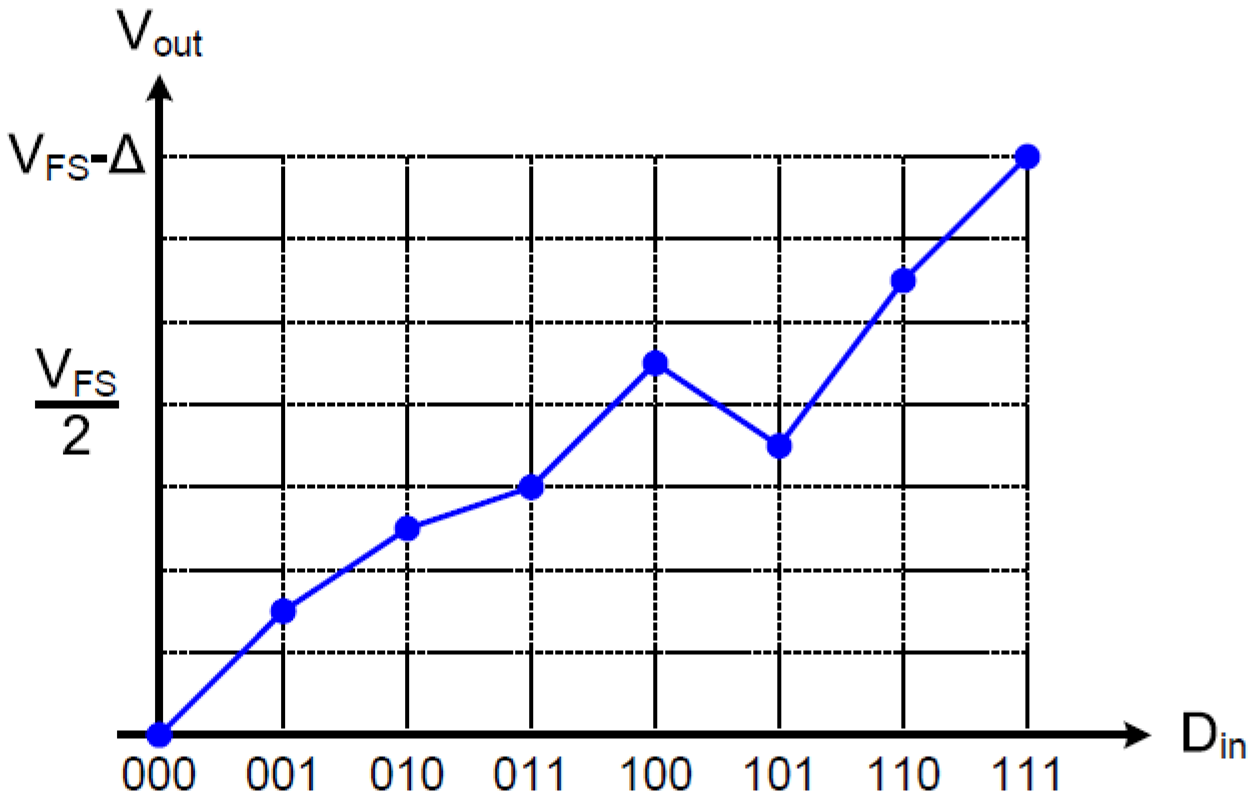
Offset



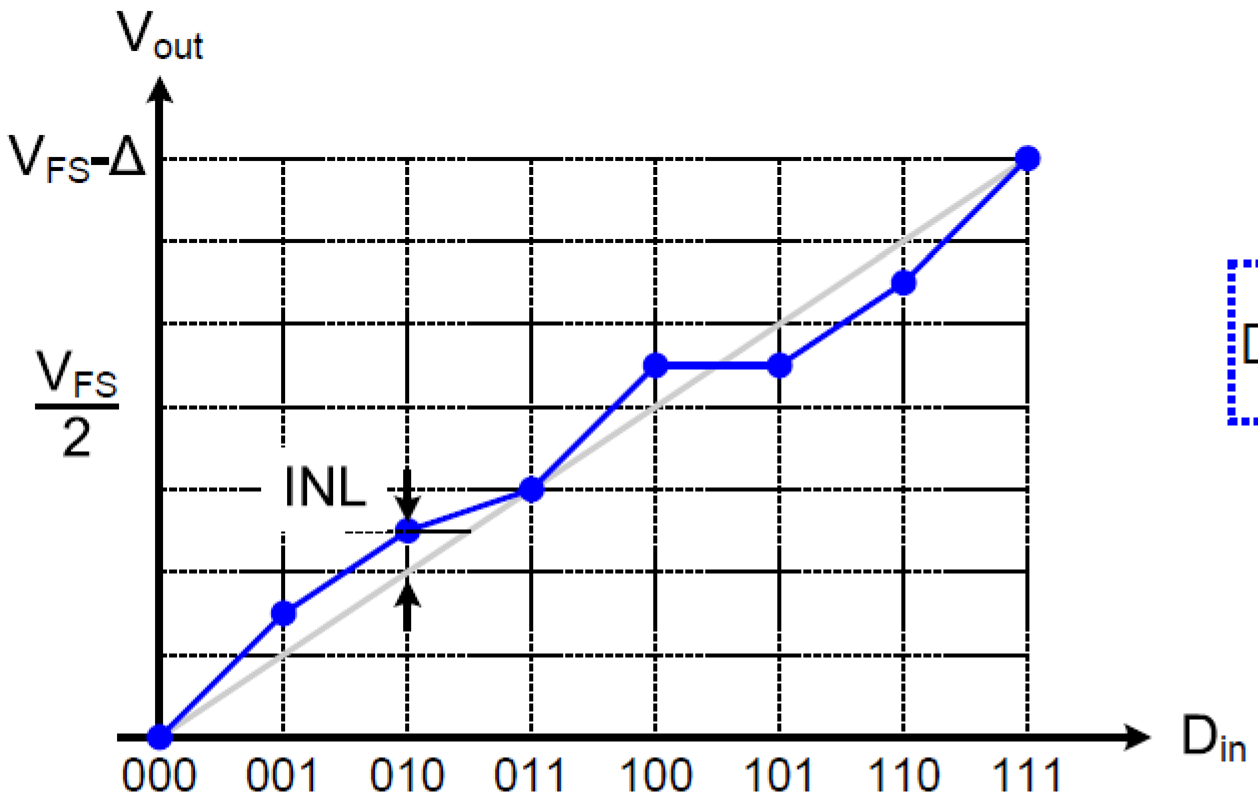
Gain Error



Monotonicity



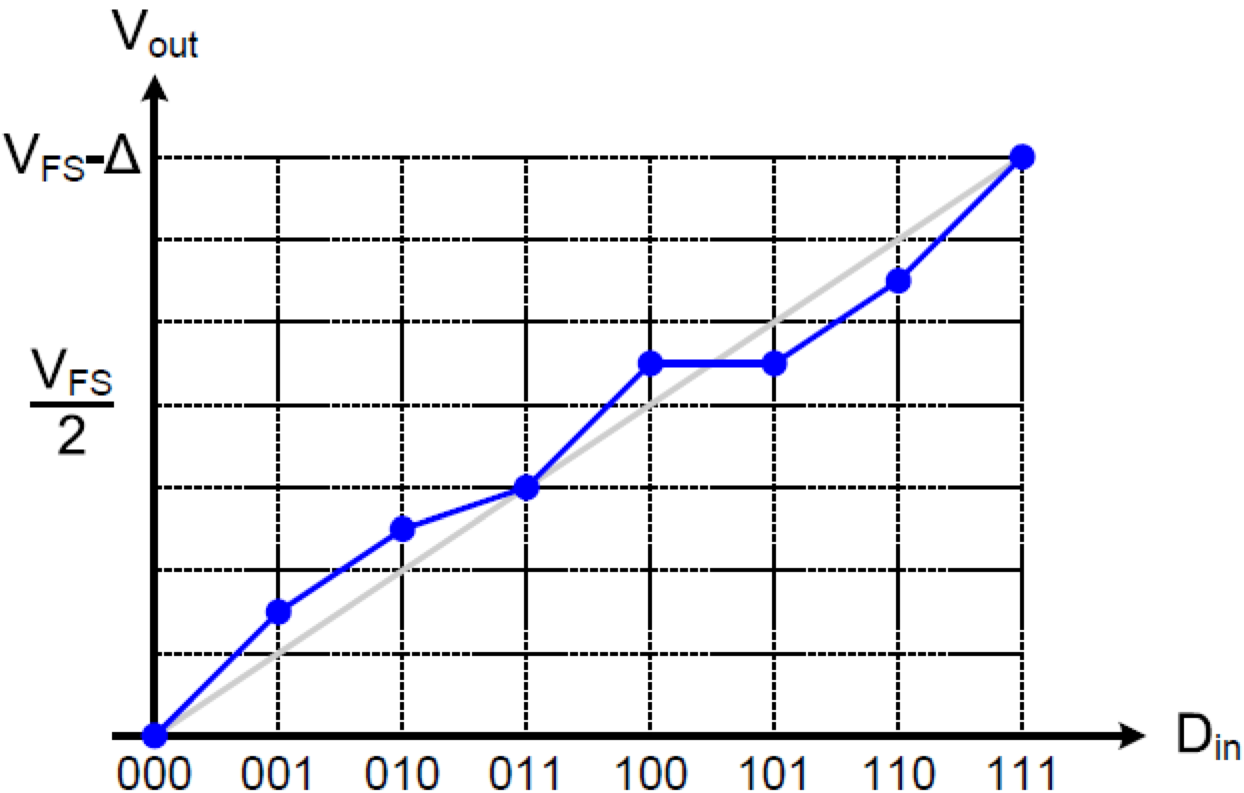
Differential and Integral Nonlinearity



$$DNL_i = \frac{i^{th}\ \text{Step Size} - \Delta}{\Delta}$$

- DNL = deviation of an output step from 1 LSB (= Δ = $V_{FS}/2^N$)
- INL = deviation of the output from the ideal transfer curve

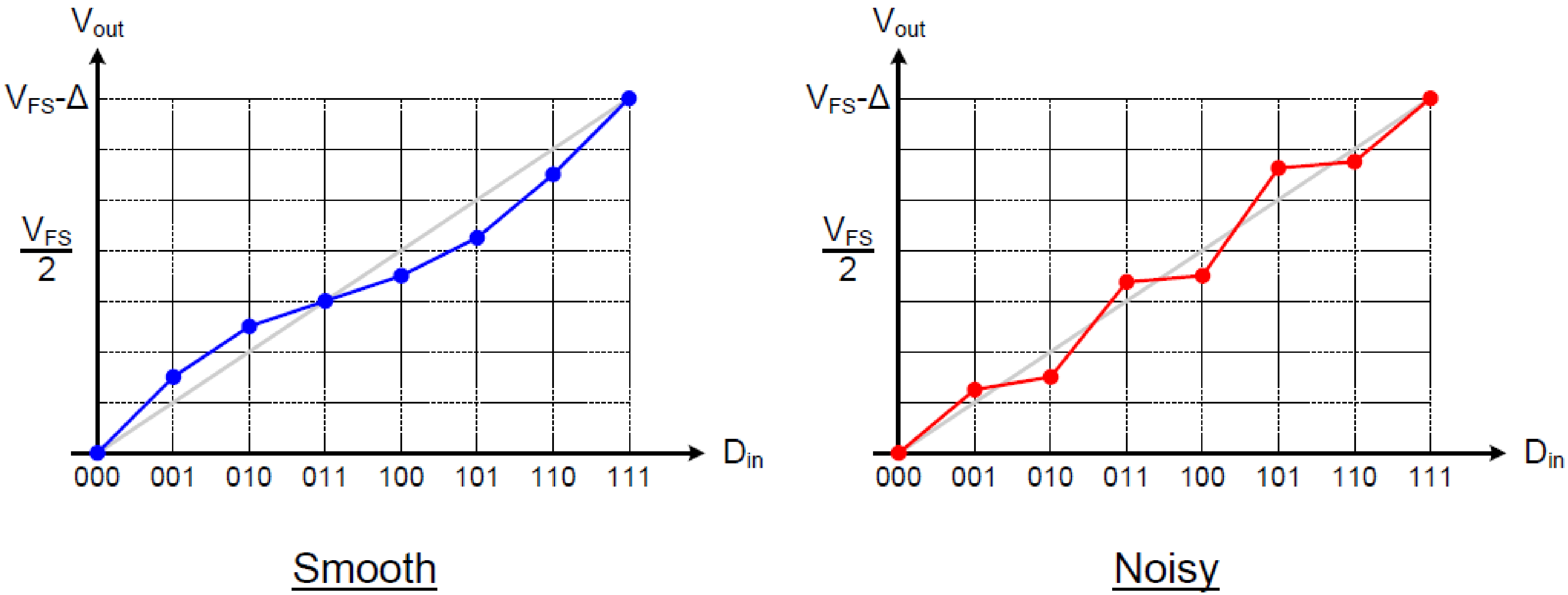
DNL and INL



$$INL_i = \sum_{j=0}^{i} DNL_j$$

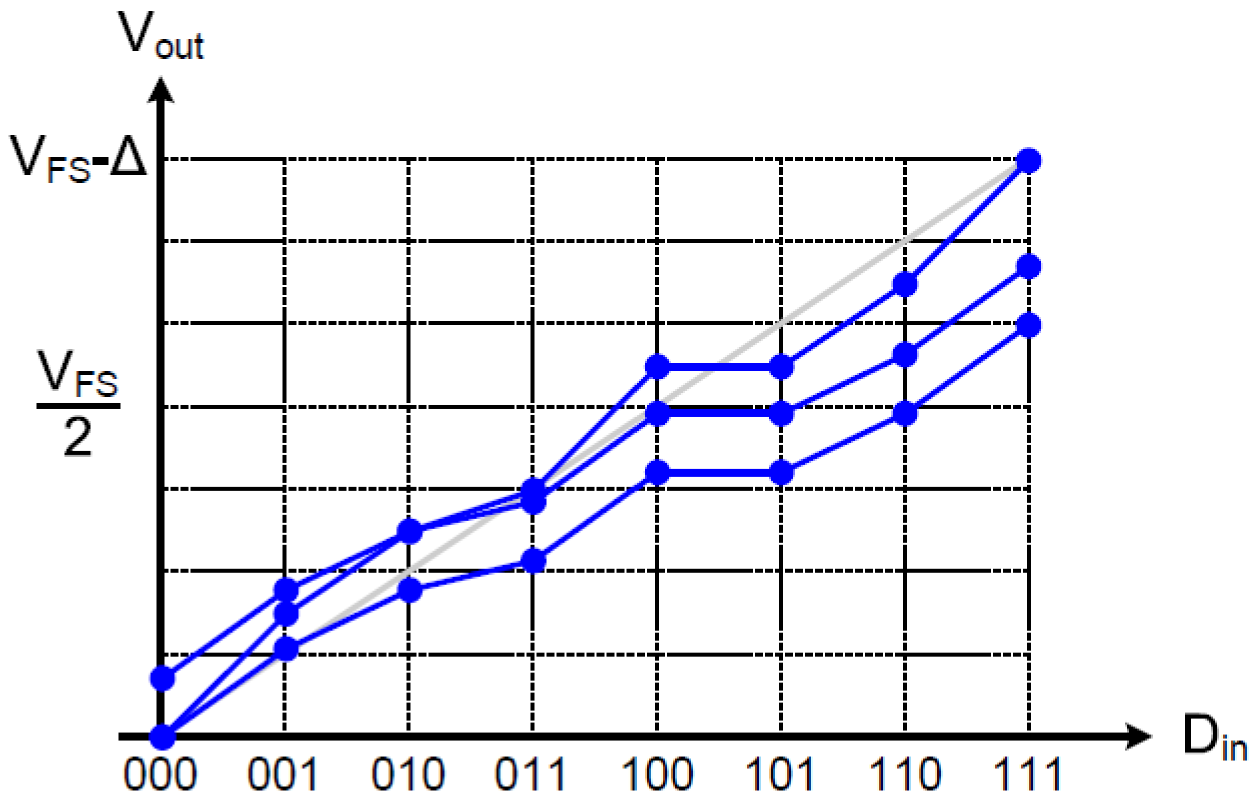
INL = cumulative sum of DNL

DNL and INL



- DNL measures the uniformity of quantization steps, or incremental (local) nonlinearity; small input signals are sensitive to DNL.
- INL measures the overall, or cumulative (global) nonlinearity; large input signals are often sensitive to both INL (HD) and DNL (QE).

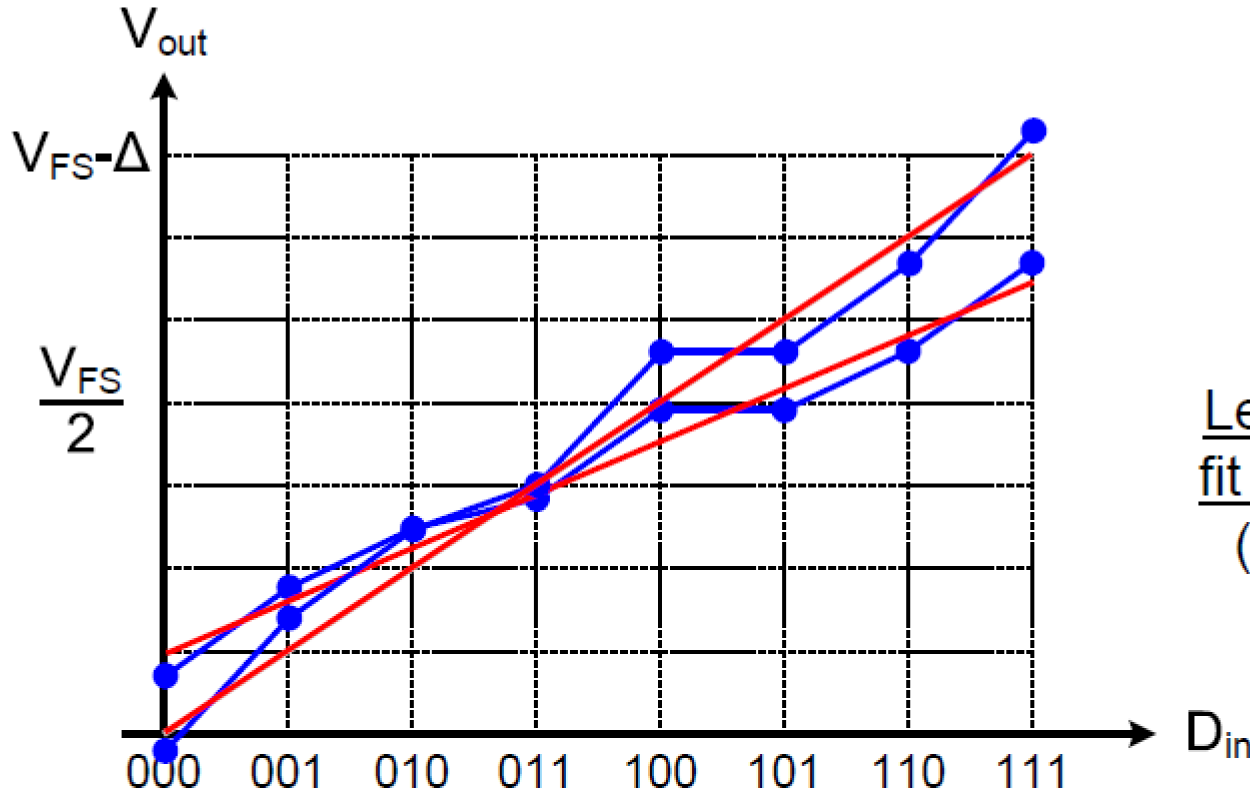
Measure DNL and INL (Method 1)



Endpoint stretch

Endpoints of the transfer characteristic are always at 0 and V_{FS}-Δ

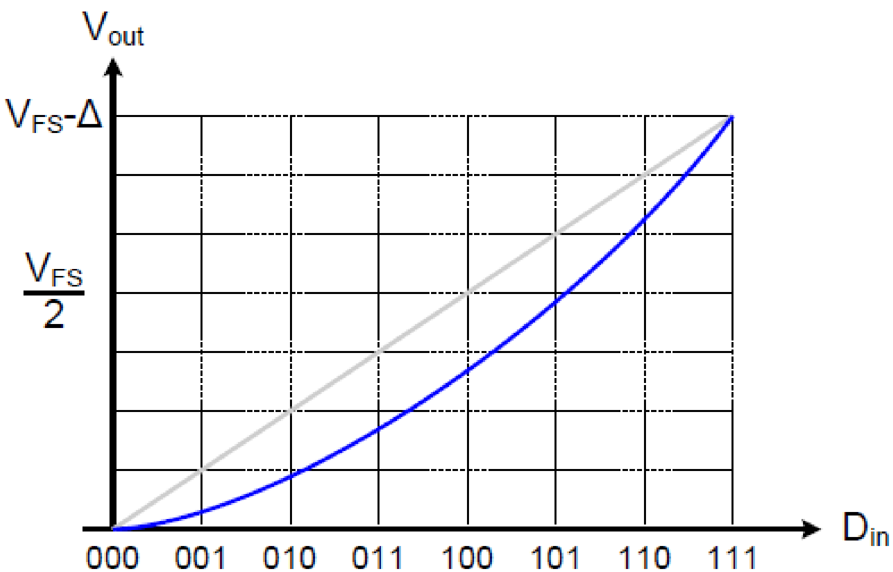
Measure DNL and INL (Method 2)

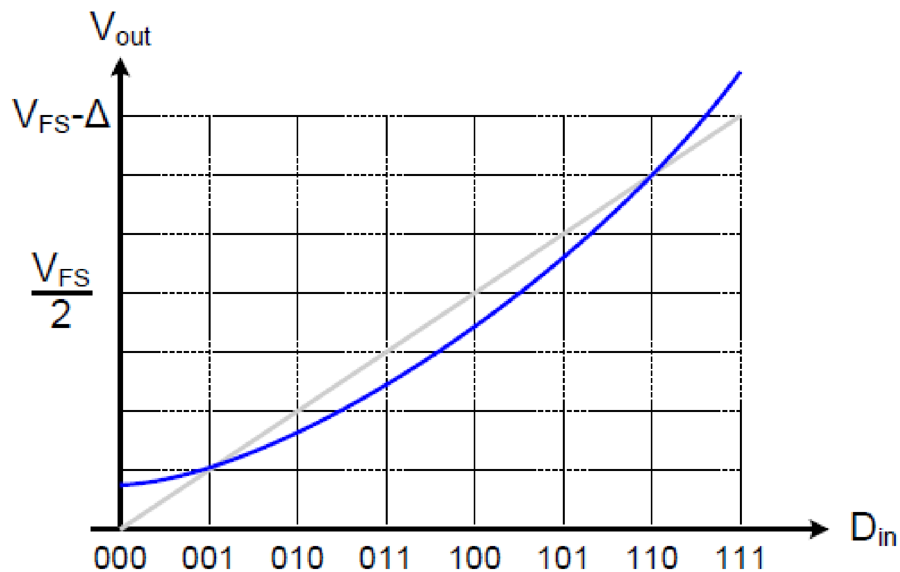


Least-square fit and stretch ("detrend")

Endpoints of the transfer characteristic may not be at 0 and V_{FS}-Δ

Measure DNL and INL





Method I (endpoint stretch)

$\Sigma(\text{INL}) \neq 0$

Method II (LS fit & stretch)

$\Sigma(\text{INL}) = 0$

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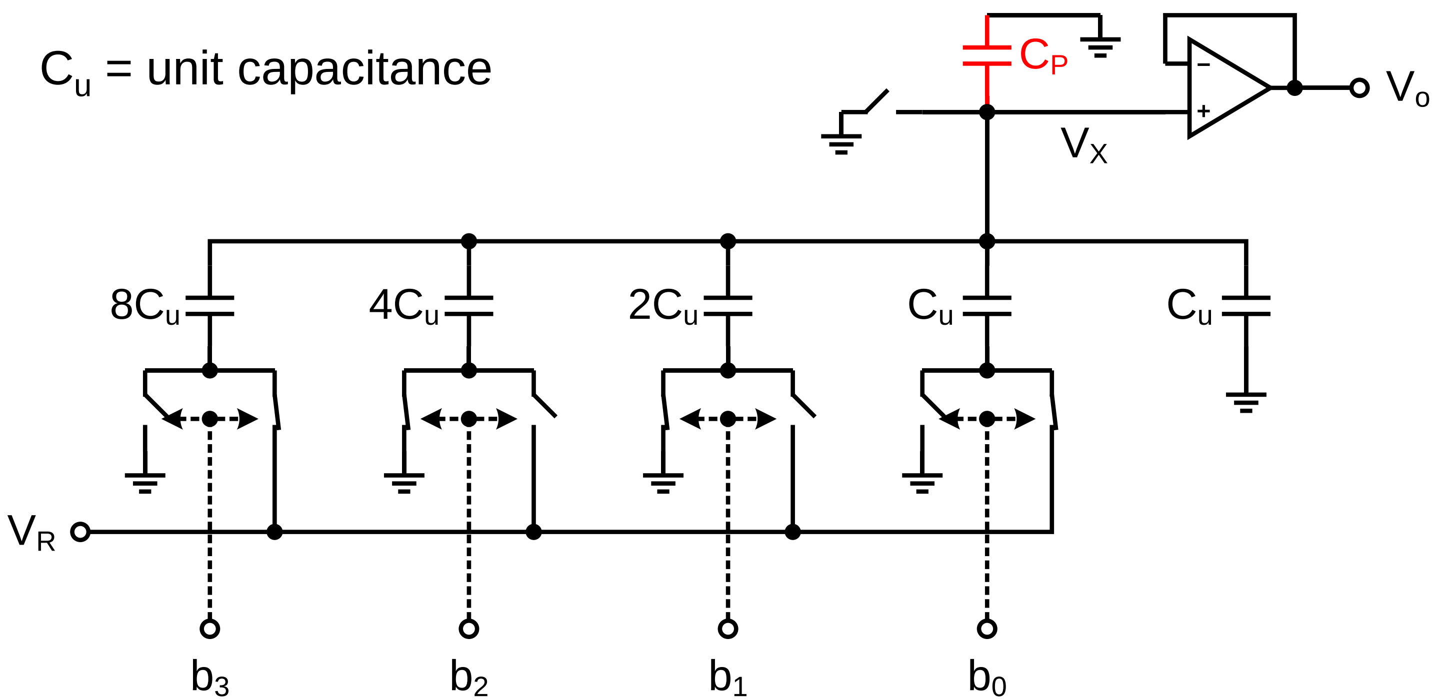
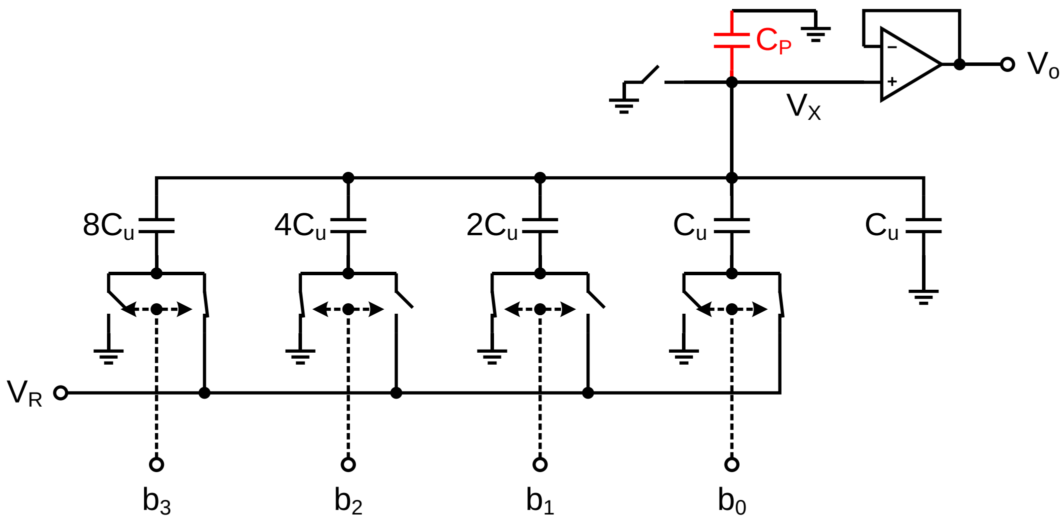
Binary-Weighted CR DAC



- Binary-weighted capacitor array → most efficient architecture
- Bottom plate @ V_R with b_j = 1 and @ GND with b_j = 0

Binary-Weighted CR DAC



$$V_o = \left(\frac{\sum_{j=1}^{N} b_{N-j} \cdot 2^{N-j} C_u}{C_p + C_u + \sum_{j=1}^{N} 2^{N-j} C_u} \right) \cdot V_R$$

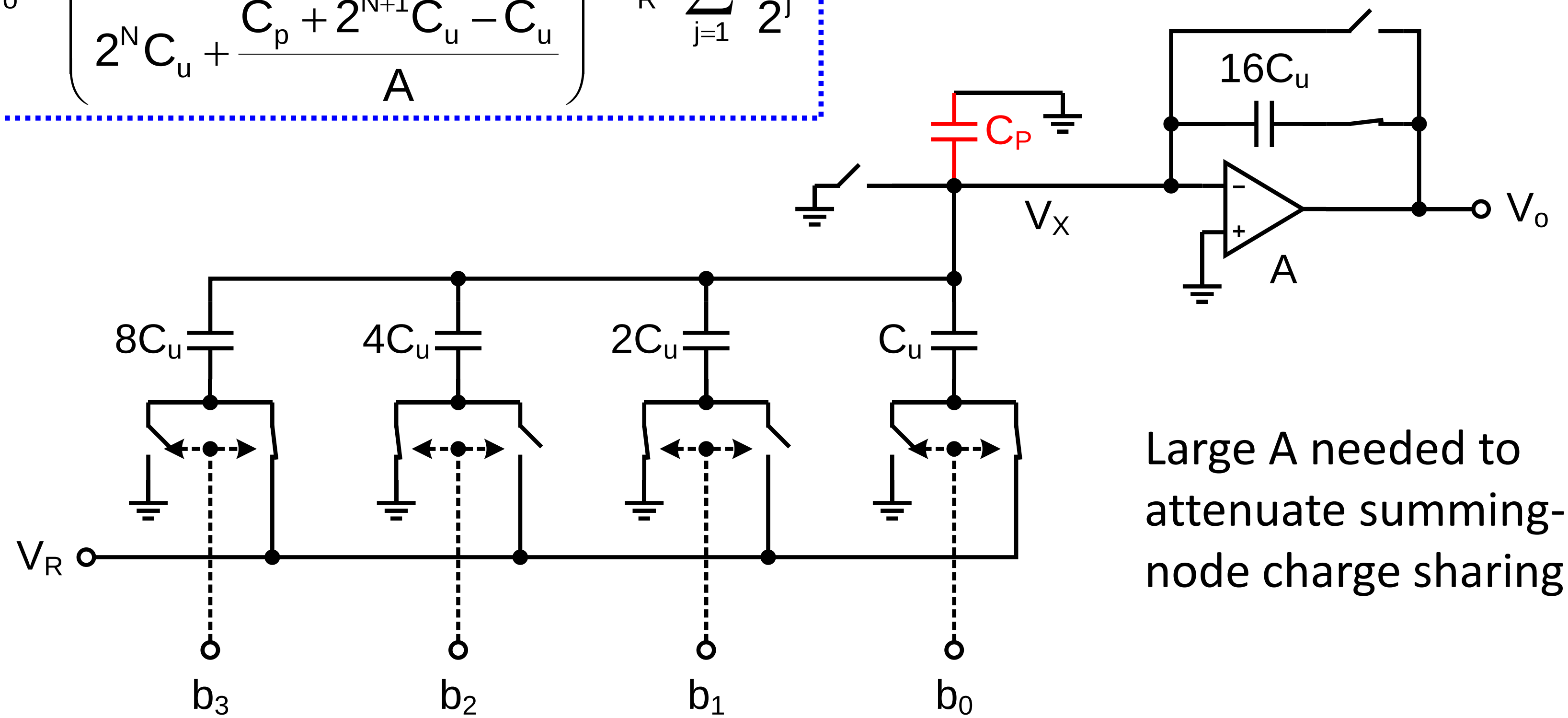
$$= \left(\frac{\sum_{j=1}^{N} b_{N-j} \cdot 2^{N-j} C_u}{C_p + 2^N C_u} \right) \cdot V_R$$

$$\boxed{V_o = \left(\frac{2^N C_u}{C_p + 2^N C_u} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}}$$

- C_p → gain error (nonlinearity if C_p is nonlinear)
- INL and DNL limited by capacitor array mismatch

Stray-Insensitive CR DAC

$$V_o = \left(\frac{2^N C_u}{2^N C_u + \dfrac{C_p + 2^{N+1} C_u - C_u}{A}} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



Large A needed to attenuate summing-node charge sharing

MSB Transition

Code 0111

$$V_o(0111) = \left(\frac{C_1 + C_2 + C_3}{C_p + C + \sum_{j=1}^{4} 2^{4-j} C} \right) \cdot V_R$$

Code 1000

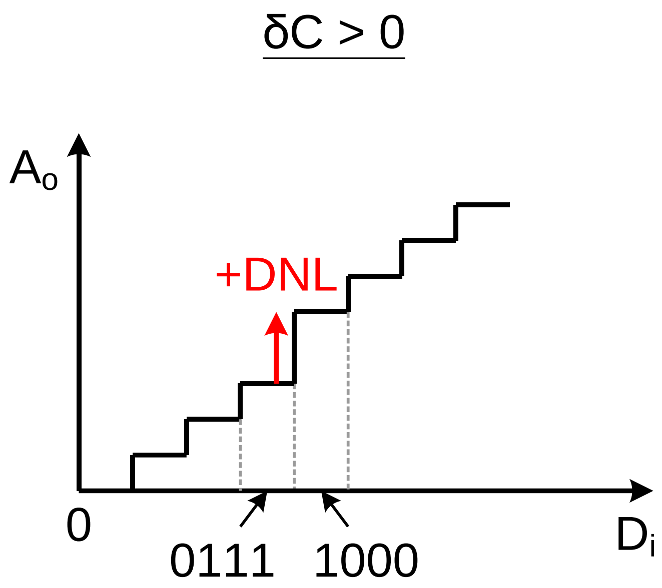
$$V_o(1000) = \left(\frac{C_4}{C_p + C + \sum_{j=1}^{4} 2^{4-j} C} \right) \cdot V_R$$

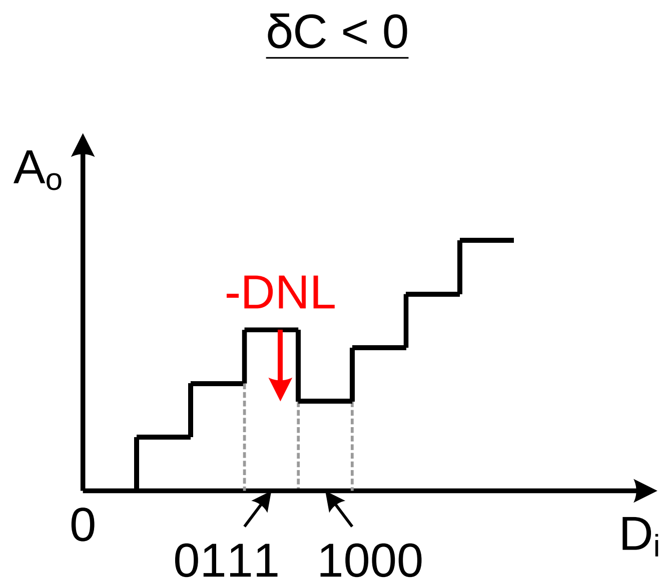
$$\text{Assume}: \ C_4 - (C_1 + C_2 + C_3) = C_u + \delta C,$$

$$\begin{aligned} \text{DNL} &= [V_o(1000) - V_o(0111) - 1\text{LSB}]/1\text{LSB} \\ &= \frac{\delta C}{\sum C} \Big/ \frac{C_u}{\sum C} = \delta C / C_u \end{aligned}$$

Largest DNL error occurs at the midpoint where MSB transitions, determined by the mismatch between the MSB capacitor and the rest of the array.

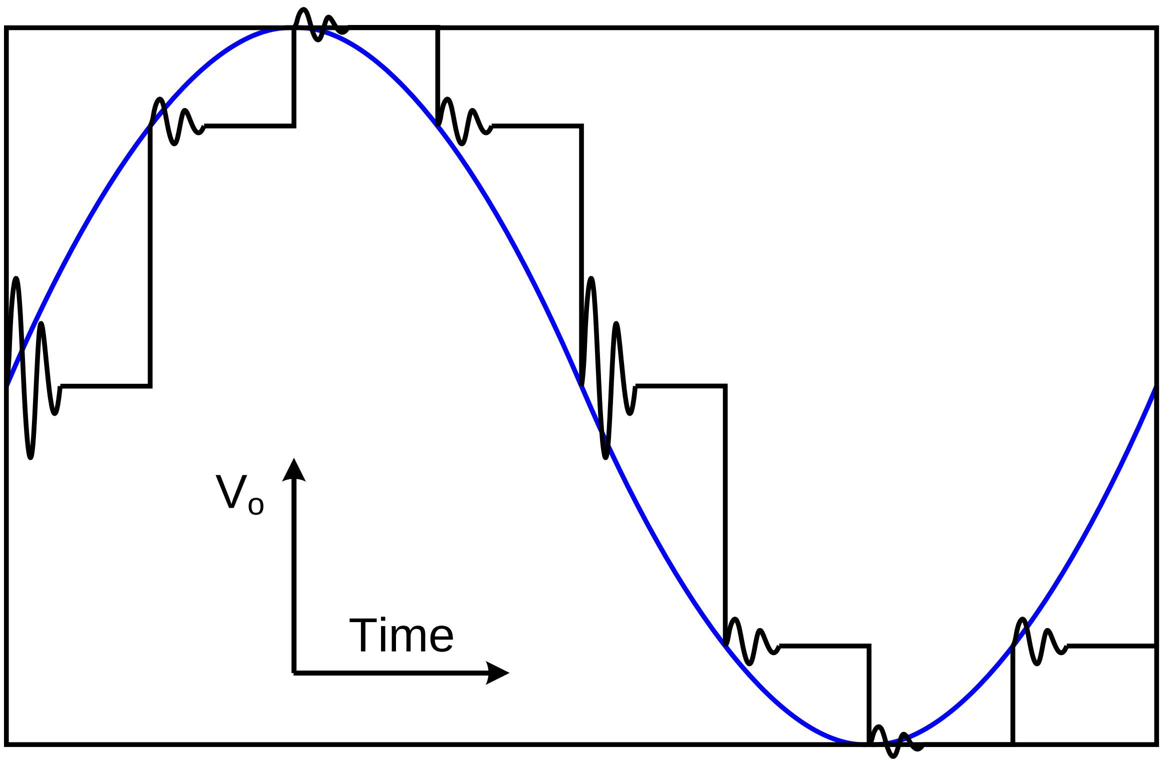
Midpoint DNL





- $\delta C > 0$ results in positive DNL
- $\delta C < 0$ results in negative DNL or even nonmonotonicity

Output Glitches

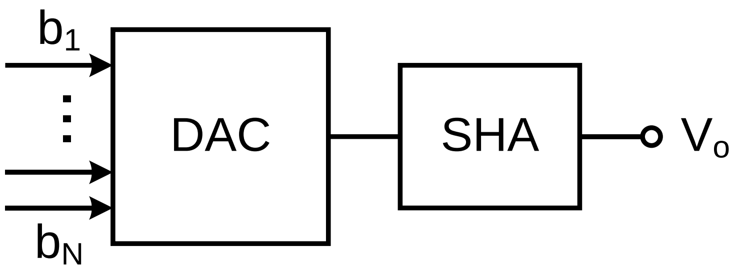


- Cause: Signal and clock skew in circuits
- Especially severe at MSB transition where all bits are switching –

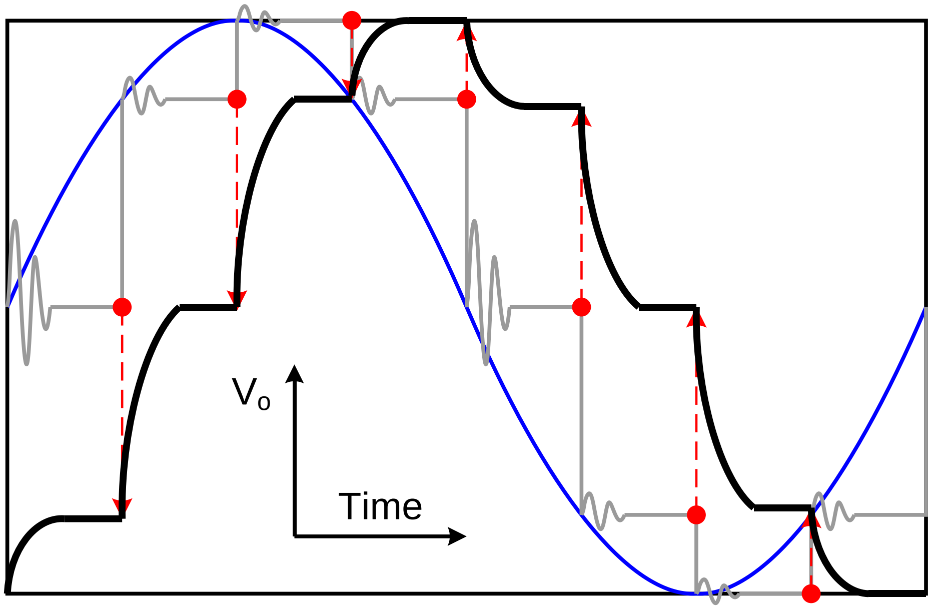
  0111…111 → 1000…000

- Glitches cause waveform distortion, spurs and elevated noise floors
- High-speed DAC output is often followed by a de-glitching SHA

De-Glitching SHA



SHA samples the output of the DAC after it settles and then hold it for T, removing the glitching energy.



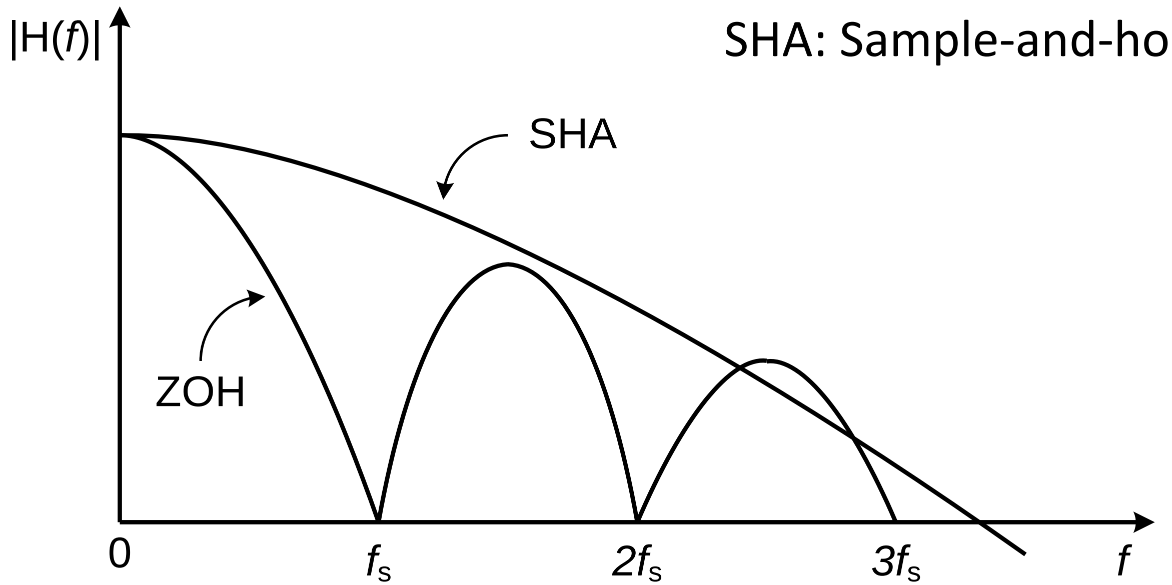
SHA output must be smooth (exponential settling can be viewed as pulse shaping

→ SHA BW does not have to be excessively large).

Frequency Response

ZOH: Zero-order hold

SHA: Sample-and-hold amplifier

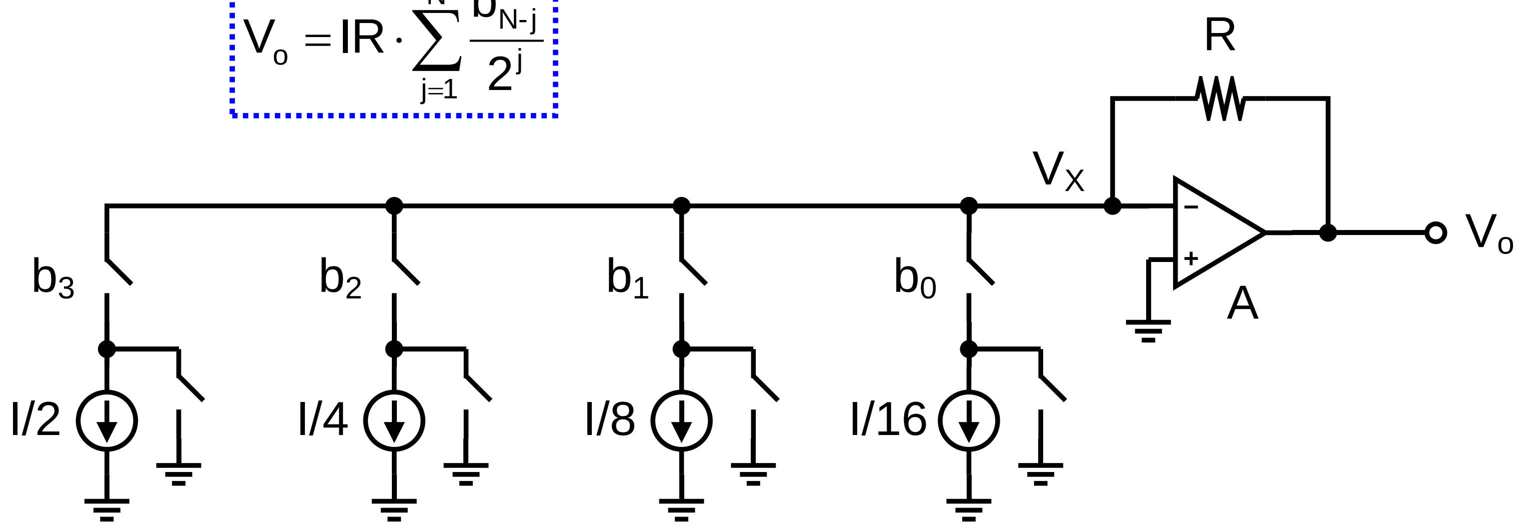


$$H_{ZOH}(j\omega) = e^{-j\frac{\omega T}{2}} \cdot \frac{\sin\left(\omega T/2\right)}{\omega T/2}$$

$$H_{SHA}(j\omega) = \frac{1}{1 + j\,\omega/\omega_{-3dB}}$$

Binary-Weighted Current DAC

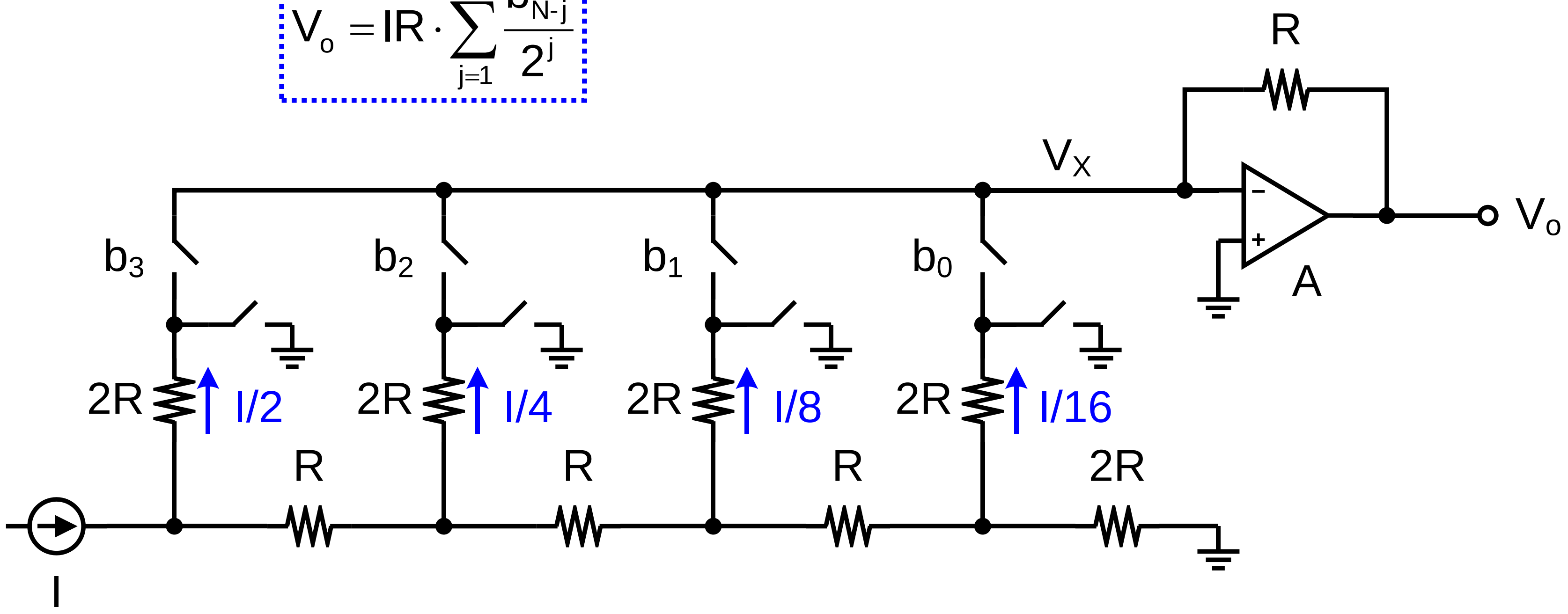
$$V_o = IR \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



- Current switching is simple and fast
- V_o depends on R_{out} of current sources without op-amp
- INL and DNL depend on matching, not inherently monotonic
- Large component spread (2^{N-1}:1)

R-2R DAC

$$V_o = IR \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j}$$



- A binary-weighted current DAC
- Component spread greatly reduced (2:1)

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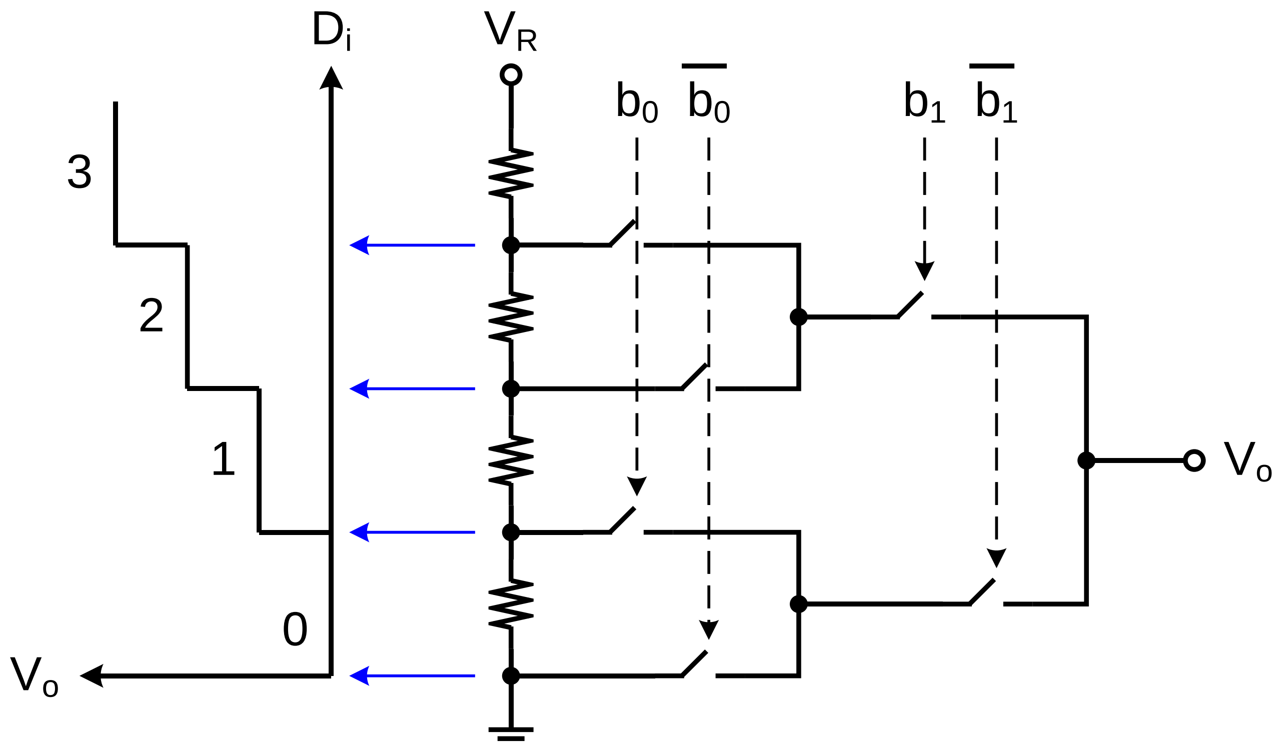
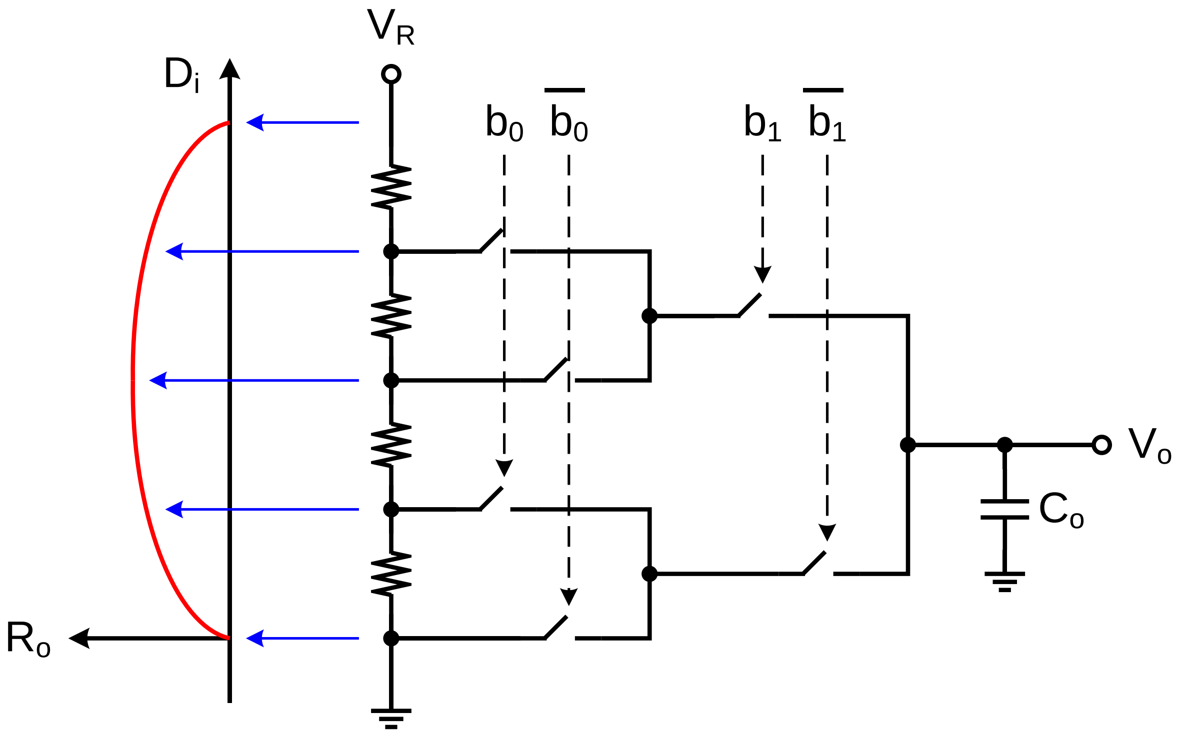
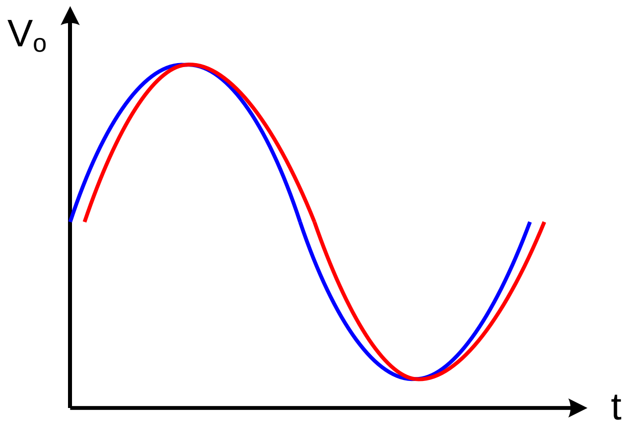
Resistor-String DAC



- Simple, inherently monotonic → good DNL performance
- Complexity ↑ speed ↓ for large N, typically N ≤ 8 bits

Code-Dependent R_o

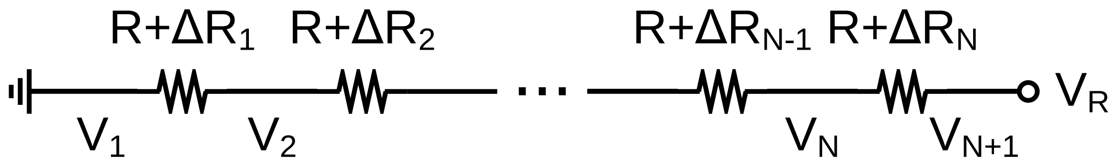




Signal-dependent R_oC_o causes HD

- R_o of ladder varies with signal (code)
- On-resistance of switches depend on tap voltage

DNL



$$\Delta R = [0, \sigma_R]$$

$$V_j = \frac{\sum_1^{j-1} R_k}{\sum_1^{N} R_k} \cdot V_R = \frac{(j-1)R + \sum_1^{j-1} \Delta R_k}{NR + \sum_1^{N} \Delta R_k} \cdot V_R$$

$$V_{j\text{-}1} = \frac{(j-2)R + \sum_1^{j-2} \Delta R_k}{NR + \sum_1^{N} \Delta R_k} \cdot V_R$$

$$V_j - V_{j\text{-}1} = \frac{R + \Delta R_{j-1}}{NR + \sum_1^{N} \Delta R_k} \cdot V_R \approx \frac{V_R}{N} + \frac{\Delta R_{j-1}}{NR} \cdot V_R$$

$$DNL_j = \left(V_j - V_{j\text{-}1} - \frac{V_R}{N} \right) \Big/ \frac{V_R}{N} \approx \frac{\Delta R_{j-1}}{R} \quad \Rightarrow \quad \overline{DNL} = 0,\ \sigma_{DNL} = \frac{\sigma_R}{R}$$

DNL of UE DAC is not related number of bit (N)

INL

$$V_j = \frac{\sum_1^{j-1} R_k}{\sum_1^{N} R_k} \cdot V_R = \frac{(j-1)R + \sum_1^{j-1} \Delta R_k}{NR + \sum_1^{N} \Delta R_k} \cdot V_R \approx \frac{j-1}{N} V_R + \frac{(N-j+1)\sum_1^{j-1} \Delta R_k - (j-1)\sum_j^{N} \Delta R_k}{N^2 R} V_R$$

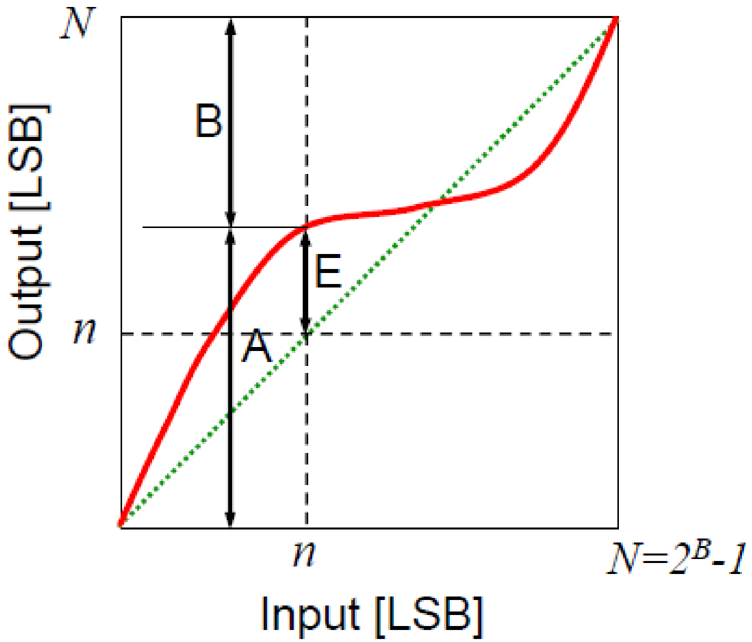
$$\Rightarrow \quad \overline{V_j} = \frac{j-1}{N} V_R, \quad \sigma_{V_j}{}^2 \approx \frac{(j-1)(N-j+1)}{N^3} \frac{\sigma_R{}^2}{R^2} V_R{}^2$$

$$\Rightarrow \quad \sigma_{V_j}{}^2 (\max) \approx \frac{1}{4N} \frac{\sigma_R{}^2}{R^2} V_R{}^2, \quad \text{when} \quad j = \frac{N}{2} + 1 \approx \frac{N}{2}$$

$$INL_j = \left(V_j - \frac{j\text{-}1}{N} V_R \right) \Big/ \frac{V_R}{N} \quad \Rightarrow \quad \overline{INL} = 0, \; \sigma_{INL}(\max) \approx \frac{\sqrt{N}}{2} \left(\frac{\sigma_R}{R} \right)$$

INL of UE DAC is related number of bit (N)

INL (cont.)



	Ideal	Variance
$A=n+E$	n	$n.\sigma_\varepsilon^2$
$B=N-n-E$	$N-n$	$(N-n).\sigma_\varepsilon^2$

$E = A-n \qquad r = n/N \qquad N=A+B$

$= A-r(A+B)$

$= A\,(1-r)\,-B.r$

$\rightarrow$ *Variance of E:*

$$\sigma_E^2 = (1-r)^2 .\sigma_A^2 + r^2 .\sigma_B^2$$

$$= N.r.(1-r).\sigma_\varepsilon^2$$

INL (cont.)

$$\sigma_E^2 = n\left(1-\frac{n}{N}\right)\times\sigma_\varepsilon^2$$

$$\text{To find max. variance:} \quad \frac{d\sigma_E^2}{dn} = 0$$

$$\rightarrow n = N/2$$

- Error is maximum at mid-scale (N/2):

$$\boxed{\begin{gathered}\sigma_{INL} = \frac{1}{2}\sqrt{2^B - 1}\,\sigma_\varepsilon \\ \text{with} \quad N = 2^B - 1\end{gathered}}$$

- INL depends on DAC resolution and element matching σ_ε
- While $\sigma_{DNL} = \sigma_\varepsilon$

Ref: Kuboki et al, TCAS, 6/1982

INL (cont.)

$$\sigma_{INL} \cong \frac{1}{2}\sqrt{2^B - 1}\,\sigma_\varepsilon$$

$$B \cong 2 + 2\log_2\left[\frac{\sigma_{INL}}{\sigma_\varepsilon}\right]$$

<u>Example:</u>

Assume the following requirement:

σ_{INL} $= 0.1\ LSB$

Then:

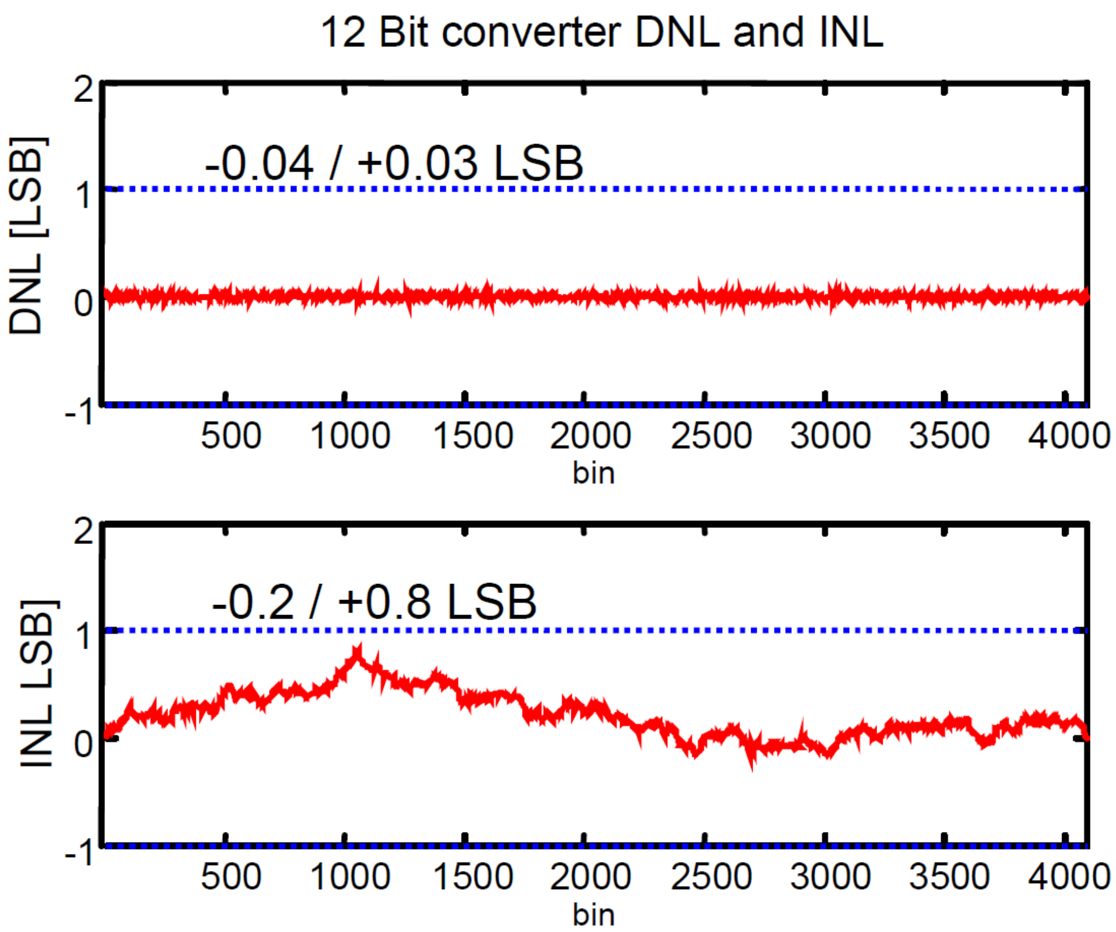
σ_ε = 1% → $B = 8.6$

σ_ε = 0.5% → $B = 10.6$

σ_ε = 0.2% → $B = 13.3$

σ_ε = 0.1% → $B = 15.3$

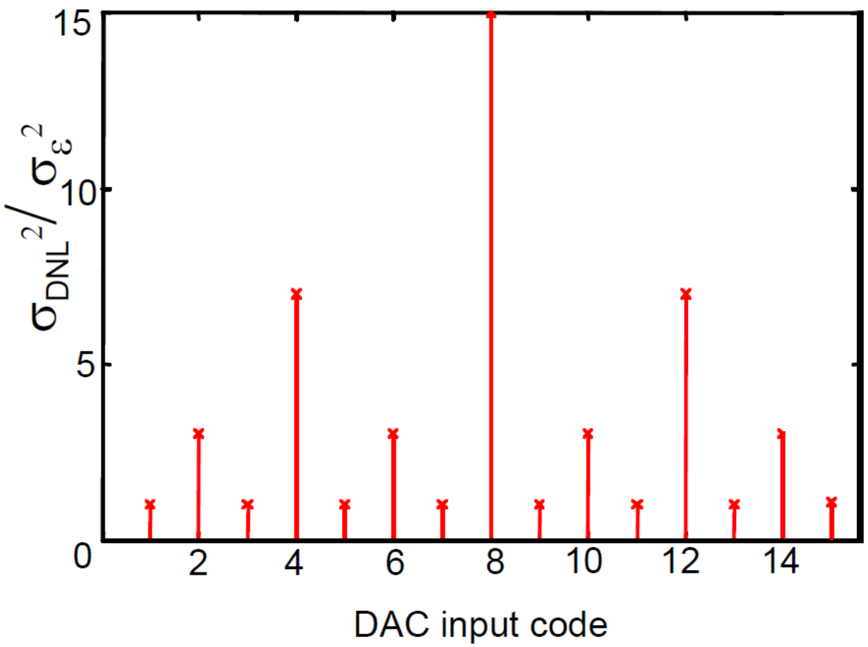
Simulation Example



σ_ε = 1%
B = 12
Random # generator used in MatLab

Computed INL:
σ_{DNL} = 0.01 LSB
σ_{INL} = 0.3 LSB
(midscale)

Binary Weighted (BW) DAC DNL



- Worst-case transition occurs at mid-scale:

$$\sigma_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)\sigma_\varepsilon^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)\sigma_\varepsilon^2}_{1000\ldots}$$

$$\cong 2^B \sigma_\varepsilon^2$$

$$\sigma_{DNL_{max}} = 2^{B/2}\sigma_\varepsilon$$

$$\sigma_{INLmax} \cong \frac{1}{2}\sqrt{2^B-1}\,\sigma_\varepsilon \cong \frac{1}{2}\sigma_{DNL_{max}}$$

- <u>Example:</u>

  $B = 12$, $\sigma_\varepsilon = 1\%$

  → σ_{DNL} = 0.64 LSB

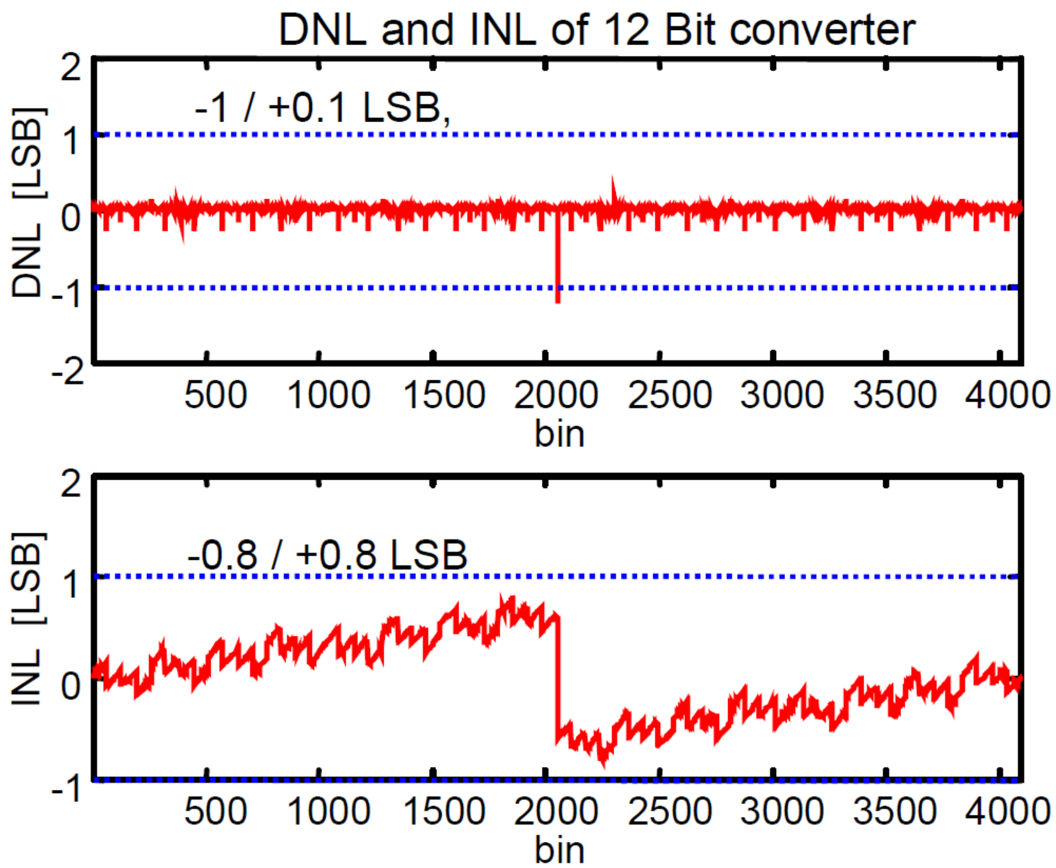
  → σ_{INL} = 0.32 LSB

INL and DNL of BW DAC

A BW DAC is typically constructed using unit elements, the same way as that of a UE DAC, for good component matching accuracy.

$$\Rightarrow \begin{array}{l} \overline{\mathrm{INL}} = 0,\ \sigma_{\mathrm{INL}}(\max) \approx \dfrac{\sqrt{N}}{2}\left(\dfrac{\sigma_R}{R}\right) \\ \overline{\mathrm{DNL}} = 0,\ \sigma_{\mathrm{DNL}}(\max) = 2 \cdot \mathrm{INL} \approx \sqrt{N}\left(\dfrac{\sigma_R}{R}\right) \end{array}$$

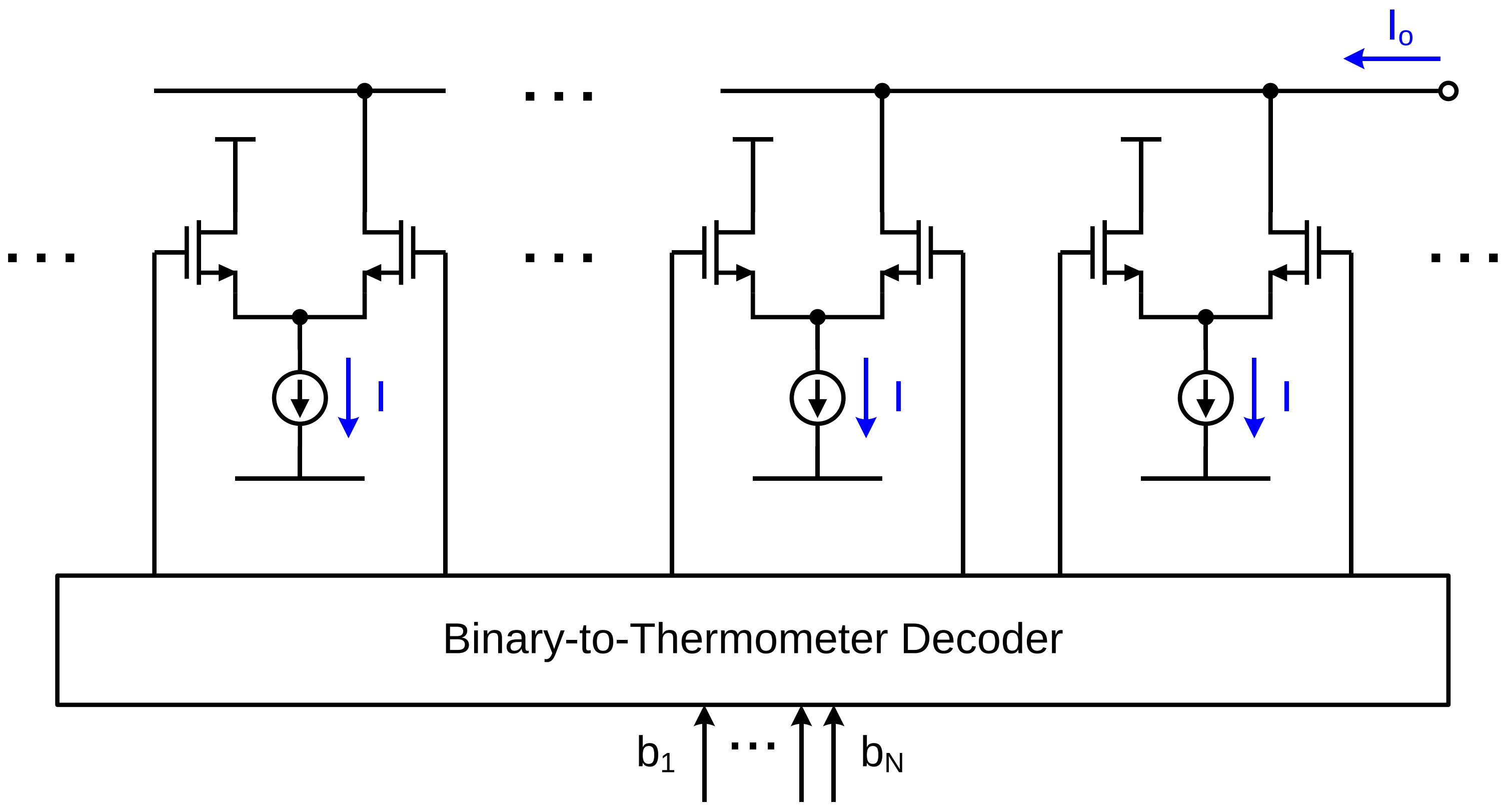
Simulation Example



Now (by chance) worst DNL is mid-scale.

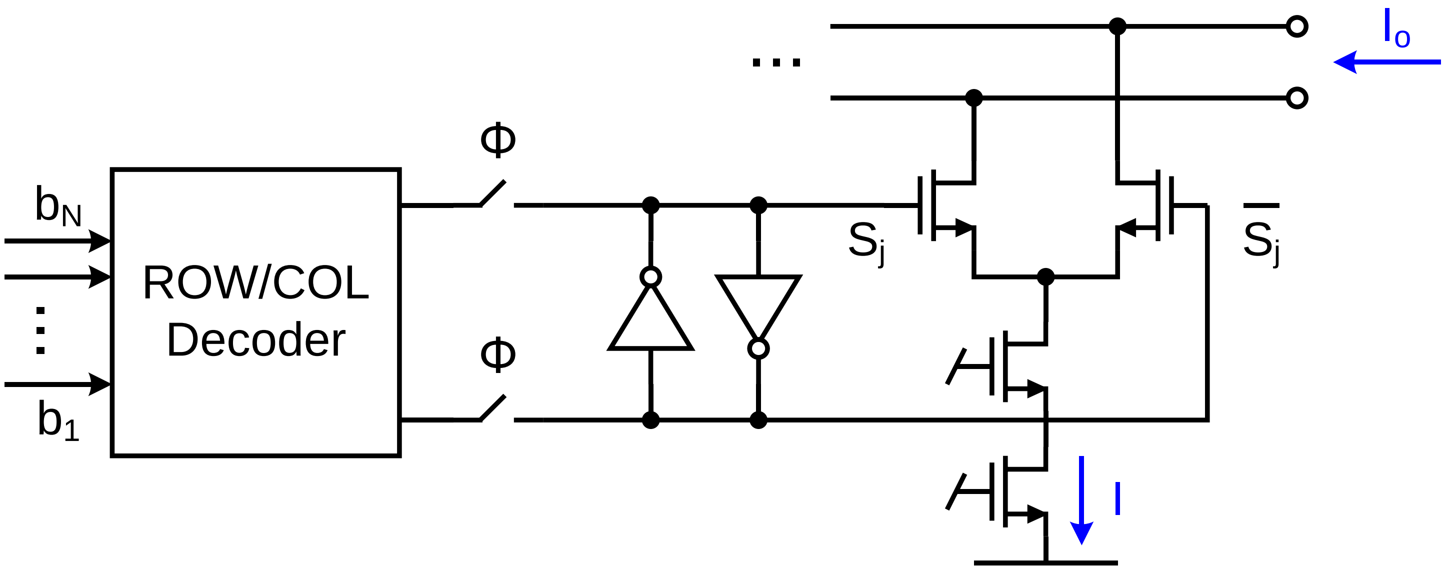
Close to statistical result!

Current-Steering DAC



- Fast, inherently monotonic → good DNL performance
- Complexity increases for large N, requires B2T decoder

Unit Current Cell



- 2^N current cells typically decomposed into a $(2^{N/2} \times 2^{N/2})$ matrix
- Current source cascoded to improve accuracy (R_o effect)
- Coupled inverters improve synchronization of current switches

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BW vs. UE DACs

Binary-weighted DAC

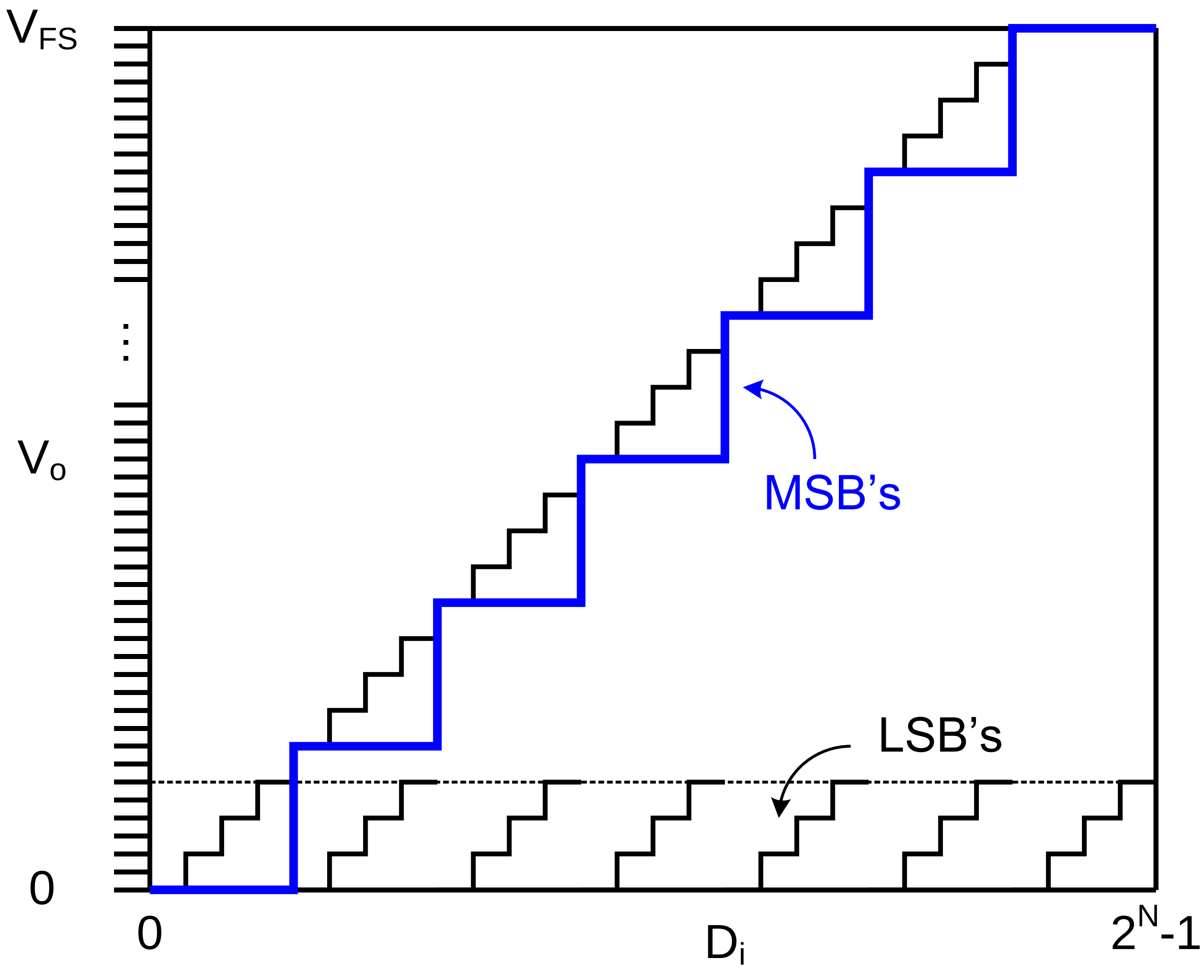
- Pros
  - Min. # of switched elements
  - Simple and fast
  - Compact and efficient
- Cons
  - Large DNL and glitches
  - Monotonicity not guaranteed
- INL/DNL
  - INL(max) ≈ $(\sqrt{N}/2)\sigma$
  - DNL(max) ≈ 2*INL

Unit-element DAC

- Pros
  - Good DNL, small glitches
  - Linear glitch energy
  - Guaranteed monotonic
- Cons
  - Needs B2T decoder
  - complex for $N \geq 8$
- INL/DNL
  - INL(max) ≈ $(\sqrt{N}/2)\sigma$
  - DNL(max) ≈ σ

Combine BW and UE architectures → Segmentation

Segmented DAC



- MSB DAC:
  M-bit UE DAC
- LSB DAC:
  L-bit BW DAC
- Resolution:
  B = M + L
- 2^M+L switching elements
- Same INL as BW or UE
- DNL equivalent to (L+1) bits of BW DAC

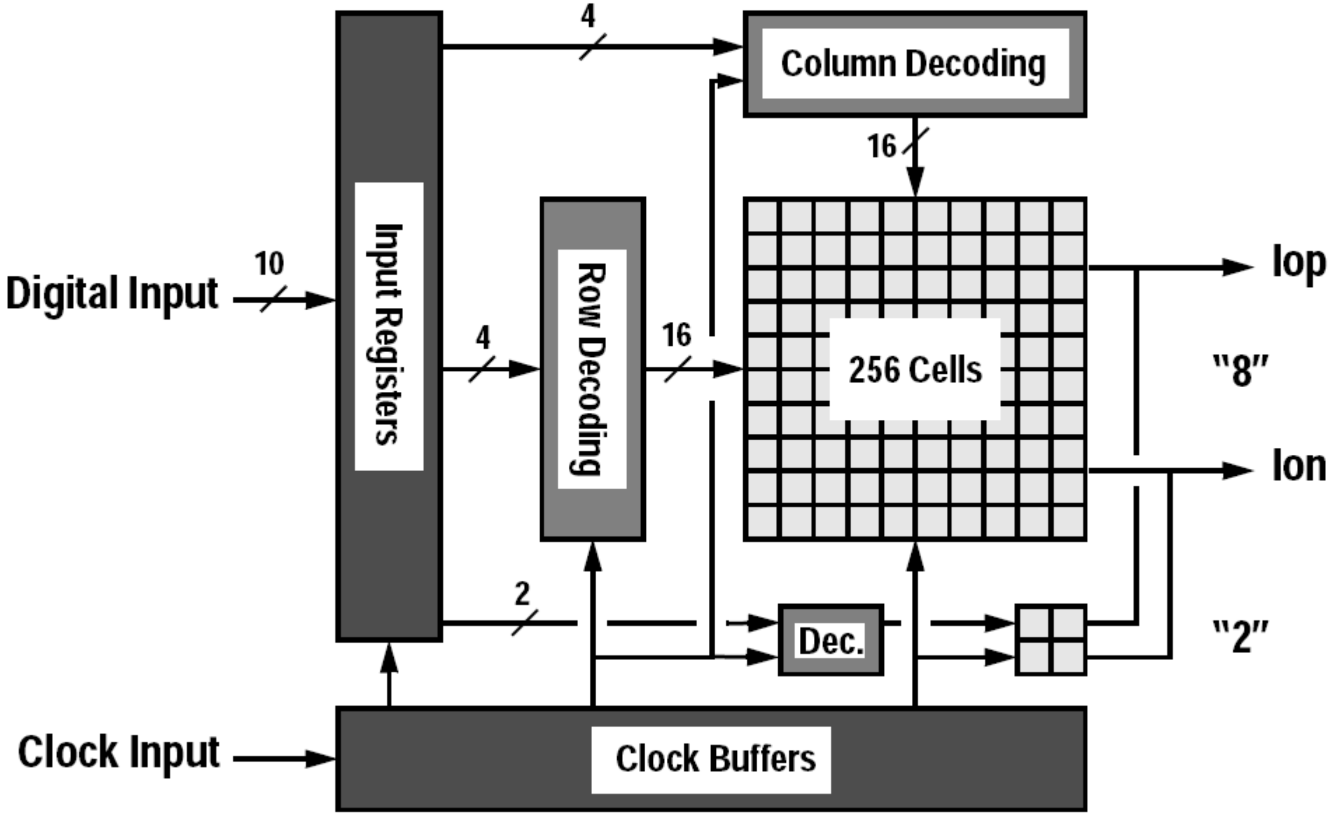
Comparison

Example: B = 12, N = 4096, σ = 1%

Architecture	σ_{INL}	σ_{DNL}	# of s.e.	
				$\sigma_{INL}(\max) \approx \frac{\sqrt{2^B}}{2}(\sigma)$
Unit-element	0.32 LSB's	0.01 LSB's	2^B = 4096	$\sigma_{DNL}(\max) = 1(\sigma)$
Segmented1	0.32 LSB's	0.06 LSB's	M=8, L=4 2^M+L = 260	$\sigma_{DNL}(\max) = \sqrt{2^{L+1}}(\sigma)$
Segmented2	0.32 LSB's	0.22 LSB's	M=4, L=8 2^M+L = 22	$\sigma_{DNL}(\max) = \sqrt{2^{L+1}}(\sigma)$
Binary-weighted	0.32 LSB's	0.64 LSB's	N = 12	$\sigma_{DNL}(\max) = \sqrt{2^B}(\sigma)$

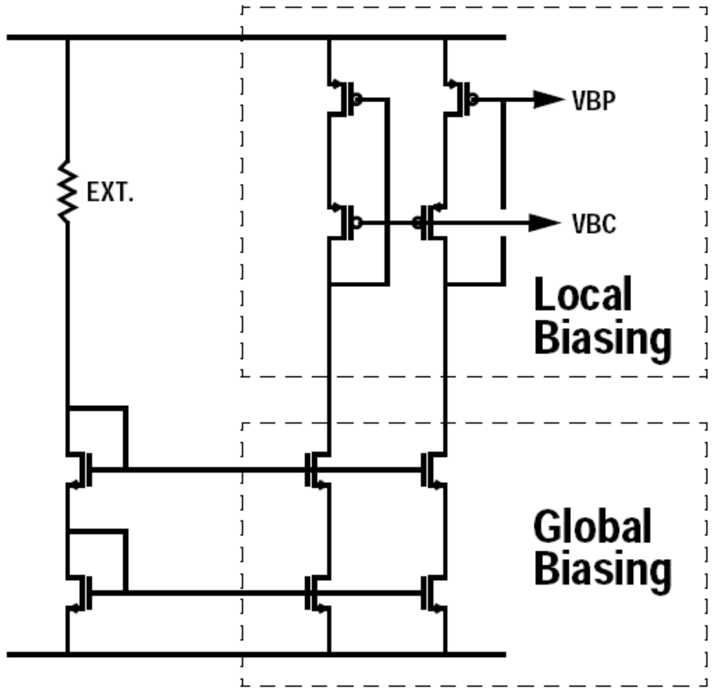
Max. DNL error occurs at the transitions of MSB segments

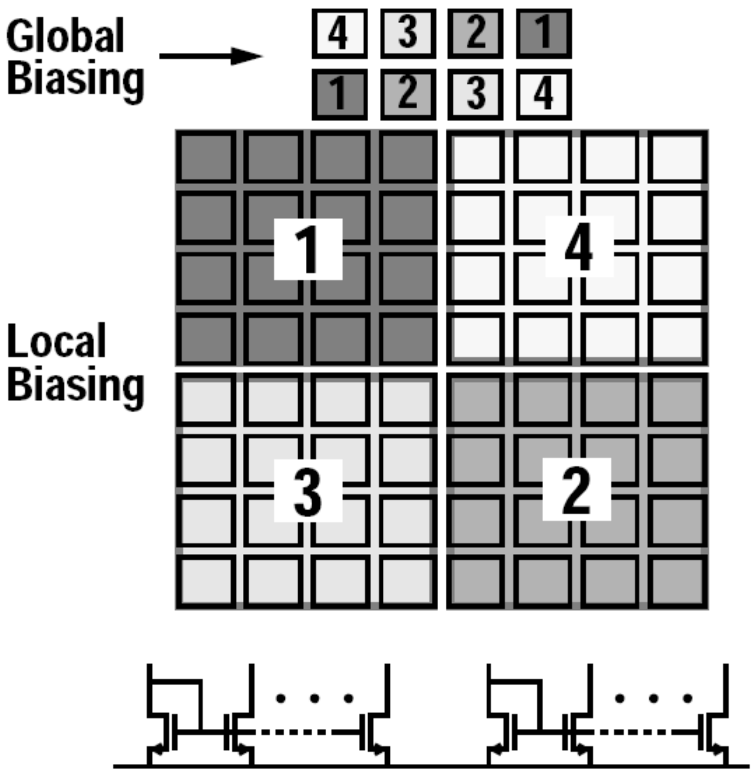
Exp: “8+2” Segmented Current DAC



Ref: C.-H. Lin and K. Bult, “A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2,” *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

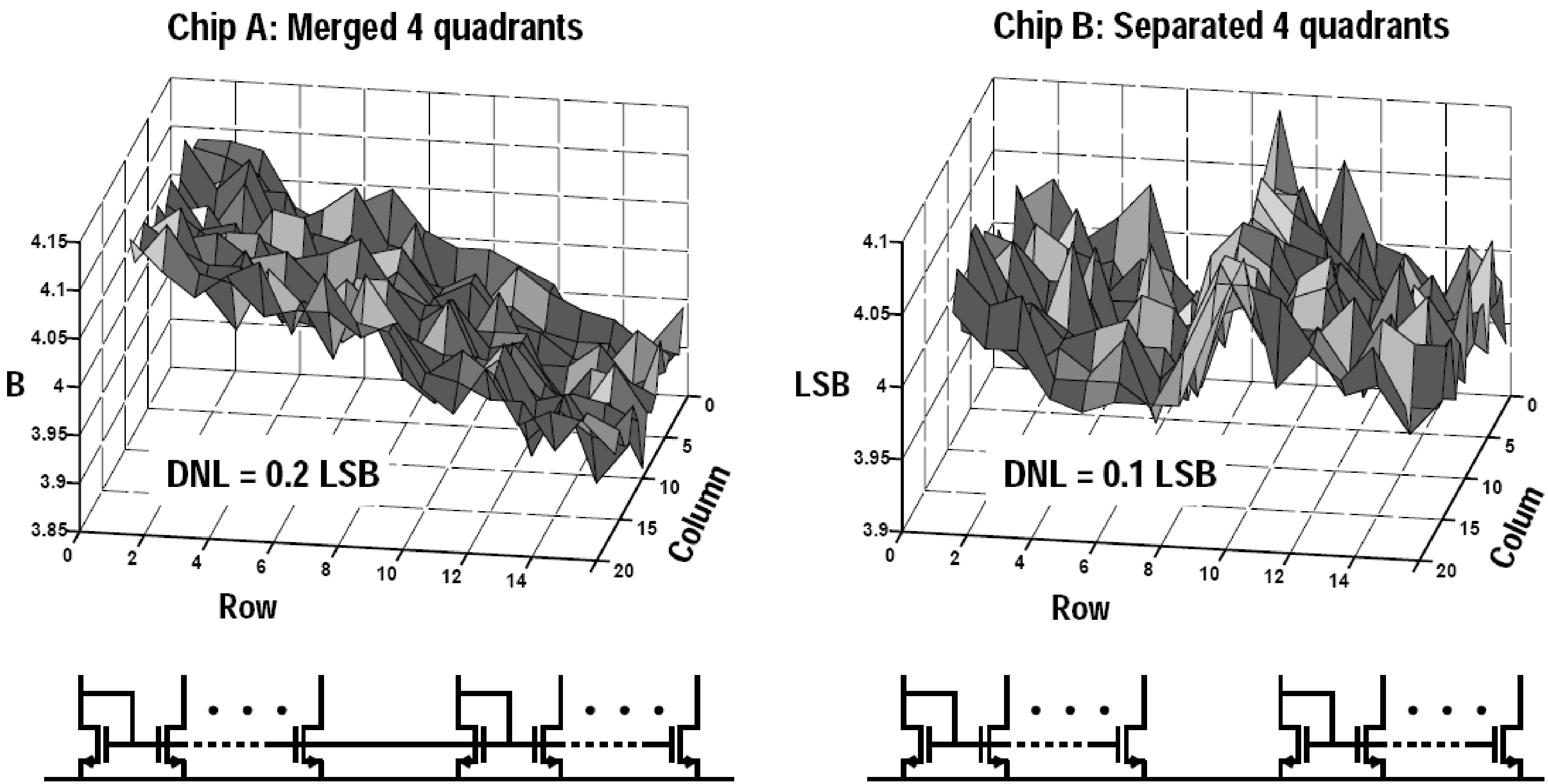
MSB-DAC Biasing Scheme



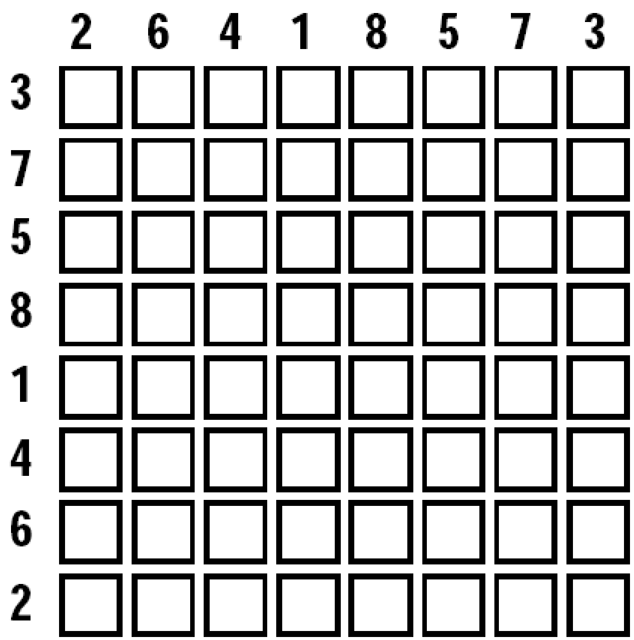


Common-centroid global biasing + divided 4 quadrants of current cells

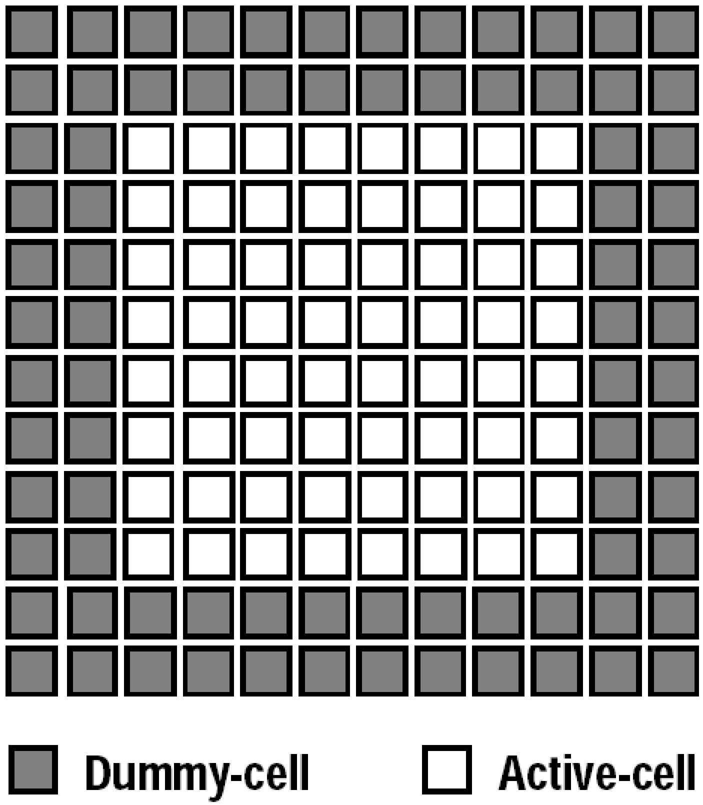
MSB-DAC Biasing Scheme



Randomization and Dummies



- Column and row randomization to improve INL



References

1. Y. Chiu, Data Converters Lecture Slides, UT Dallas 2012.
2. V. Saxena, Advance Analog Circuit Design, Boise State University 2012.
3. M. J. M. Pelgrom, JSSC, pp. 1347-1352, issue 6, 1990.
4. D. K. Su and B. A. Wooley, JSSC, pp. 1224-1233, issue 12, 1993.
5. C.-H. Lin and K. Bult, JSSC, pp. 1948-1958, issue 12, 1998.
6. K. Khanoyan, F. Behbahani, A. A. Abidi, VLSI, 1999, pp. 73-76.
7. K. Falakshahi, C.-K. Yang, B. A. Wooley, JSSC, pp. 607-615, issue 5, 1999.
8. G. A. M. Van Der Plas et al., JSSC, pp. 1708-1718, issue 12, 1999.
9. A. R. Bugeja and B.-S. Song, JSSC, pp. 1719-1732, issue 12, 1999.
10. A. R. Bugeja and B.-S. Song, JSSC, pp. 1841-1852, issue 12, 2000.
11. A. van den Bosch et al., JSSC, pp. 315-324, issue 3, 2001.