CHAPTER 6

Analog Front End

Outline

- 6.1 Introduction
- 6.2 Switched-Capacitor Circuit
- 6.3 SC Application
- 6.4 Noise in SC
- 6.5 Non-ideal Effects in SC
- 6.6 Practical Issues

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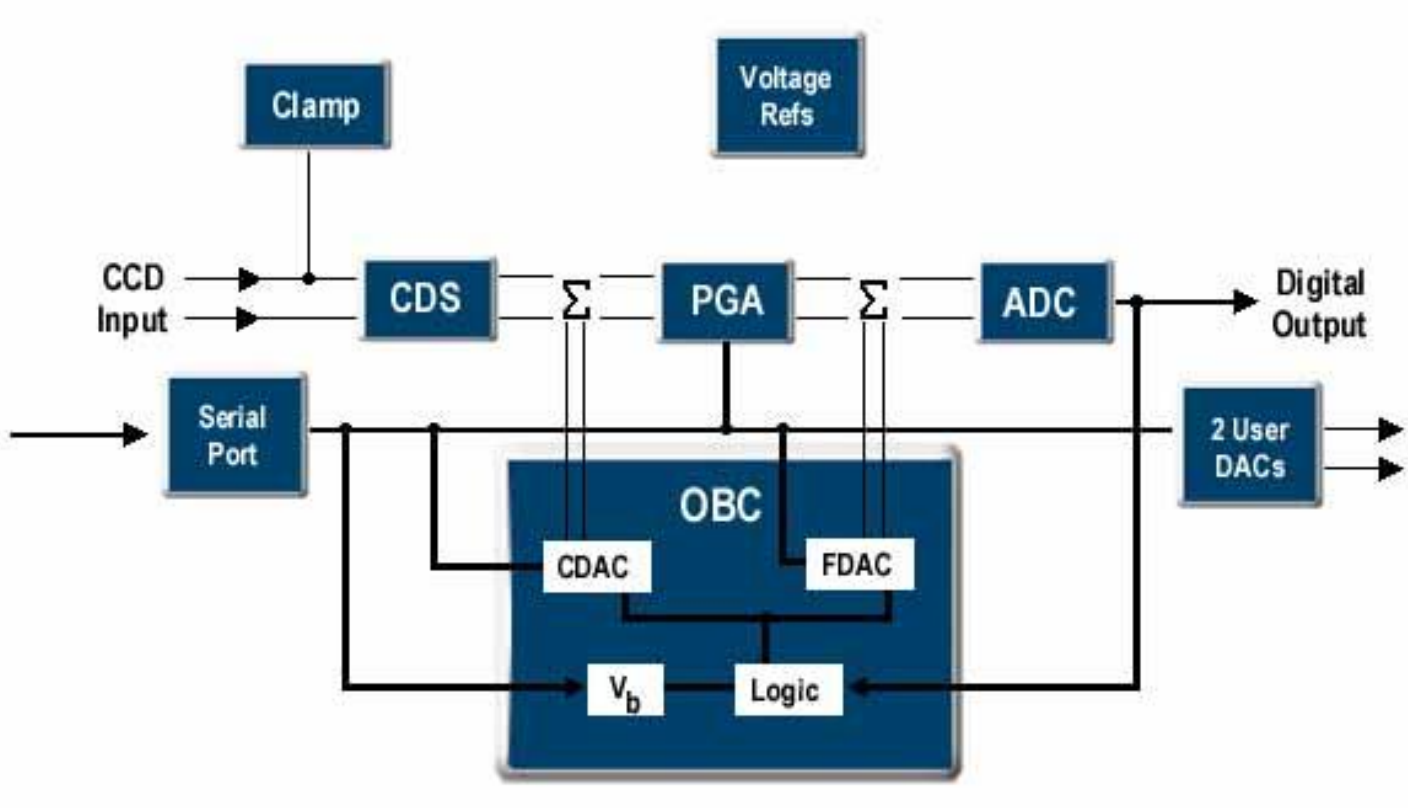
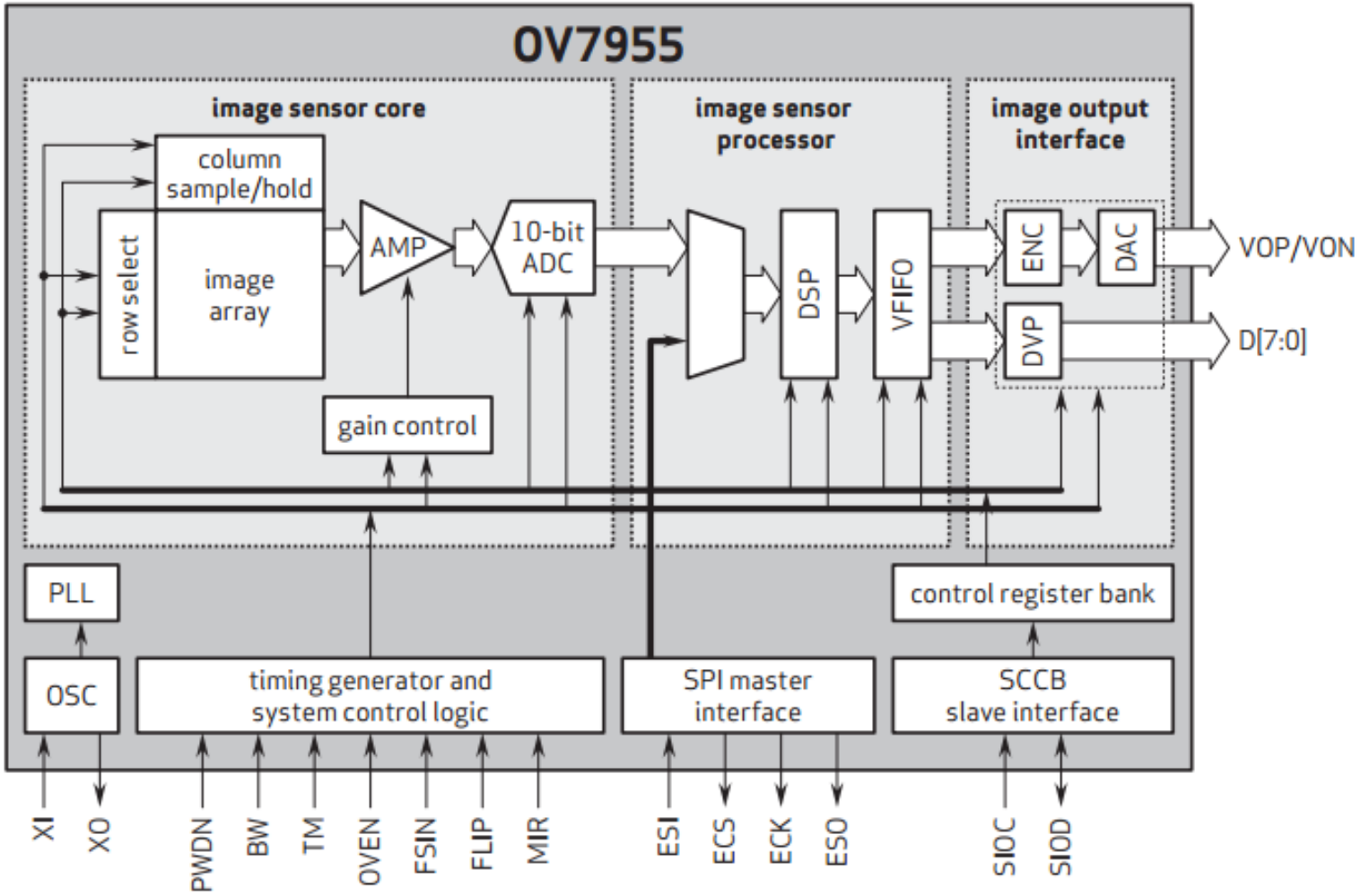
Introduction

- Analog front end
  - Correlated double sampling (CDS) : optional
  - Programmable gain amplifier (PGA)
  - Digital to analog converter (DAC)
  - Analog to digital converter (ADC)

AFE for CCD

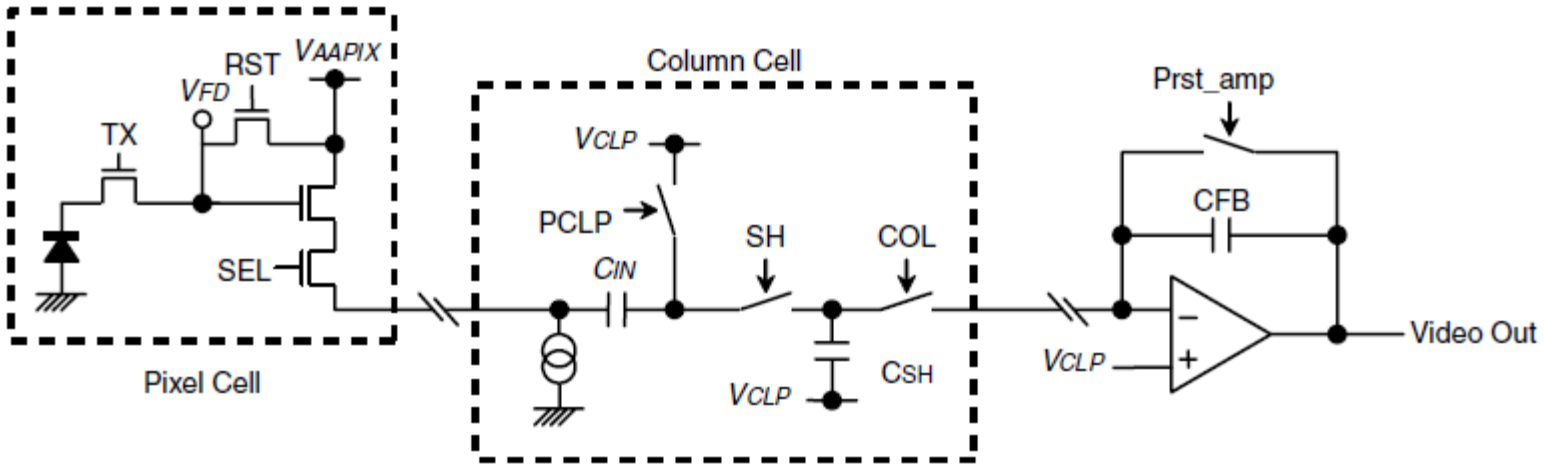

Clamp
Voltage Refs
CCD Input
CDS
Σ
PGA
Σ
ADC
Digital Output
Serial Port
2 User DACs
OBC
CDAC
FDAC
V_b
Logic

Commercial CIS Product



Correlated Double Sampling

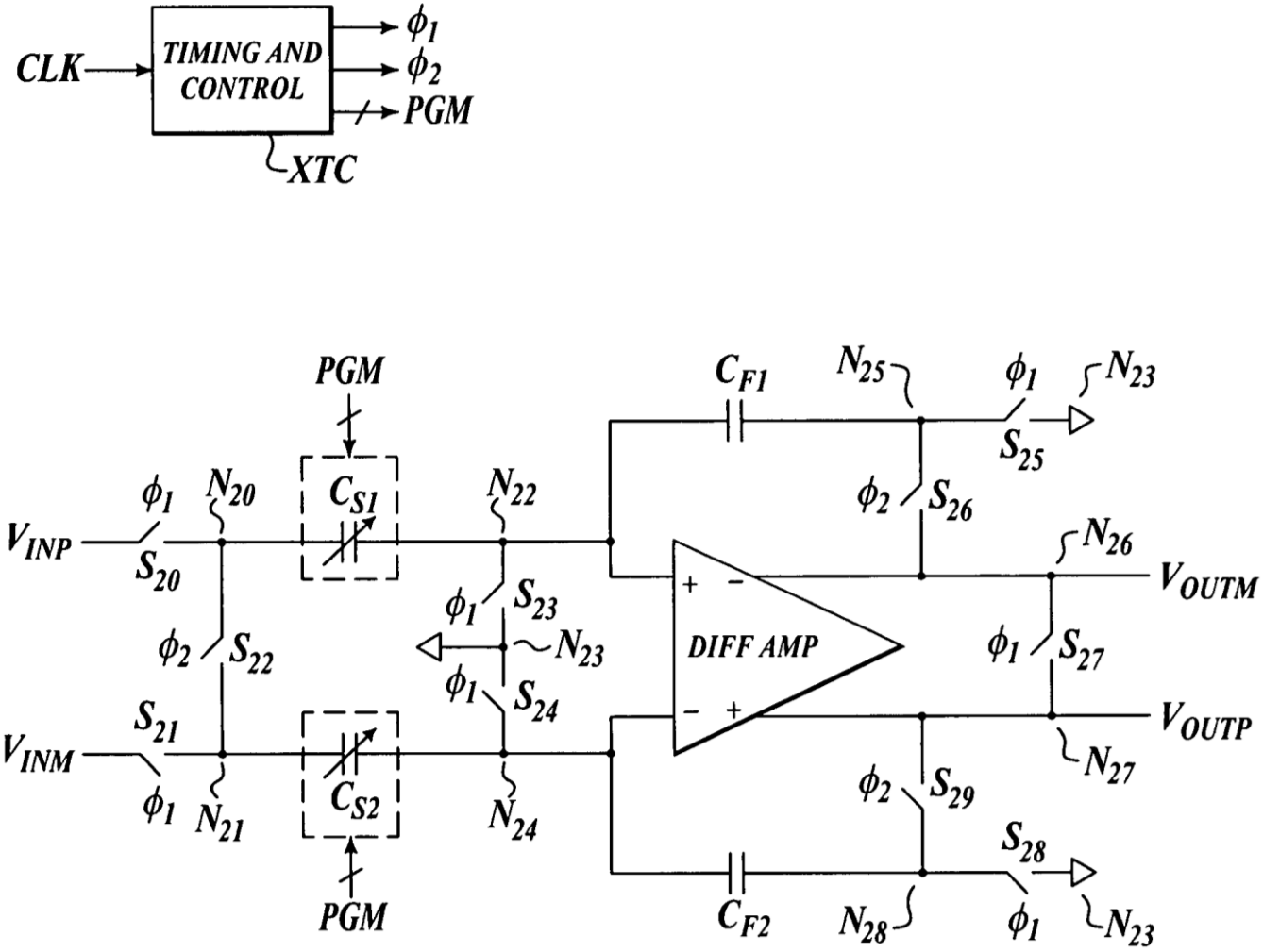
- Purpose of CDS
  - Inter-chip signal sampling, signal clamp (CCD + AFE)
  - Offset cancellation
  - Fixed pattern cancellation
  - KTC cancellation
  - Signal buffering & level shifting



Programmable Gain Amplifier

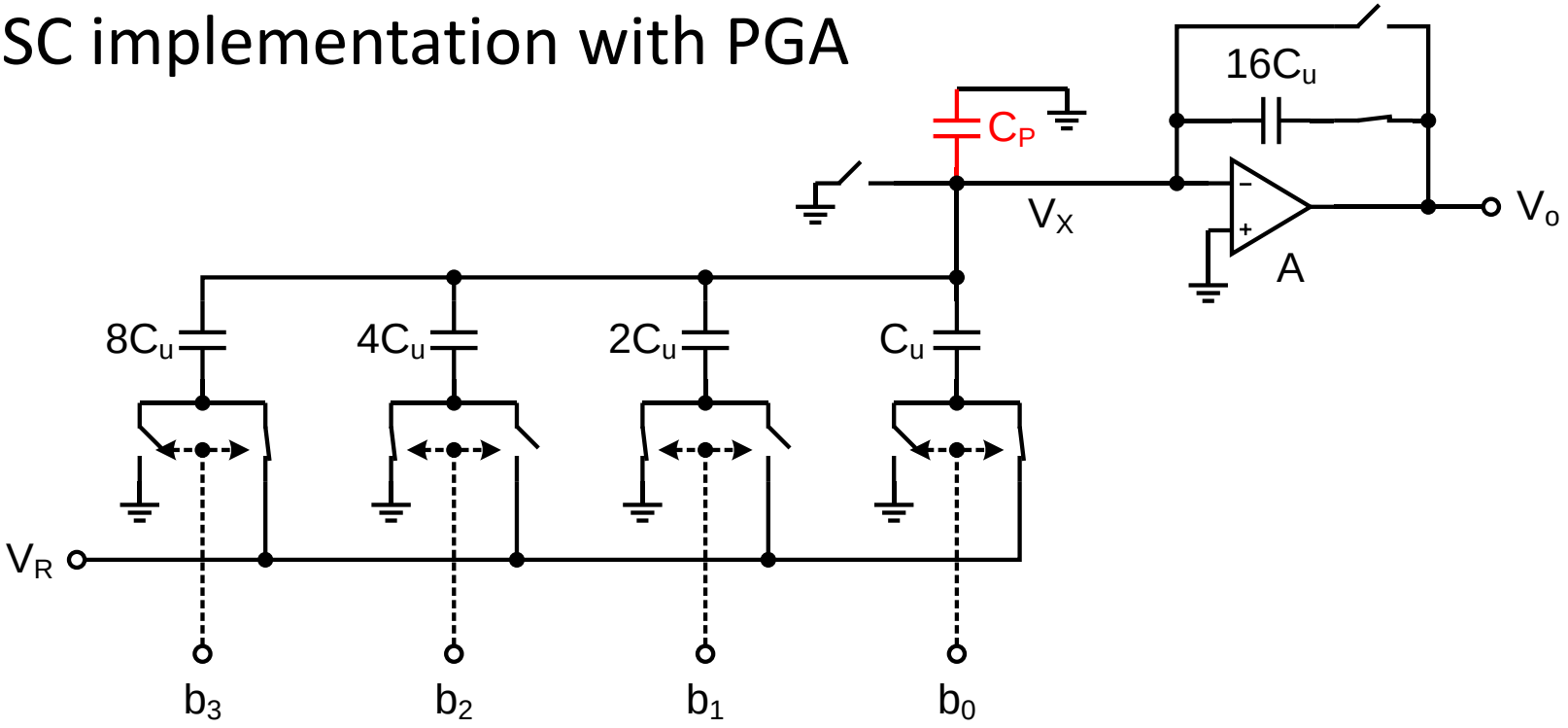
- Purpose of PGA
  - CDS implementation
  - Single-to-differential conversion
  - Signal amplification
  - Color balance in analog domain (white balance)
  - ADC input level fitting : signal full-swing tuning

Switched Capacitor PGA



Digital to Analog Converter

- Purpose of DAC
  - Signal path offset cancellation
  - Optical black calibration (analog domain)
  - SC implementation with PGA



Analog to Digital Converter

- Purpose of ADC
  - Digitization for subsequent signal processing
  - 8b ~ 12b depends on application
  - Single / Column-parallel / Pixel-parallel implementation depends on required bandwidth
  - Pipeline / Single-slope / SAR / Cyclic …

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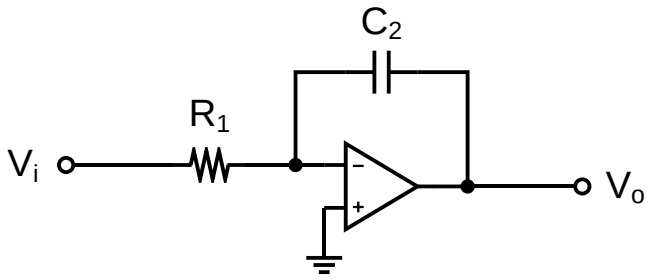
Continuous-Time Integrator

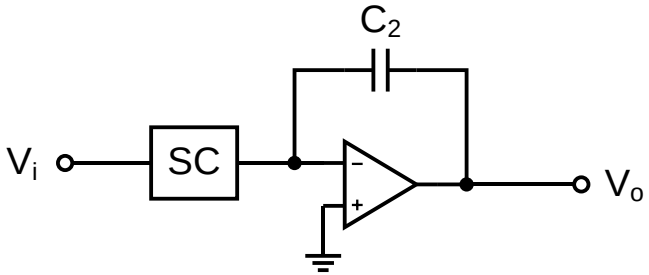


$$v_o(t) = -\frac{1}{R_1 \cdot C_2}\int_{-\infty}^{t} v_{in}(\xi)\,d\xi$$

$$H(s) = \frac{V_o}{V_i}(s) = -\left(\frac{1}{R_1 \cdot C_2}\right)\cdot\frac{1}{s}$$

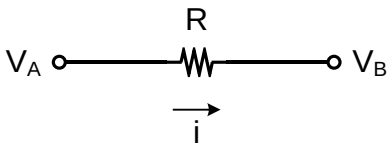
$$\tau = R_1 \cdot C_2$$

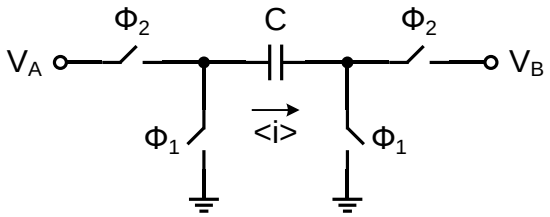
Goal:



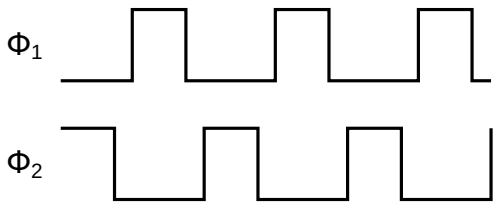
Approach: emulating resistors with switched capacitors

Concept of Switched Capacitor





Non-overlapping two-phase clock



$$i = \frac{1}{R}(V_A - V_B)$$

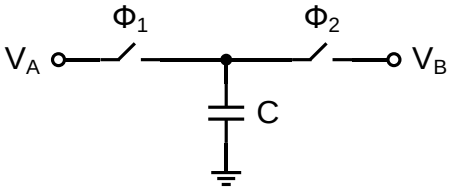
$$\langle i \rangle = \frac{q}{T} = \frac{C}{T}(V_A - V_B)$$

$$\Rightarrow \quad \boxed{R_{eq} = \frac{T}{C}} \qquad \text{so,} \quad \tau = R_{eq,1} \cdot C_2 = \frac{T}{C_1} \cdot C_2 = T \cdot \frac{C_2}{C_1}$$

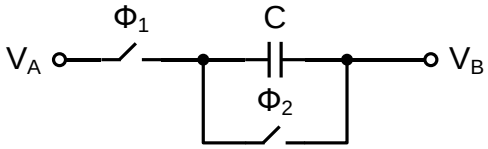
- A switched capacitor is a discrete-time “resistor”
- RC time constant set by capacitor ratio C_2/C_1 (match considerably better than R and C) and clock period T (flexibility)

Switched Capacitors

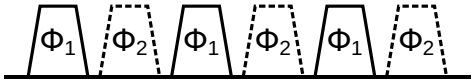
Shunt-type

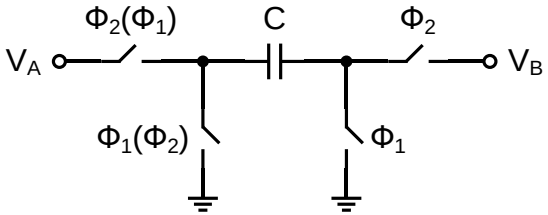


Series-type



2-phase clock



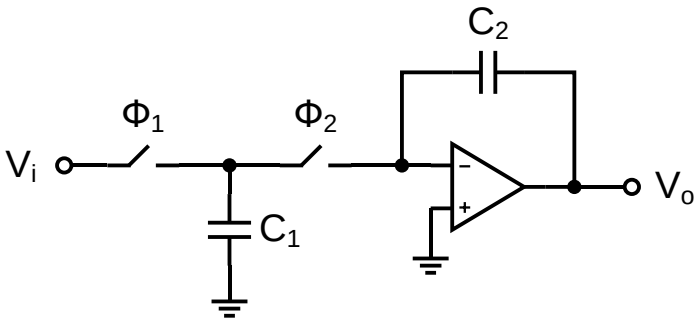


Stray-insensitive

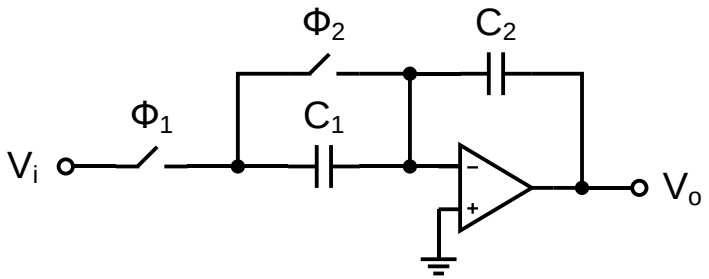
- Shunt- and series-type SCs are simple and cheap to implement
- Stray-insensitive SC requires 2 more switches

Discrete-Time Integrator (DTI)

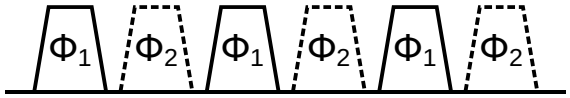
Shunt-type



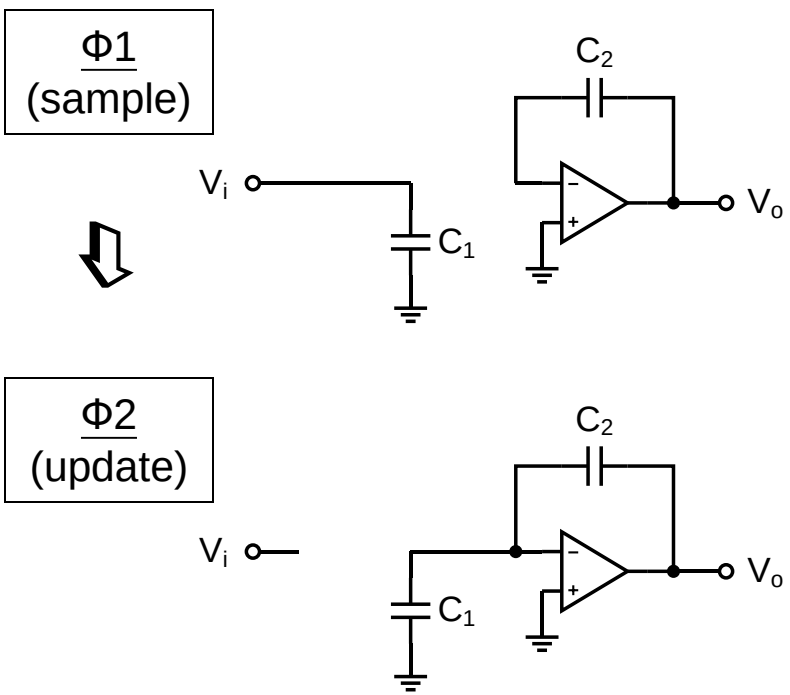
Series-type

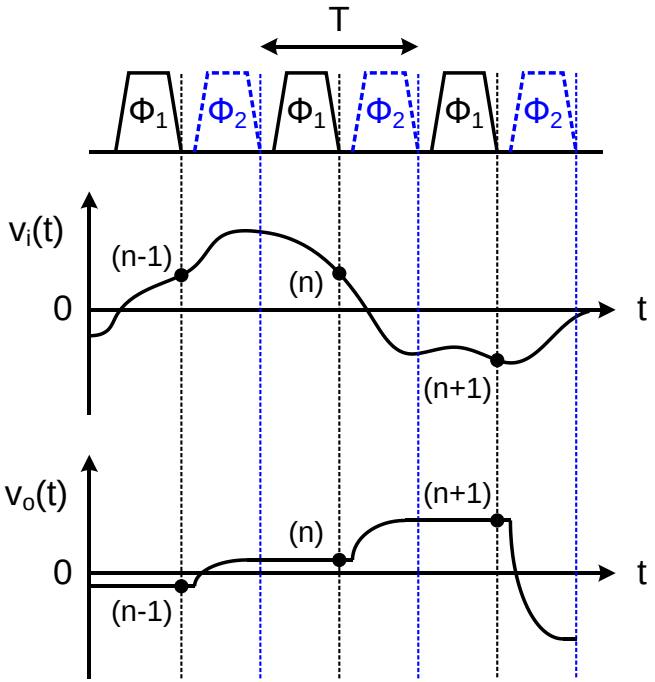


2-phase clock



Shunt-Type DTI

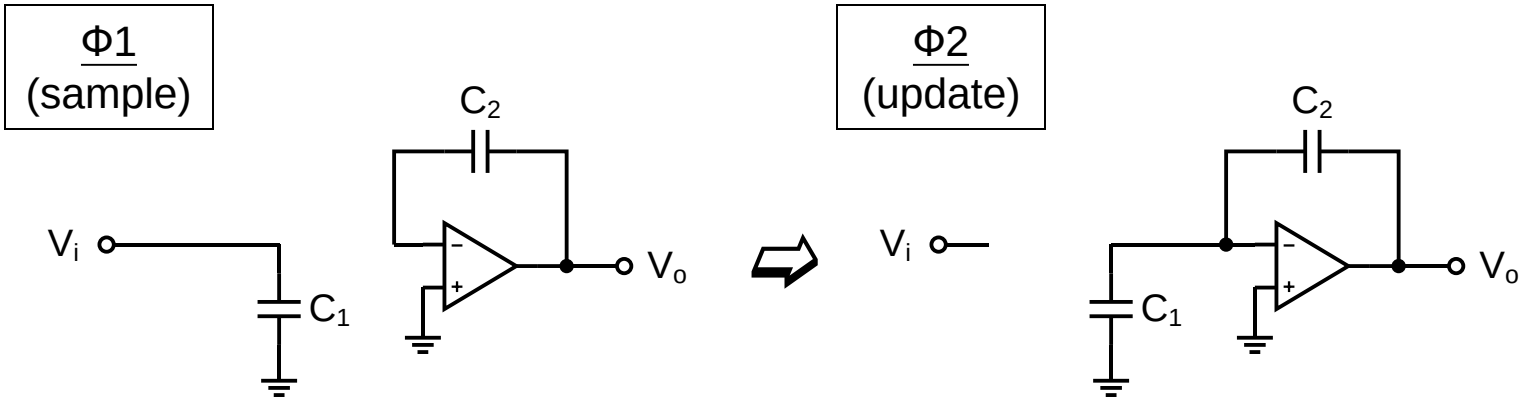




Charge conservation law (ideal):

Total charge on C_1 and C_2 during $\Phi_1 \rightarrow \Phi_2$ transition must remain unchanged!

Shunt-Type DTI



$$\sum Q(\varphi_1) = V_i(n)\cdot C_1 - V_o(n)\cdot C_2 \qquad \sum Q(\varphi_2) = 0\cdot C_1 - V_o(n+1)\cdot C_2$$

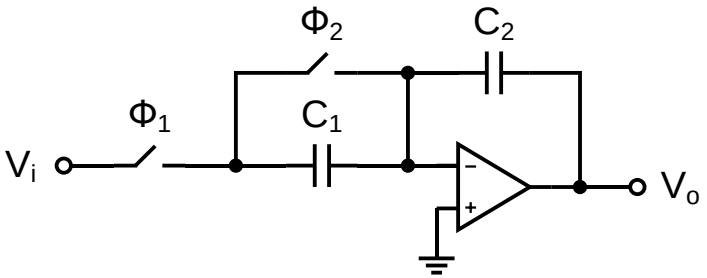
$$\sum Q(\varphi_1) = \sum Q(\varphi_2) \;\Rightarrow\; V_i(n)\cdot C_1 - V_o(n)\cdot C_2 = 0\cdot C_1 - V_o(n+1)\cdot C_2$$

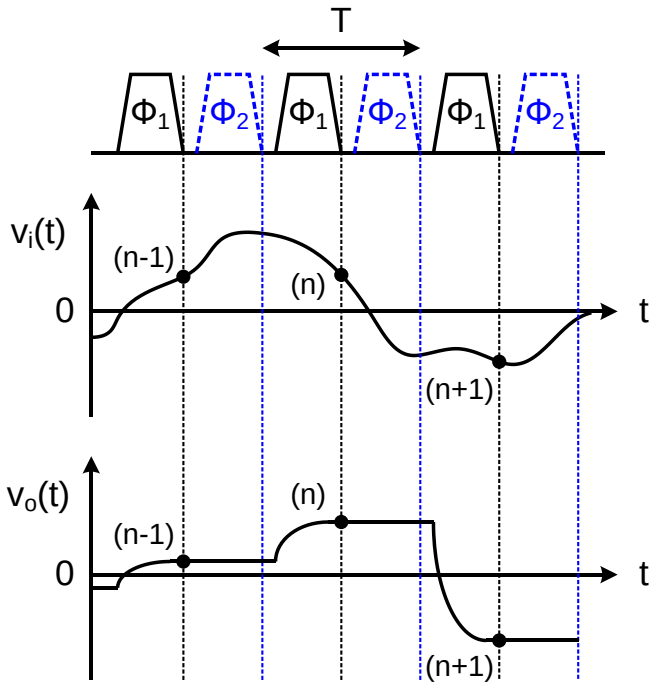
$$V_i(z)\cdot C_1 - V_o(z)\cdot C_2 = -z\cdot V_o(z)\cdot C_2$$

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}$$

Series-Type DTI

Φ1 (sample/update) ⇨ Φ2 (reset C_1)





$$\sum Q(\phi_2) = \sum Q(\phi_1) \quad \Rightarrow \quad 0 \cdot C_1 - V_o(n) \cdot C_2 = -V_i(n+1) \cdot C_1 - V_o(n+1) \cdot C_2$$

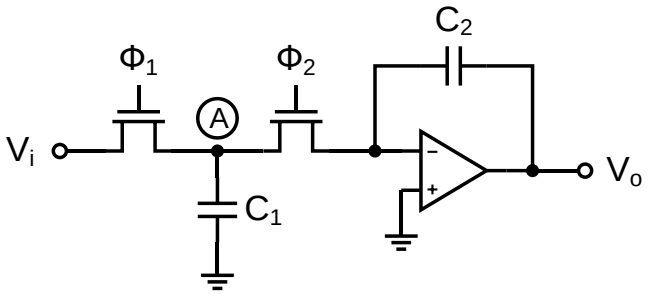
$$V_o(z) \cdot C_2 = z \cdot V_i(z) \cdot C_1 + z \cdot V_o(z) \cdot C_2$$

VTF:

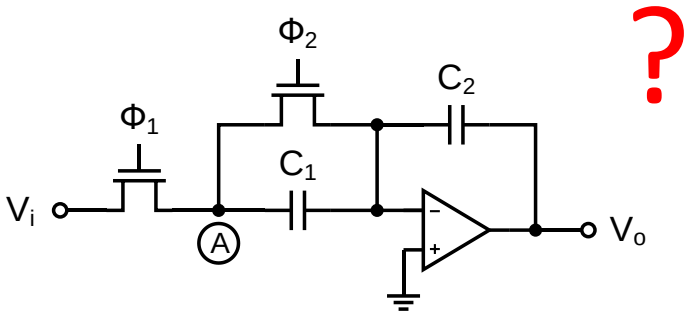
$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2} \frac{1}{1 - z^{-1}}$$

Stray Capacitance

Shunt-type

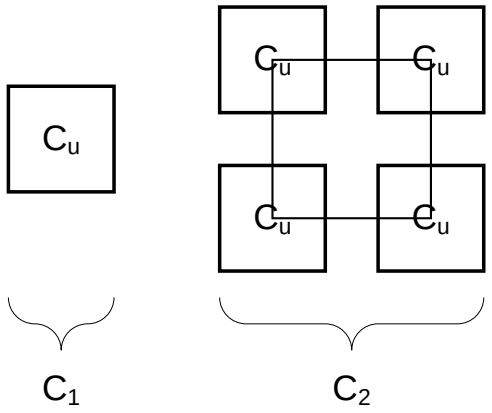


Series-type



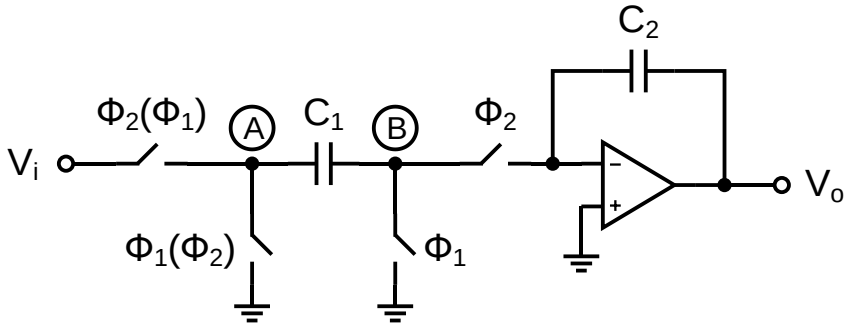
?

$$\frac{C_2}{C_1} = 4$$



- Strays derive from D/S diodes and wiring capacitance
- VTF is modified due to strays
- Strays at the summing node is of no significance (virtual ground)

Stray-Insensitive SC Integrator



"Inverting"

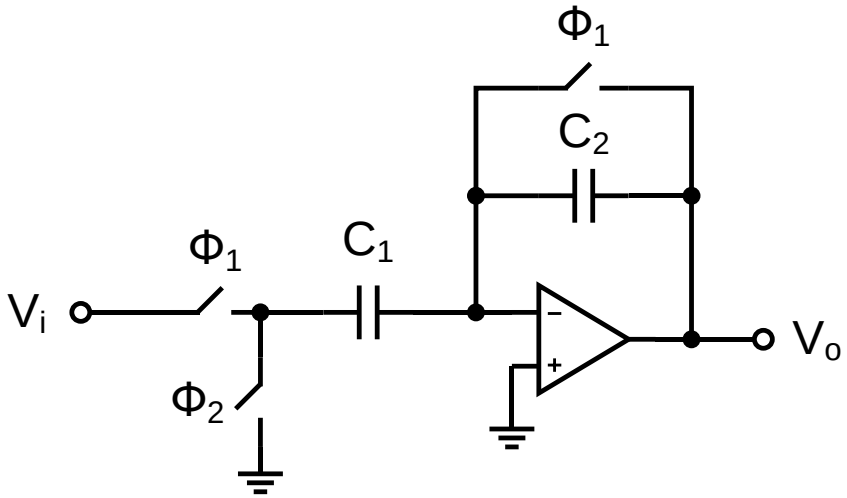
VTF: $$H(z) = -\frac{C_1}{C_2}\frac{1}{1-z^{-1}}$$

"Non-inverting"

VTF: $$H(z) = +\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}$$

- Capacitors can be significantly sized down to save power/area
- Sizes are eventually limited by kT/C noise, mismatch, etc.

SC Amplifier

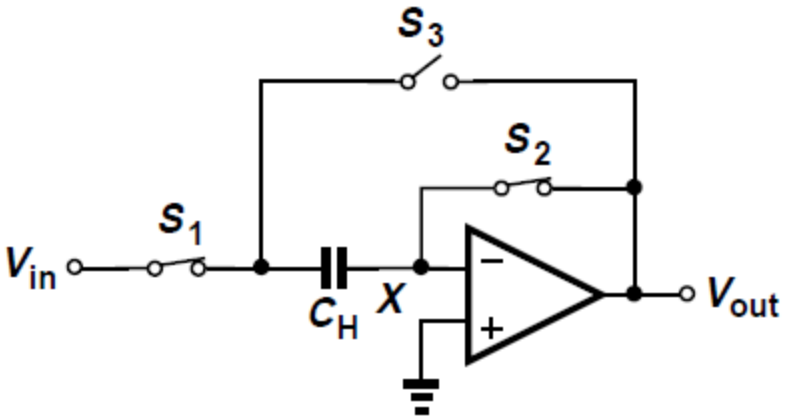


VTF:

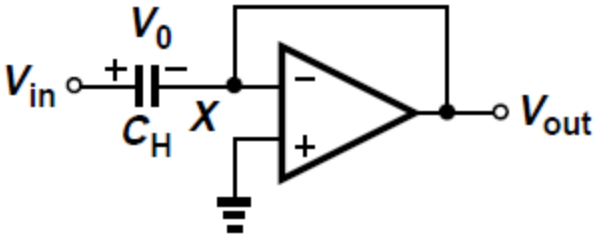
$$H(z) = +\frac{C_1}{C_2} \cdot z^{-1}$$

- Gain implemented by C ratio
- No resistive loading of amplifier (high gain)

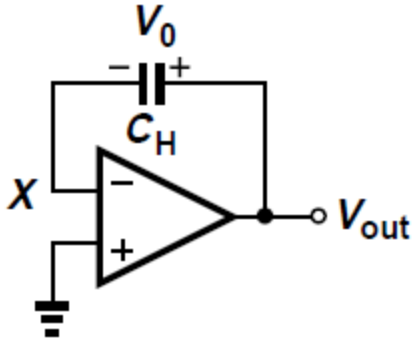
SC Unit Gain Buffer



(a)

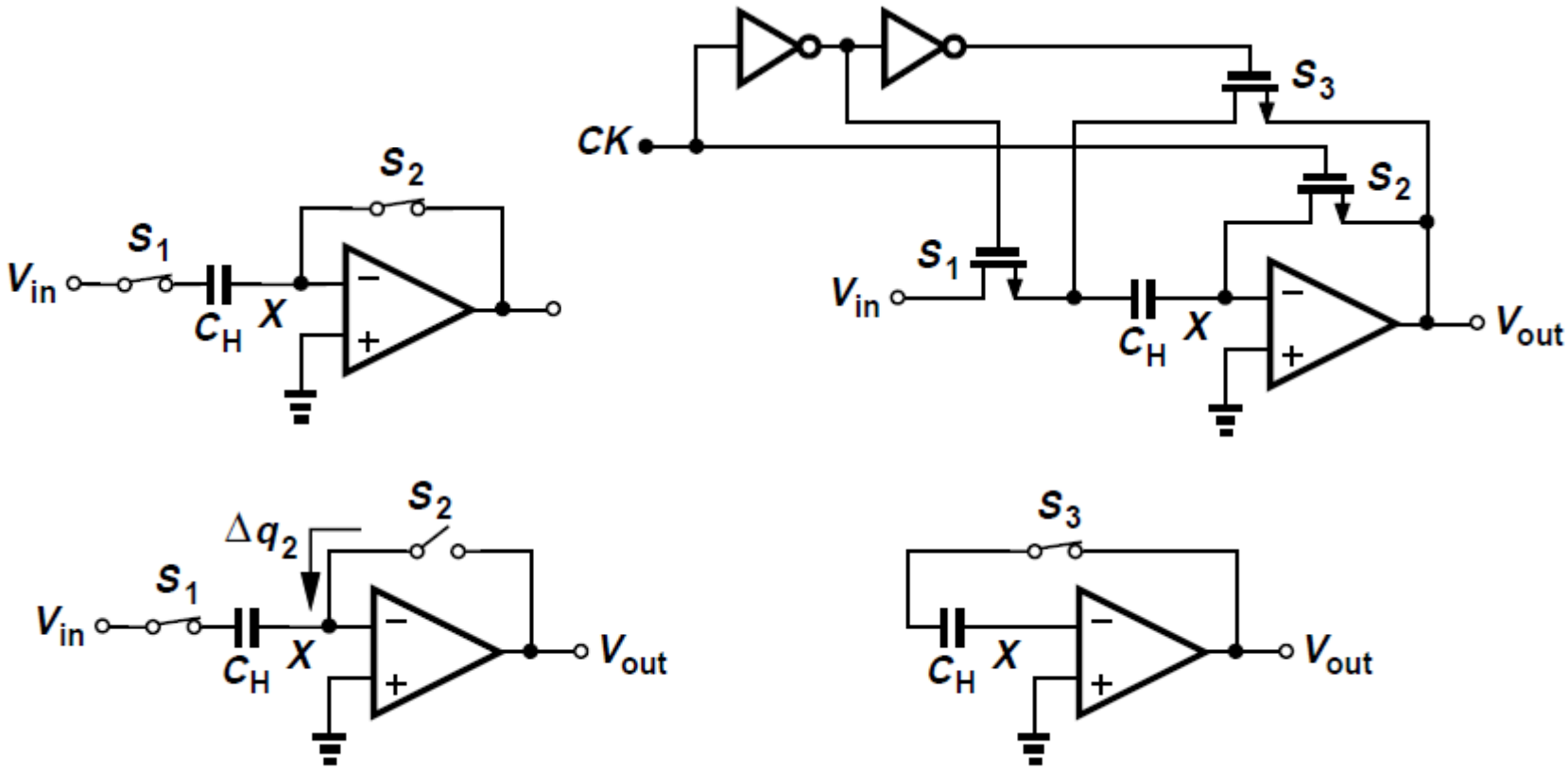


(b)



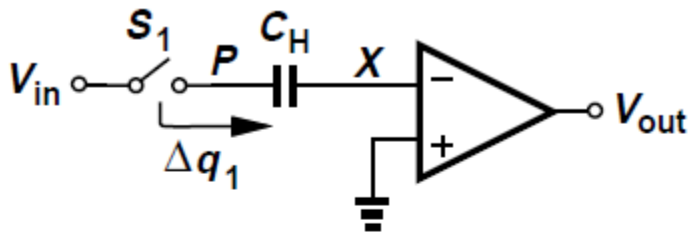
(c)

Early Sampling

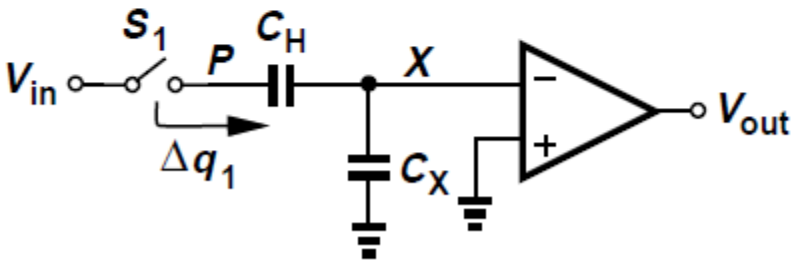


- S2 turning OFF a little earlier than S1
- Reduce signal dependent switching error

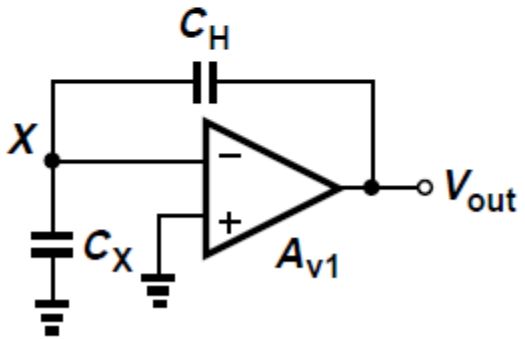
Switching Error



(a)



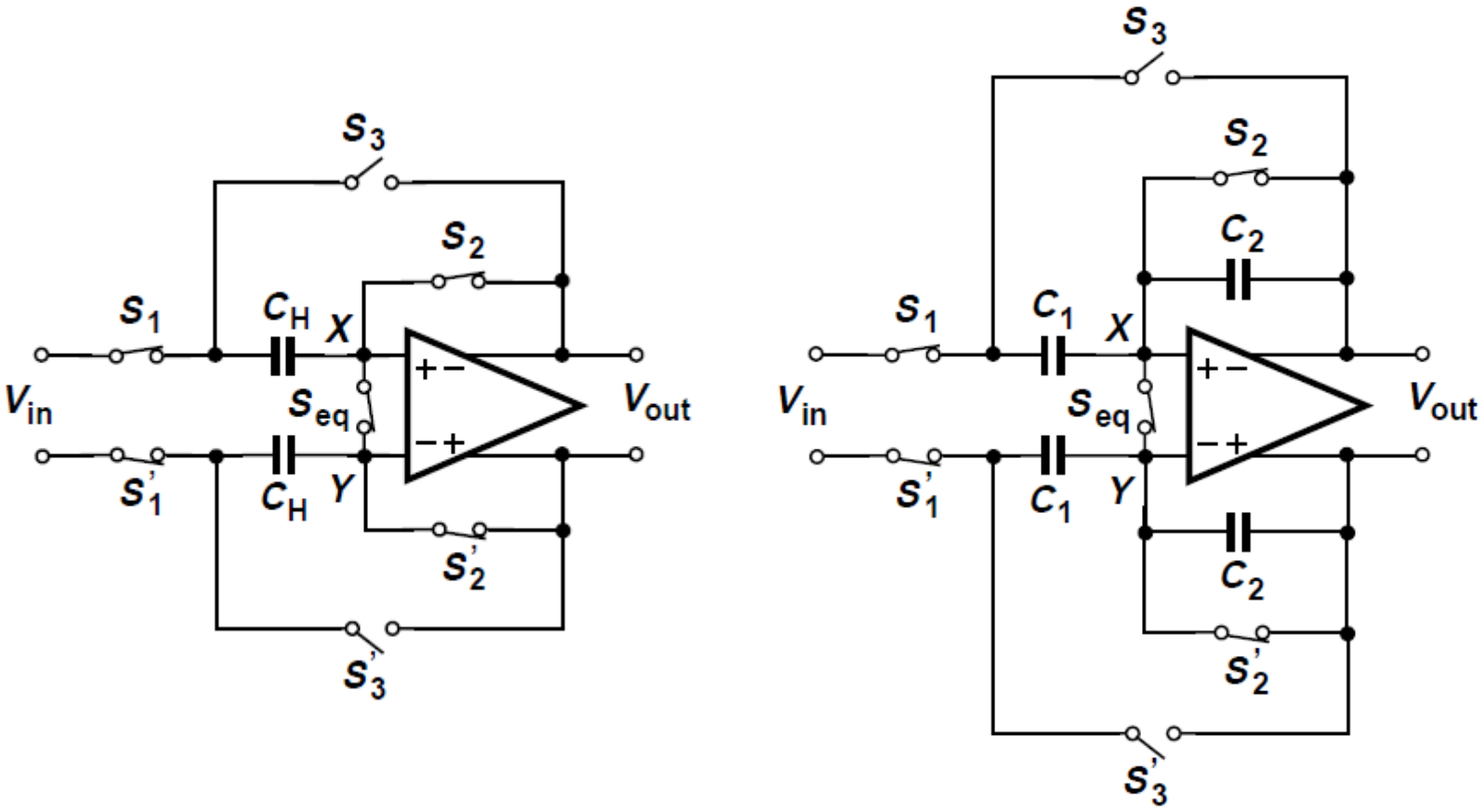
(b)



(c)

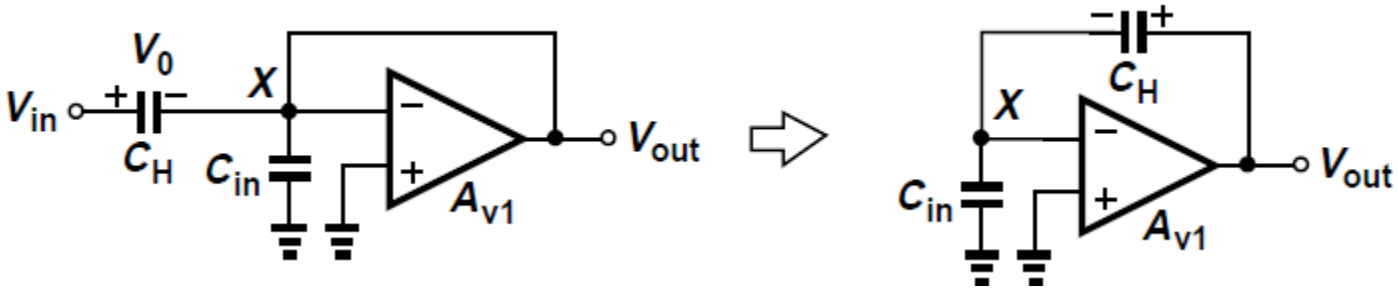
- V_X is floating by turning off S2, and define the charge on C_H
- S1 turning OFF will not change the charge on C_H

Differential Realization



- S_{eq} turning OFF a little after S2 and earlier than S1
- To solve the mismatch of S2 and S2'

Finite Gain Effect

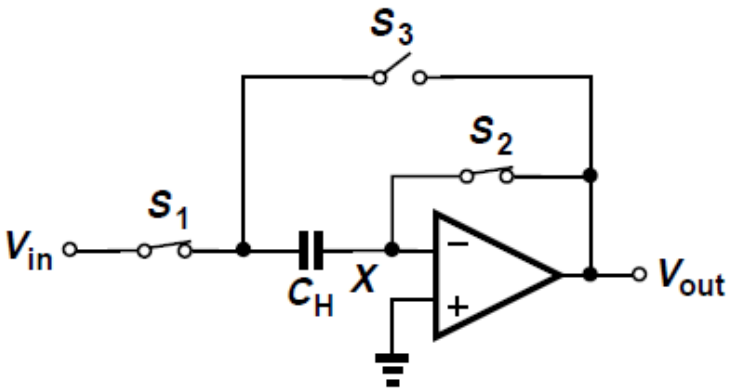


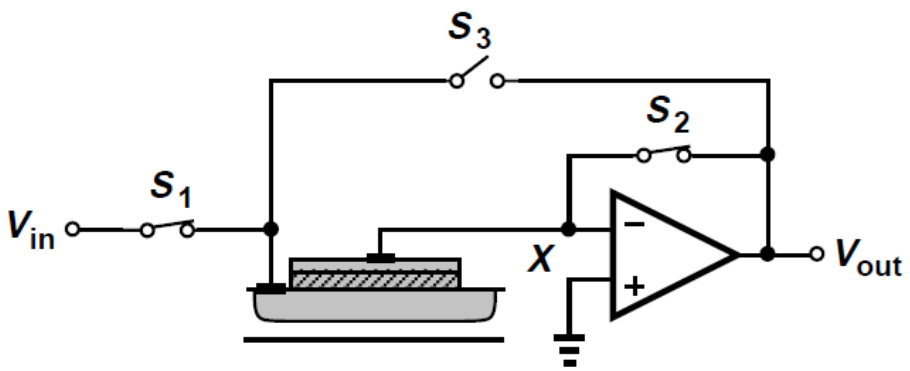
$$V_X = \frac{V_X}{A_{v1}} = 0 \qquad V_X = -\frac{V_{out}}{A_{v1}}$$

$$Q[n] = C_H(0 - V_{in}) = C_{in}V_X + C_H(V_X - V_{out}) = Q[n+1]$$

$$V_{out} = \frac{V_{in}}{1 + \frac{1}{A}\left(1 + \frac{C_{in}}{C_H}\right)} \approx V_{in}\left[1 - \frac{1}{A}\left(1 + \frac{C_{in}}{C_H}\right)\right]$$

Bottom Plate Sampling

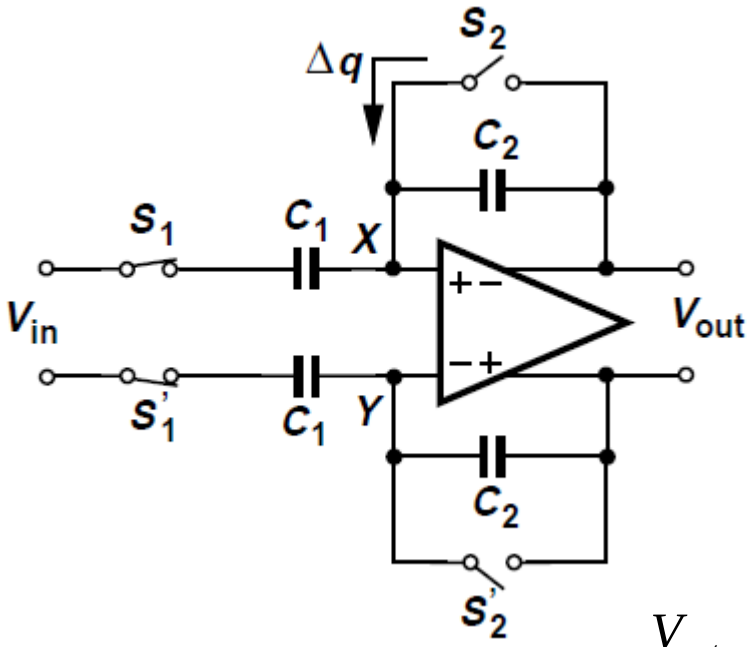




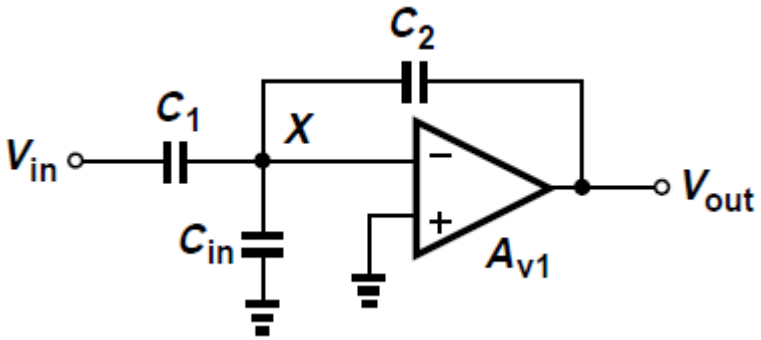
- Bottom plate sampling
- Minimize C_{in}, increase SC gain precision

SC Gain Stage

Early sampling



Finite gain



$$\frac{V_{out}}{V_{in}} = \frac{-C_1}{C_2 + \frac{C_2 + C_1 + C_{in}}{A}} \approx -\frac{C_1}{C_2}\left(1 - \frac{C_2 + C_1 + C_{in}}{C_2}\frac{1}{A}\right)$$

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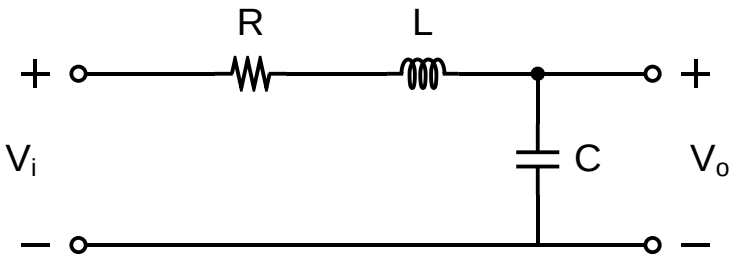
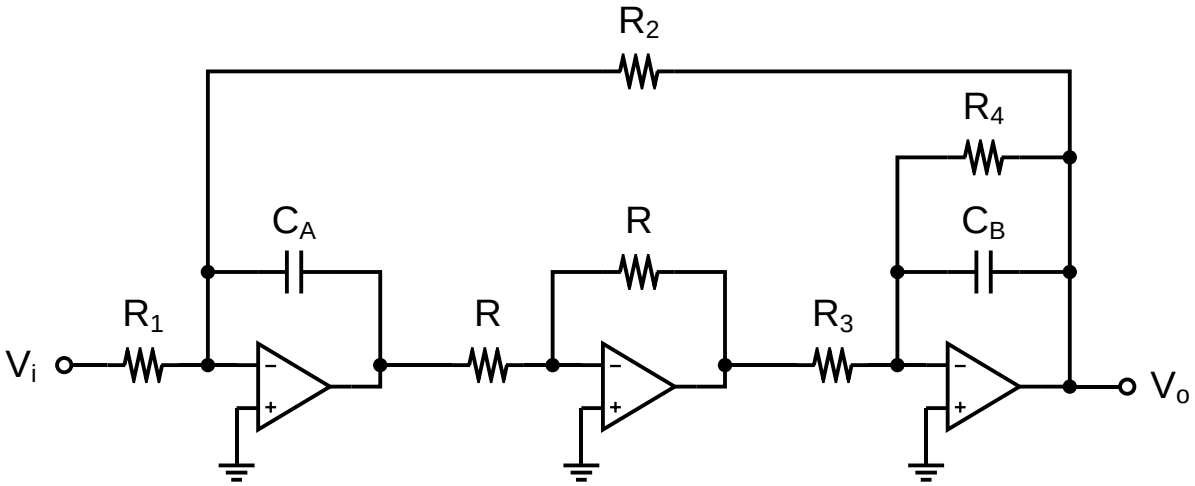
CT Filter

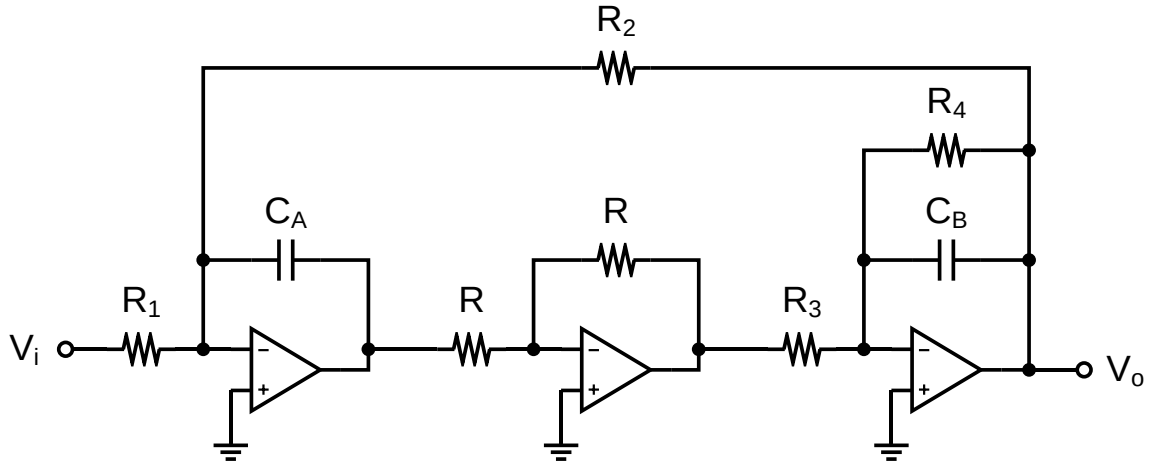


RLC prototype

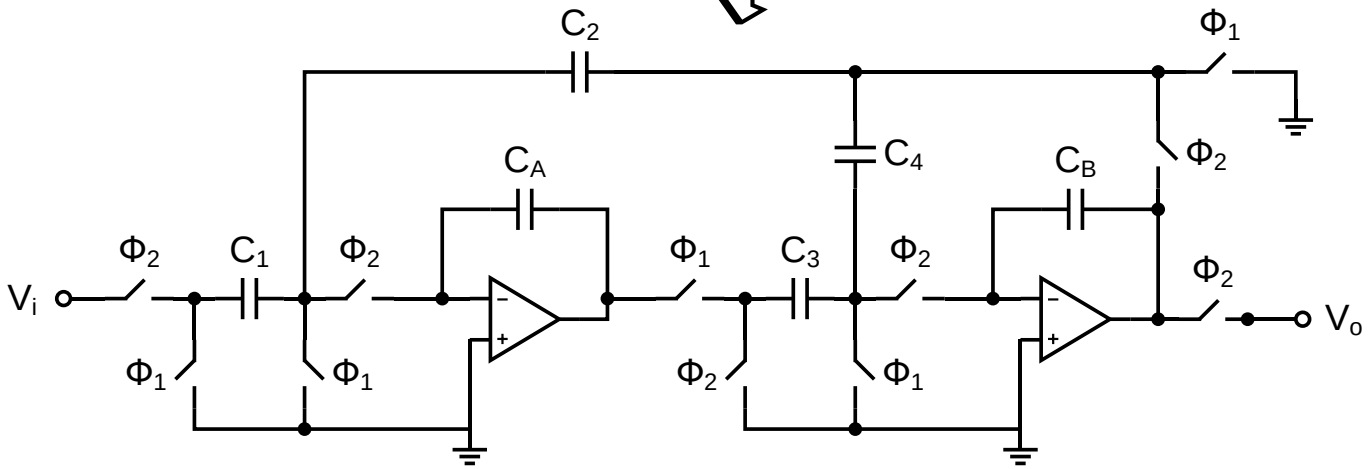


Active-RC
Tow-Thomas
CT biquad

SC DT Filter

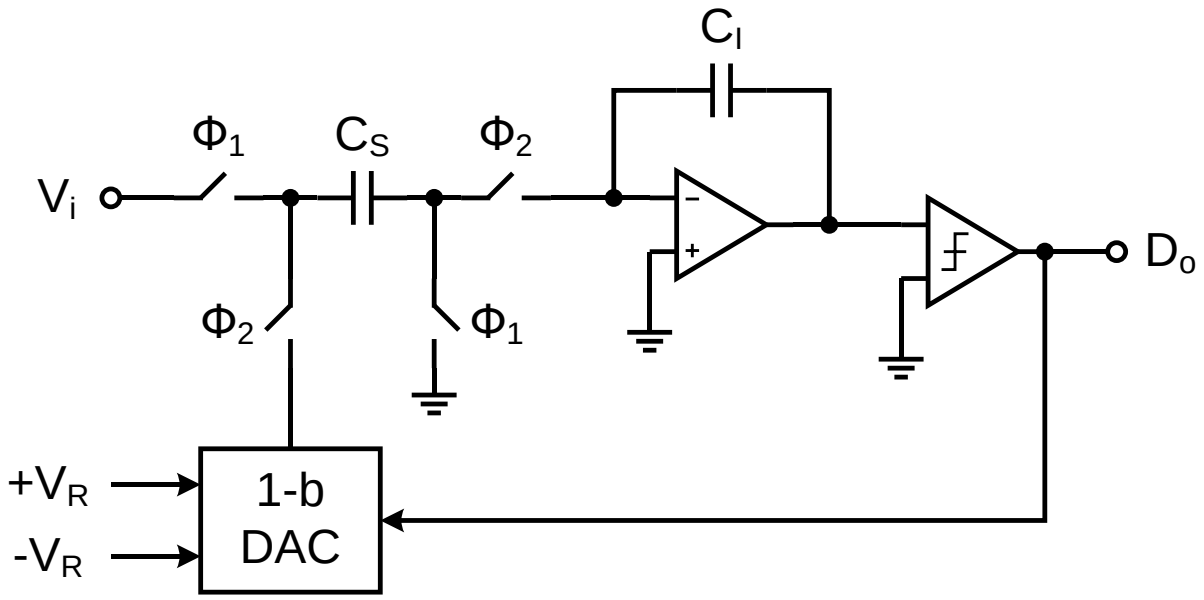


Active-RC
Tow-Thomas
CT biquad



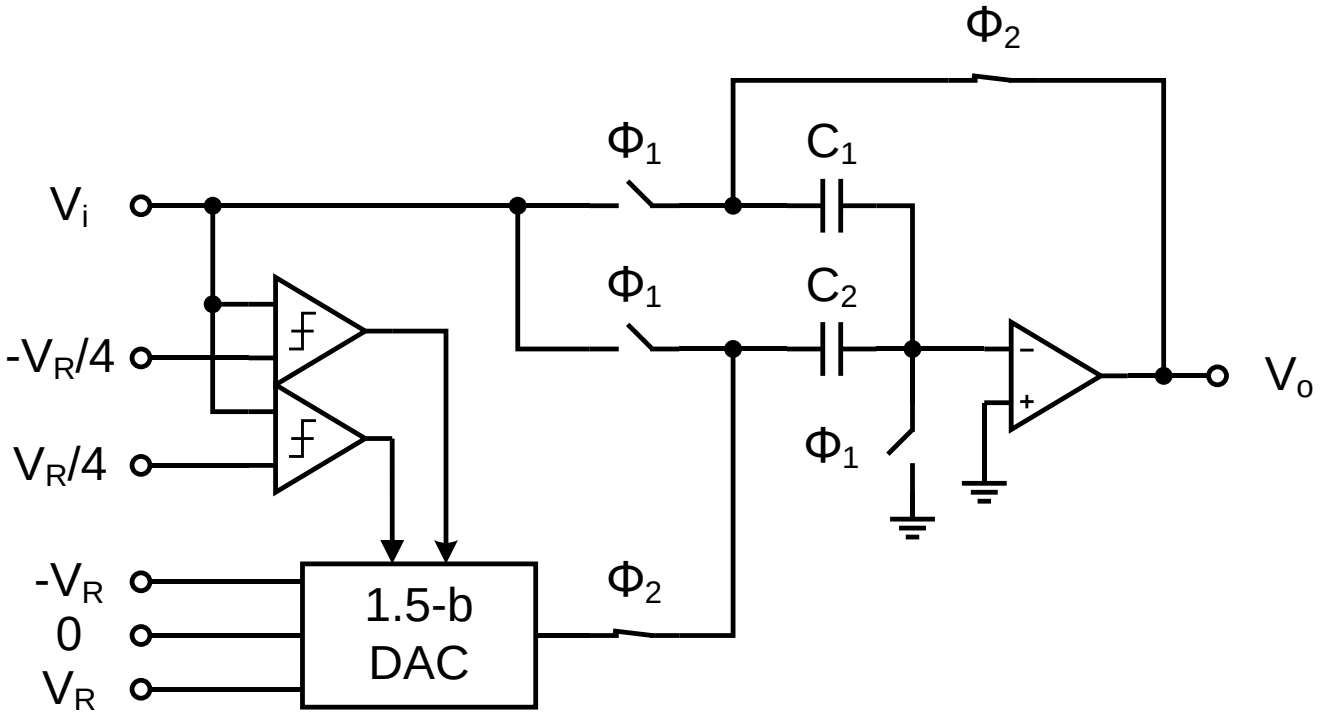
SC DT
biquad

Sigma-Delta (ΣΔ) Modulator



DTI + 1-bit comparator + 1-bit DAC = first-order ΣΔ ADC

Pipelined ADC

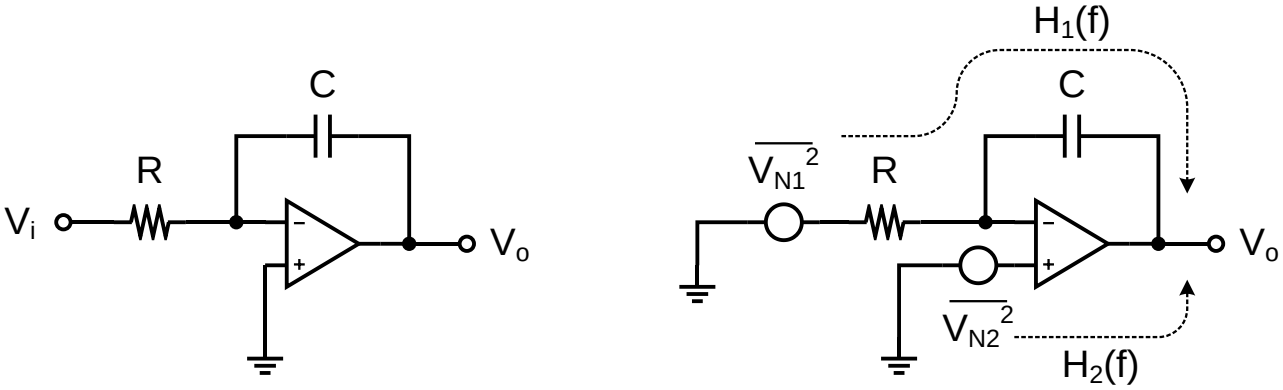


SC amplifier + 2 comparators + 3-level DAC = 1.5-bit pipelined ADC

Outline

- 6.1 Introduction
- 6.2 Switched-Capacitor Circuit
- 6.3 SC Application
- 6.4 Noise in SC
- 6.5 Non-ideal Effects in SC
- 6.6 Practical Issues

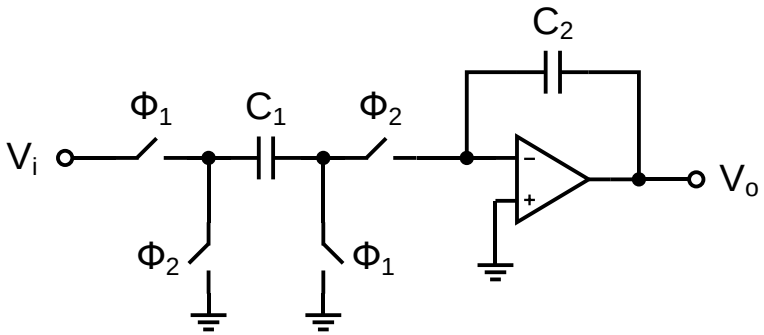
Noise of CT Integrator



$$\overline{V_{oN}^{\,2}} = \int \frac{\overline{V_{N1}^{\,2}}}{\Delta f}(f)\cdot\left|H_1(f)\right|^2 df + \int \frac{\overline{V_{N2}^{\,2}}}{\Delta f}(f)\cdot\left|H_2(f)\right|^2 df + \cdots$$

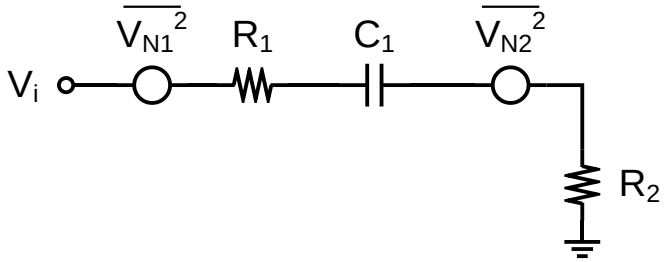
Noise in CT circuits can be simulated with SPICE (.noise)

Noise of SC Integrator



SC circuits are **NOT** noise-free! Switches and op-amps introduce noise.

Sampling (Φ_1) Ideal Voltage Source



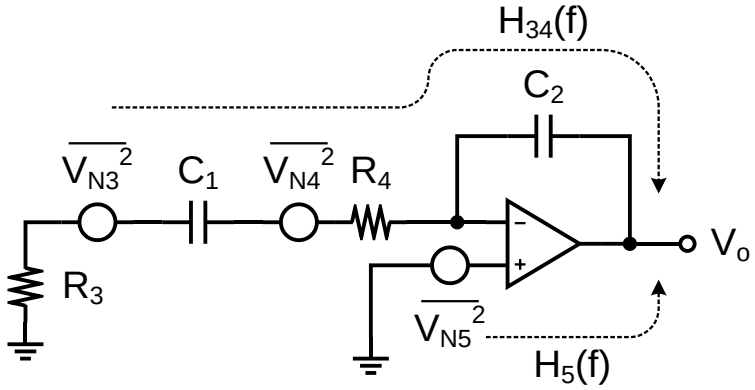
$$\overline{V_N^{\,2}}(\varphi 1) = \int_0^{\infty} \left[\frac{\overline{V_{N1}^{\,2}}}{\Delta f}(f) + \frac{\overline{V_{N2}^{\,2}}}{\Delta f}(f) \right] \cdot \left| H_1(f) \right|^2 df$$

$$= \int_0^{\infty} \left[4kTR_1 + 4kTR_2 \right] \cdot \left| \frac{1}{1 + j2\pi f \cdot (R_1 + R_2) C} \right|^2 df$$

$$= \frac{kT}{C}$$

- Noise is indistinguishable from signal after sampling
- The noise acquired by C_1 will be amplified in Φ_2 just like signal

Integration (Φ_2)

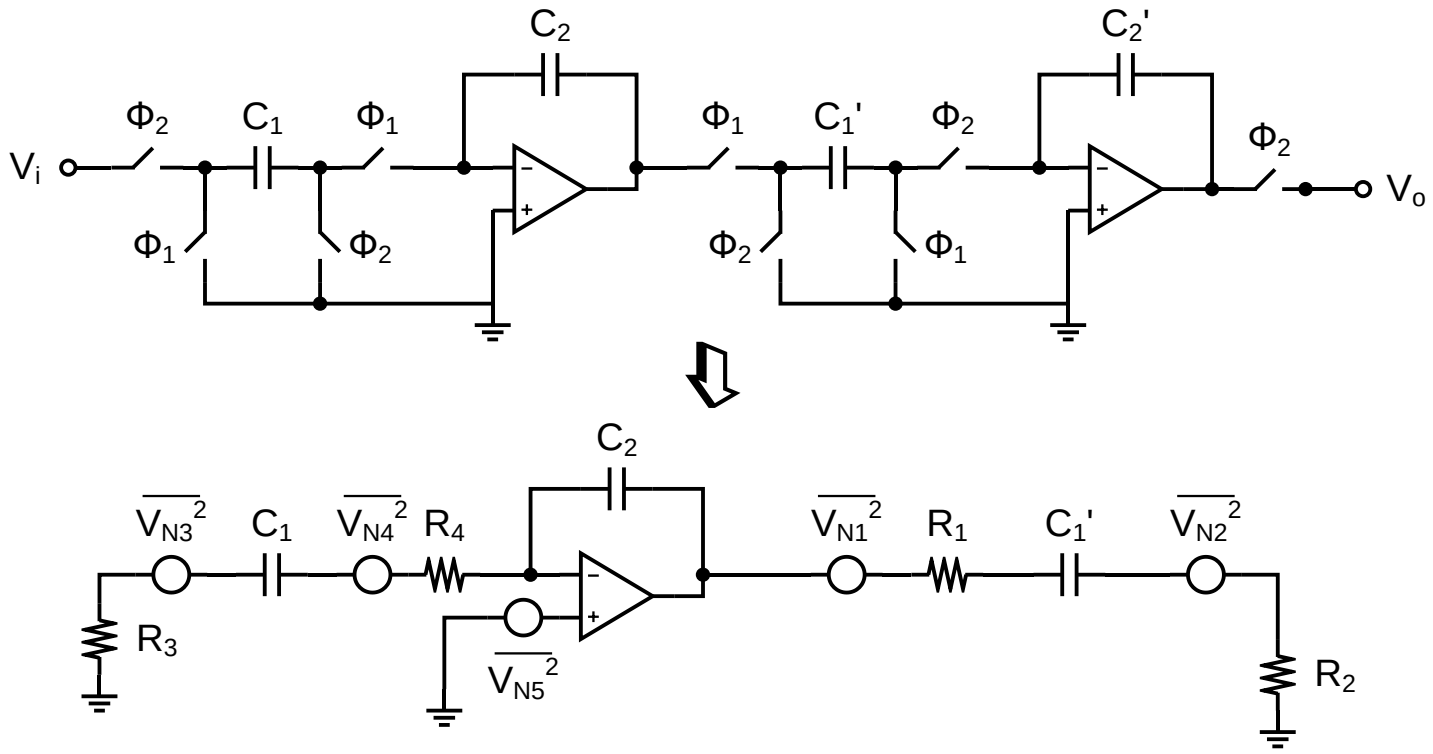


$$\overline{V_N{}^2}(\varphi 2) = \int \left[\frac{\overline{V_{N3}{}^2}}{\Delta f}(f) + \frac{\overline{V_{N4}{}^2}}{\Delta f}(f) \right] \cdot \left| H_{34}(f) \right|^2 df + \int \frac{\overline{V_{N5}{}^2}}{\Delta f}(f) \cdot \left| H_5(f) \right|^2 df + \cdots$$

$$\boxed{\overline{V_{oN}{}^2} = \left(\frac{C_1}{C_2} \right)^2 \cdot \overline{V_N{}^2}(\phi 1) + \overline{V_N{}^2}(\phi 2)}$$

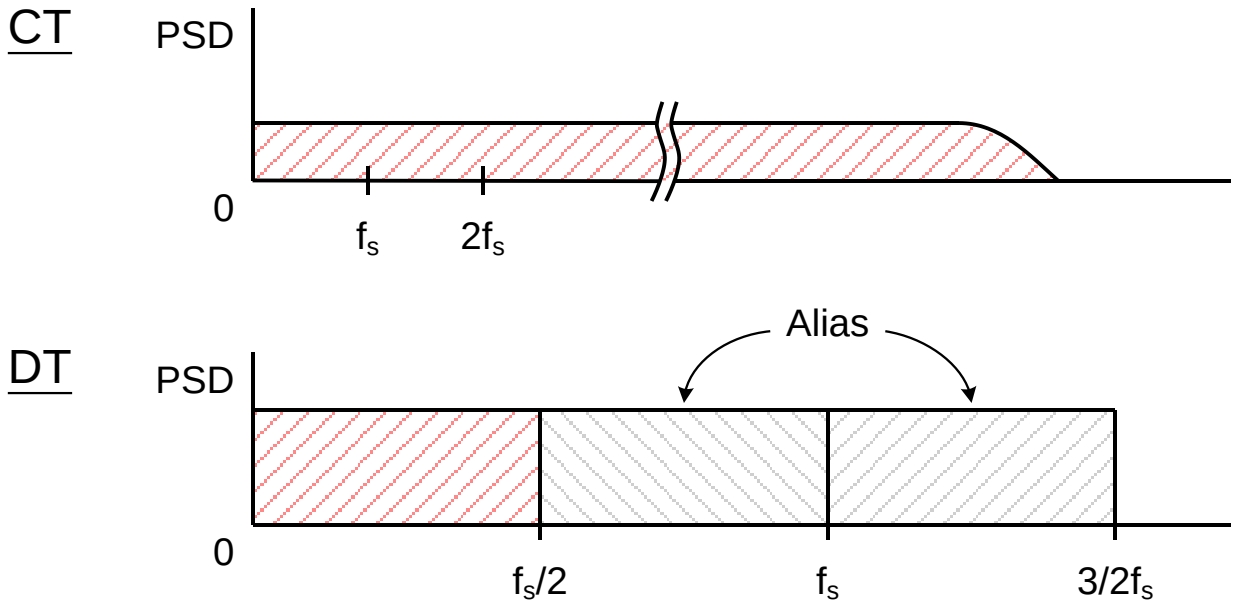
No simulator can directly simulate the aggregated output noise!

Sampling (Φ_1) Noise – Cascaded Stages



- Finite op-amp BW limits the noise bandwidth, resulting in less overall kT/C noise (noise filtering).
- But parasitic loop delay may introduce peaking in freq. response, resulting in more integrated noise (noise peaking).

Sampled Noise Spectrum



- Total integrated noise power remains constant
- SNR remains constant

Outline

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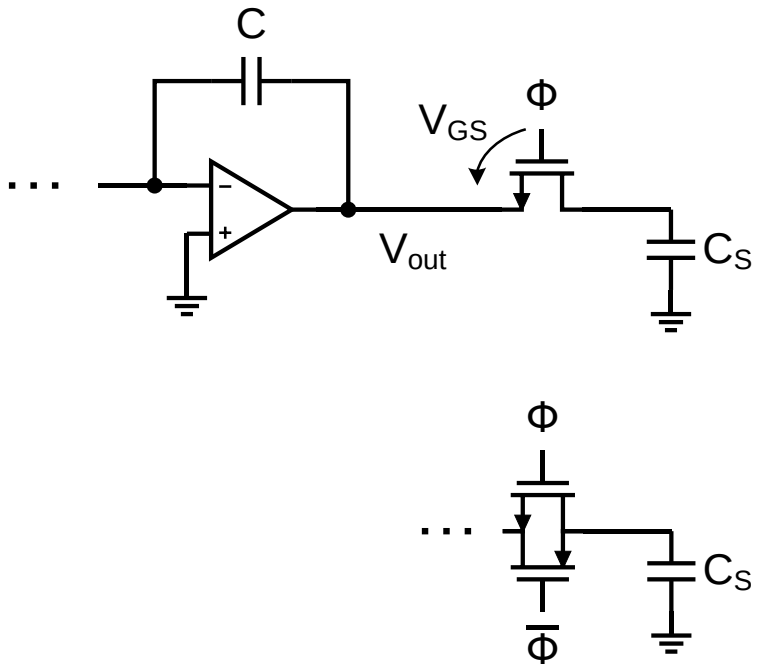
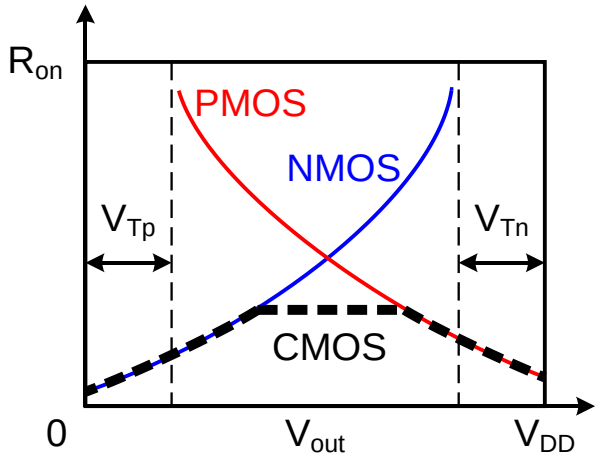
Nonideal Effects in SC Circuits

- Capacitors (poly-poly, metal-metal, MIM, MOM, sandwich, gate cap, accumulation-mode gate cap, etc.)
  - PP, MIM, and MOM are linear up to 14-16 bits (nonlinear voltage coefficients negligible for most applications)
  - Gate caps are typically good for up to 8-10 bits
- Switches (MOS transistors)
  - Nonzero on-resistance (voltage dependent)
  - (Nonlinear) stray capacitance added (C_{gs}, C_{gd}, C_{gb}, C_{db}, C_{sb})
  - Switch-induced sampling errors (charge injection, clock feedthrough, junction leakage, drain-source leakage, and gate leakage)
- Operational amplifiers
  - Offset
  - Finite-gain effects (voltage dependent)
  - Finite bandwidth and slew rate (measured by settling speed)

Nonzero On-Resistance

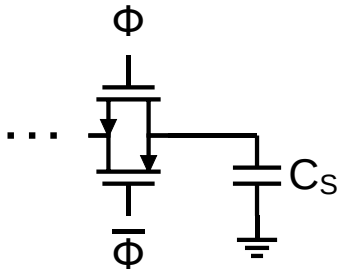




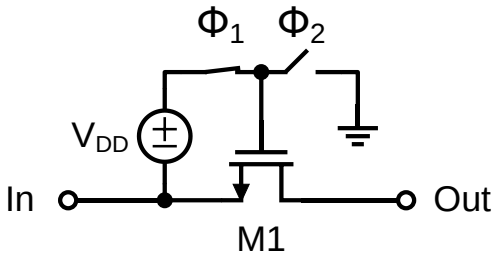
$$R_{on}^{-1} = \mu C_{ox} \frac{W}{L}\left(V_{DD} - V_{th} - V_{out}\right)$$

- FET channel resistance (thus tracking bandwidth) depends on signal level
- Usually $(R_{on}C_S)^{-1} \geq (3\text{-}5)\cdot\omega_{-3dB}$ of closed-loop op-amp for settling purpose

Clock Bootstrapping



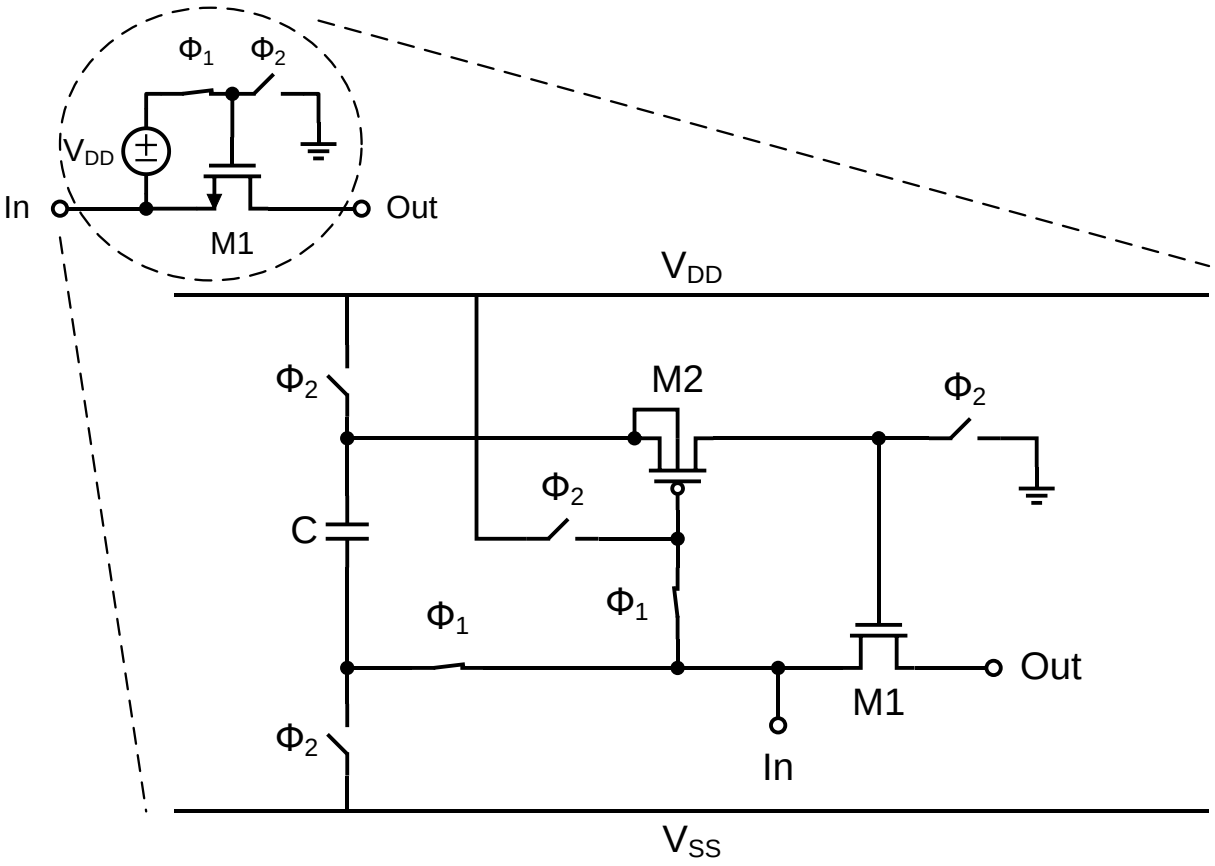
CMOS



Bootstrapped NMOS

- Small on-resistance leads to large switches → large parasitic caps and large clock buffers
- Clock bootstrapping keeps V_{GS} of the switch constant → constant on-resistance (body effect?) and less parasitics w/o the PMOS

Simplified Clock Bootstrapper



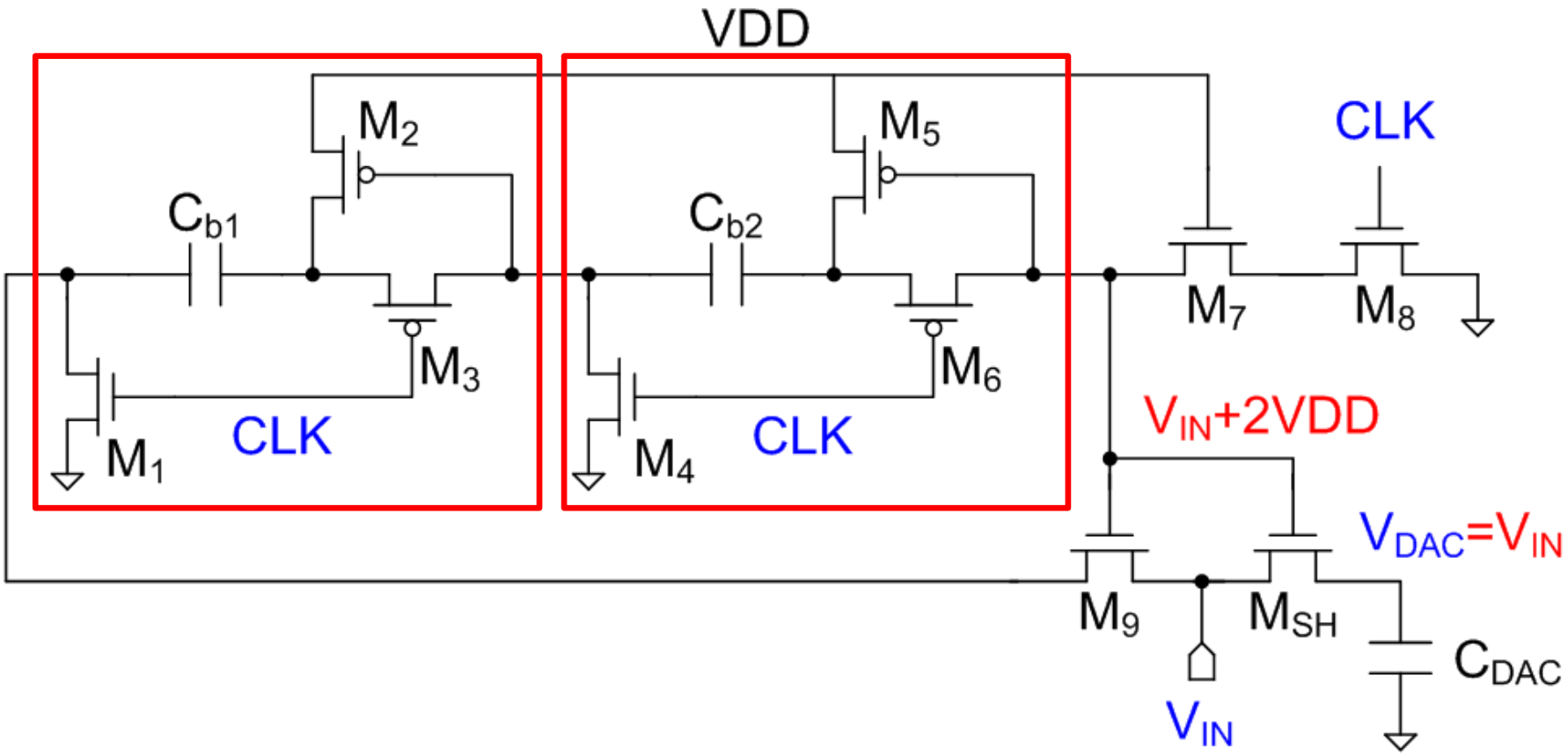
Pros

- Linearity
- Bandwidth

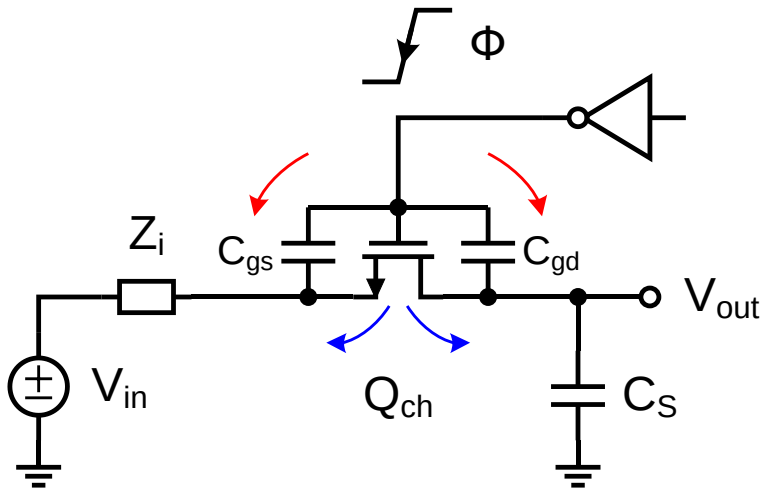
Cons

- Device reliability
- Complexity

Double Bootstrapper



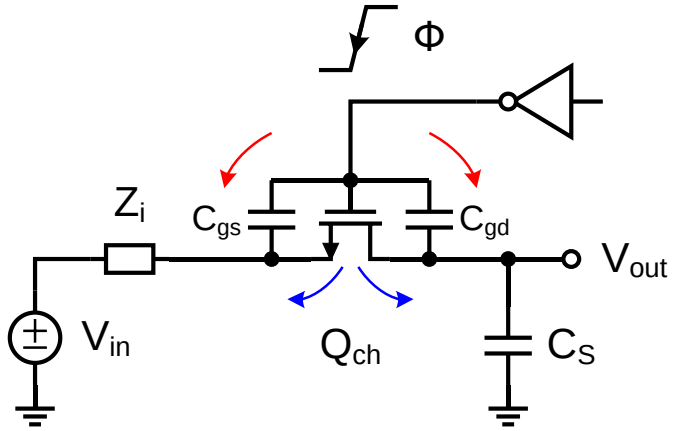
Switch-Induced Errors

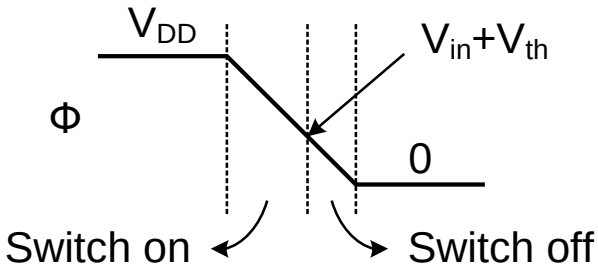


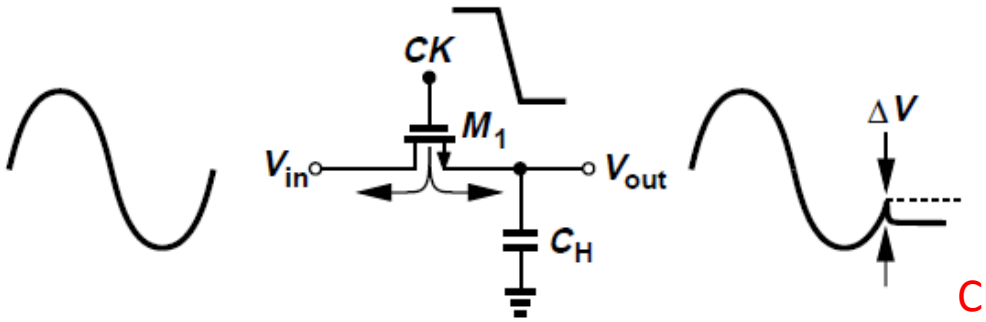
- Clock feedthrough
- Charge injection

Channel charge injection and clock feedthrough (on drain side) result in charge trapped on C_S after switch is turned off.

Clock Feedthrough / Charge Injection



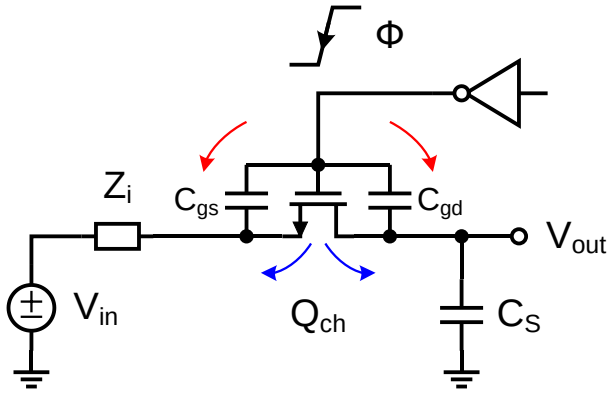




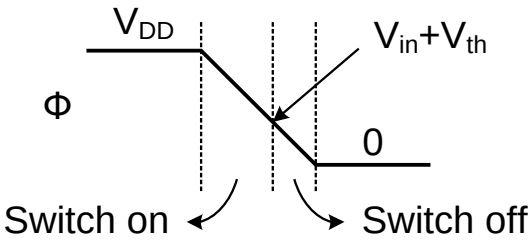
Charge Injection

- Both phenomena sensitive to Z_i, C_S, and clock rise/fall time
- Offset, gain error, and nonlinearity introduced to the sampling
- Clock feedthrough can be simulated by SPICE, but charge injection **cannot** be simulated with lumped transistor models

Clock Rise/Fall-Time Dependence

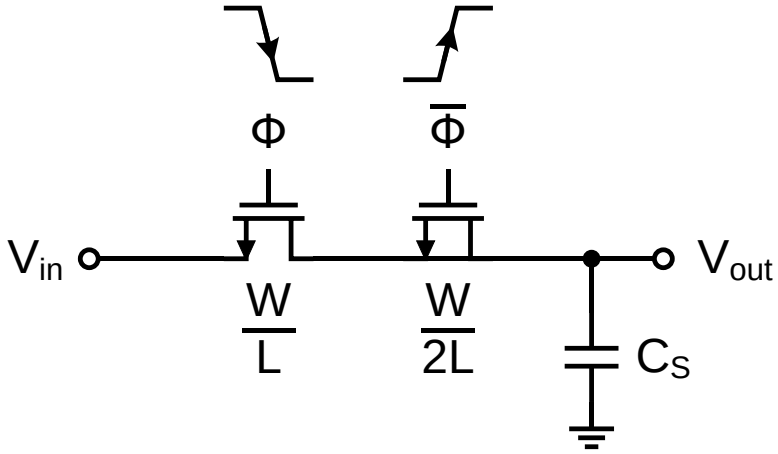


$$Q_{ch} = C_{ox}WL\left(V_{DD} - V_{th} - V_{in}\right)$$



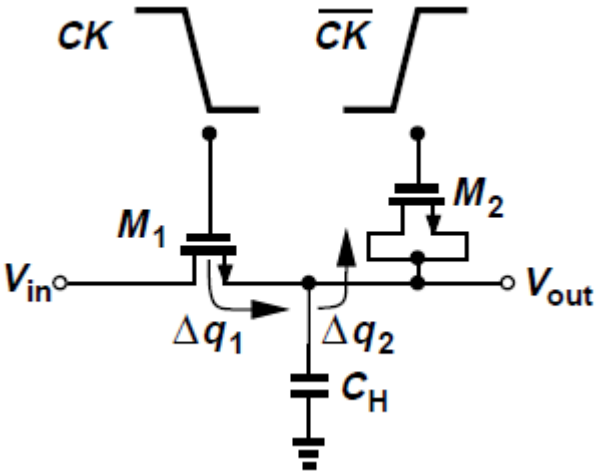
	Clock feedthrough	Charge injection
Fast turn-off	$\Delta V = -\frac{C_{gs}}{C_{gs}+C_S}V_{DD}$	$\Delta V = -\frac{C_{ox}WL\left(V_{DD}-V_{th}-V_{in}\right)}{2\left(C_{gs}+C_S\right)}$
Slow turn-off	$\Delta V = -\frac{C_{gs}}{C_{gs}+C_S}\left(V_{in}+V_{th}\right)$	$\Delta V = 0$

Dummy Switch



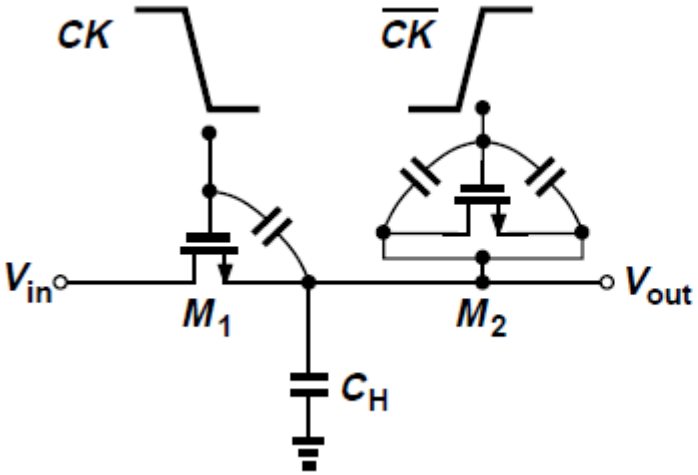
- Difficult to achieve precise cancellation due to the nonlinear dependence of ΔV on Z_i, C_S, and clock rise/fall time
- Sensitive to the phase alignment between Φ and Φ_

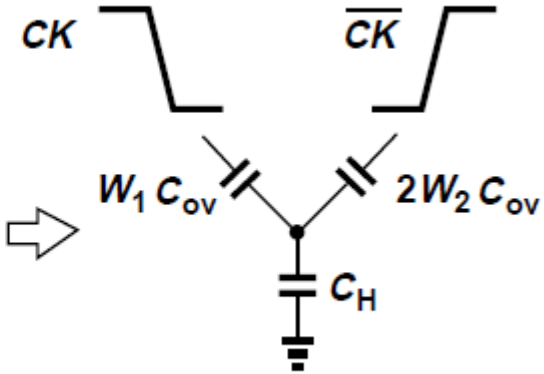
Dummy Switch



Charge injection cancellation

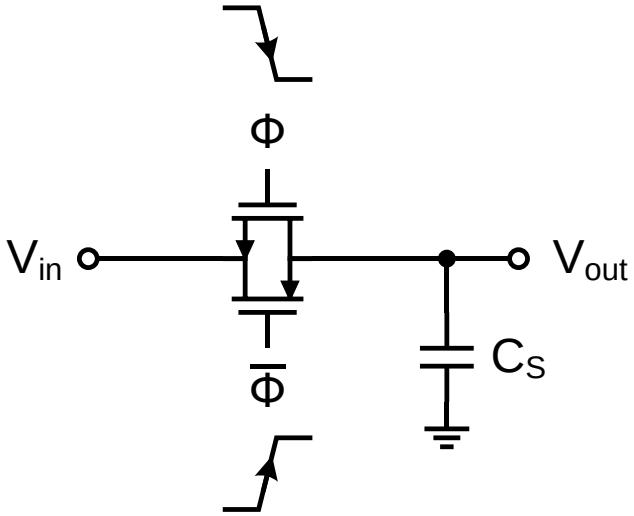
(Signal dependent)





Clock feedthrough cancellation (Depend on W/L only)

CMOS Switch

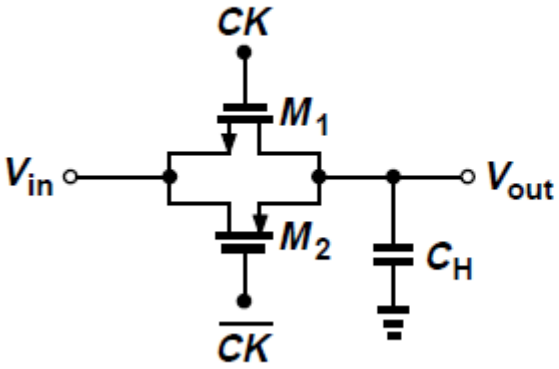


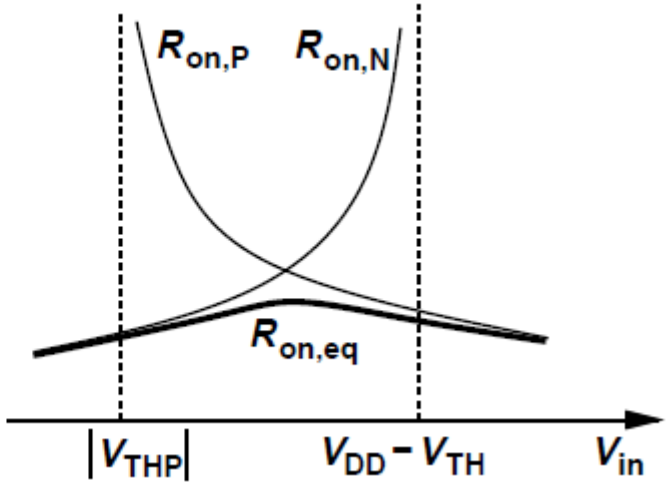
Same size for

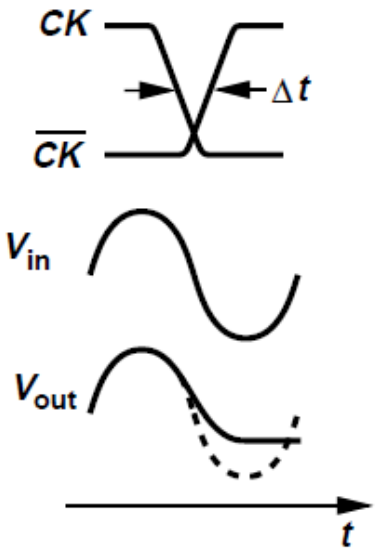
P and N FETs

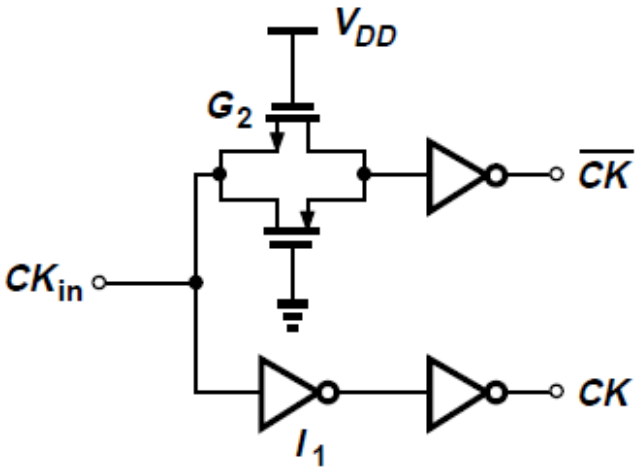
- Very sensitive to phase alignment between Φ and Φ_
- Subject to threshold mismatch between PMOS and NMOS
- Exact cancellation occurs only for one specific V_{in} (which one?)

CMOS Switch

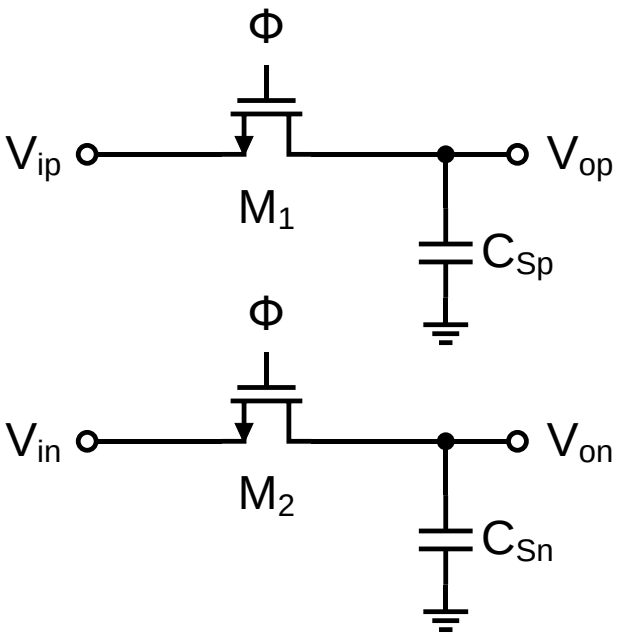

CK
M1
Vin
Vout
M2
CH
CK

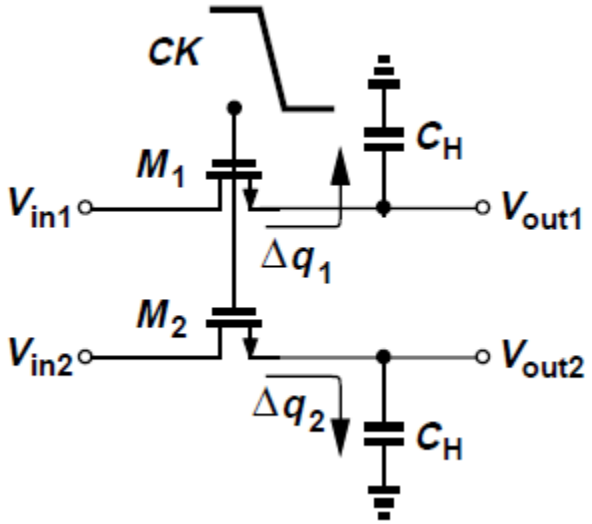

Ron,P
Ron,N
Ron,eq
|VTHP|
VDD - VTH
Vin


CK
Δt
CK
Vin
Vout
t


VDD
G2
CK
CKin
CK
I1

Differential Signaling





Balanced diff. input

- Signal-independent errors (offset) and even-order distortions cancelled
- Gain error and odd-order nonlinearities remain

Switch Performance

On-resistance: $$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{th} - V_i\right)} = \frac{L^2}{\mu C_{ox} WL\left(V_{DD} - V_{th} - V_i\right)} = \frac{L^2}{\mu Q_{ch}}$$

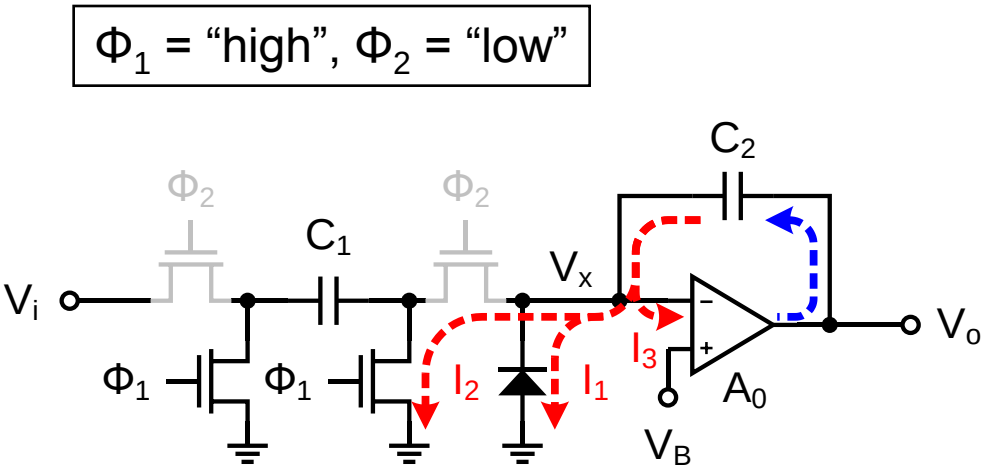
Bandwidth: $$BW \approx \frac{1}{R_{on} C_S} = \frac{\mu Q_{ch}}{L^2 C_S}$$

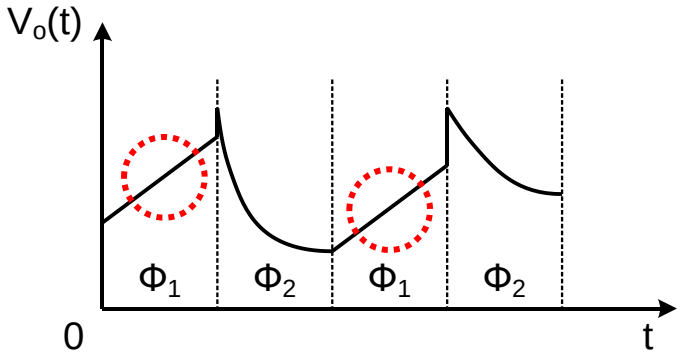
Charge injection: $$\Delta V \approx \frac{1}{2}\frac{Q_{ch}}{C_S}$$

Performance FoM: $$\boxed{\frac{\Delta V}{BW} \approx \frac{1}{2}\frac{Q_{ch}}{C_S} \cdot \frac{L^2 C_S}{\mu Q_{ch}} = \frac{L^2}{2\mu}}$$

Technology scaling improves switch performance!

Leakage in SC Circuits





- **I1** – diode leakage (existing in the old days too)
- **I2** – sub-threshold drain-source leakage of summing-node switch
- **I3** – gate leakage (FN tunneling) of amplifier input transistors
- Leakage currents are highly temperature- and process-dependent; the lower limit of clock frequency is often determined by leakage

Gate Leakage

$$I_{GS} \propto WL \cdot \exp\left(-t_{ox}\right) \cdot \exp\left(V_{GS}\right)$$

- Direct tunneling through the thin gate oxide
- Short-channel MOSFET behaves increasingly like BJT's
- Violates the high-impedance assumption of the summing node

Switch Size Optimization

- To minimize switch-induced error voltages, small transistor size, slow turn-off, low source impedance should be used.
- For fast settling (high-speed design), large W/L should be used, and errors will be inevitably large as well.

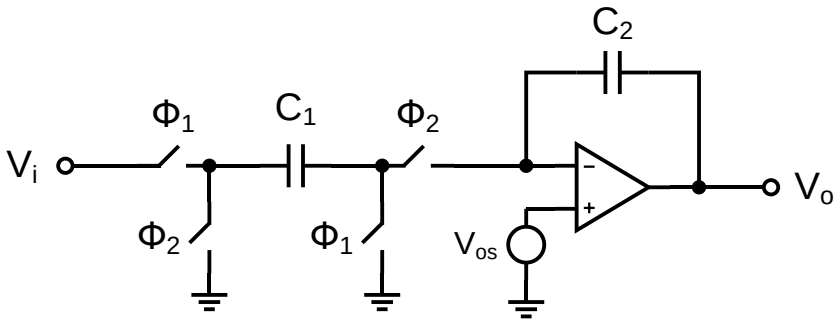
Guidelines

- Always use minimum channel length for switches as long as leakage allows.
- For a given speed, switch sizes can be optimized w/ simulation.
- Be aware of the limitations of simulators (SPICE etc.) using lumped device models.

Nonideal Effects of Op-Amps

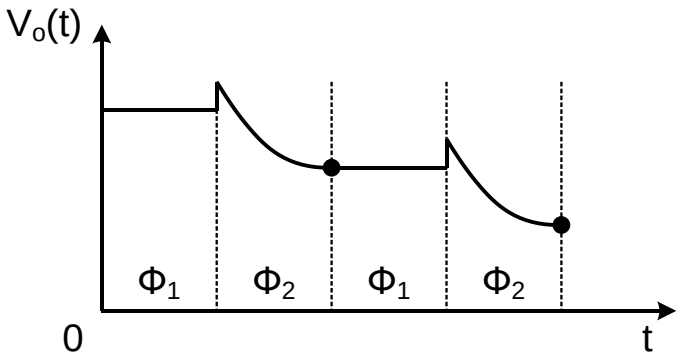
- Offset
- Finite-gain effects (voltage dependent)
- Finite bandwidth and slew rate (measured by settling speed)

Offset Voltage



$$\sum Q(\varphi_1) = V_i(n)C_1 + [V_o(n) - V_{os}]C_2$$

$$\sum Q(\varphi_2) = -V_{os}C_1 + [V_o(n+1) - V_{os}]C_2$$

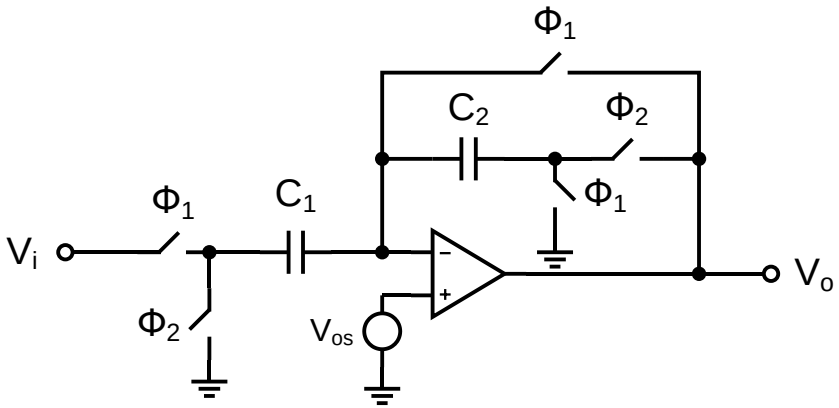


$V_i = 0$

$$V_i = 0 \quad \rightarrow \quad V_o(n+1) - V_o(n) = \left(\frac{C_1}{C_2}\right)V_{os}$$

$$V_o(z) = \frac{C_1}{C_2}\frac{z^{-1}}{1 - z^{-1}}V_i(z)$$

Autozeroing



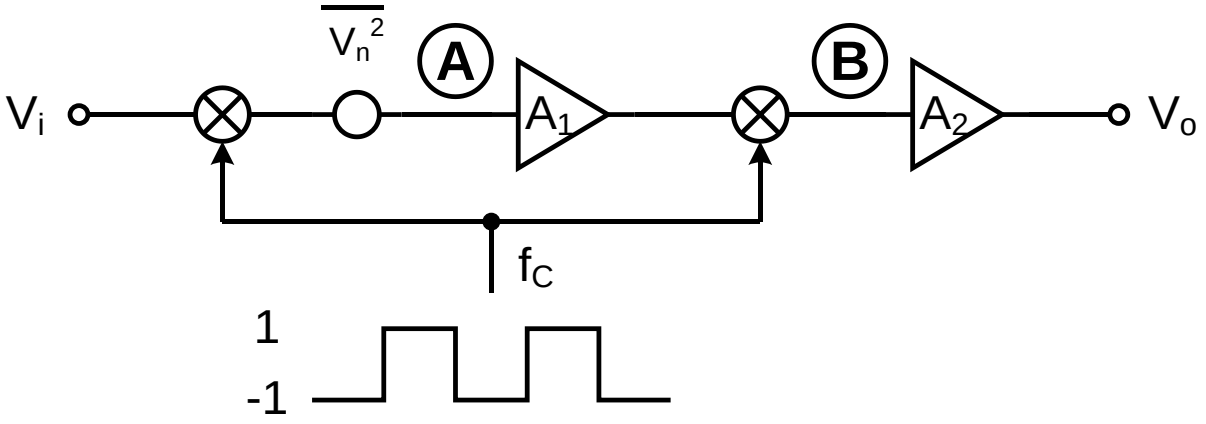
$$\sum Q(\varphi_1) = [V_i(n) - V_{os}]C_1 - V_{os}C_2$$

$$\sum Q(\varphi_2) = -V_{os}C_1 + [V_o(n) - V_{os}]C_2$$

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}$$

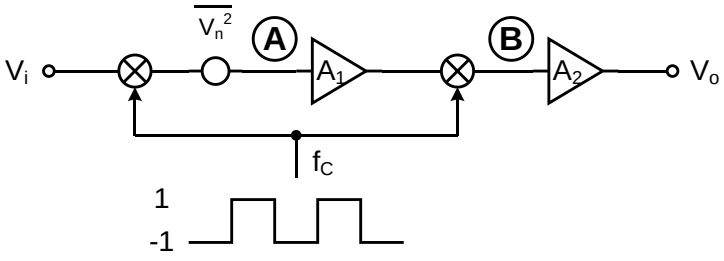
- Also eliminates low-frequency noise, e.g., 1/f noise
- A.k.a. **correlated double sampling** (**CDS**)

Chopper Stabilization

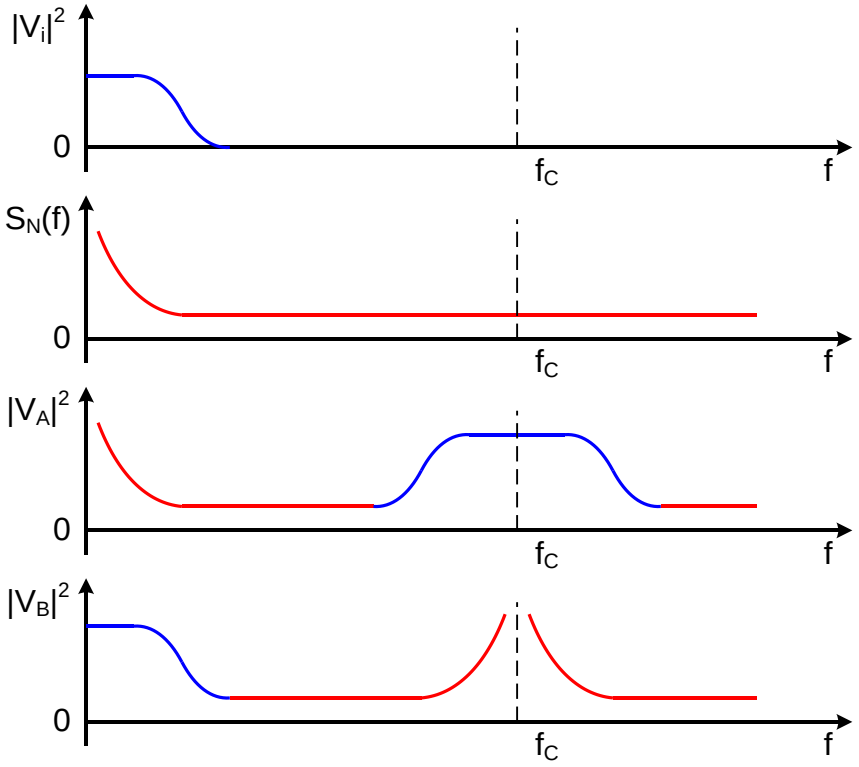


Ref: K. C. Hsieh, P. R. Gray, D. Senderowicz, and D. G. Messerschmitt, “A low-noise chopper-stabilized differential switched-capacitor filtering technique,” *IEEE Journal of Solid-State Circuits*, vol. 16, issue 6, pp. 708-715, 1981.

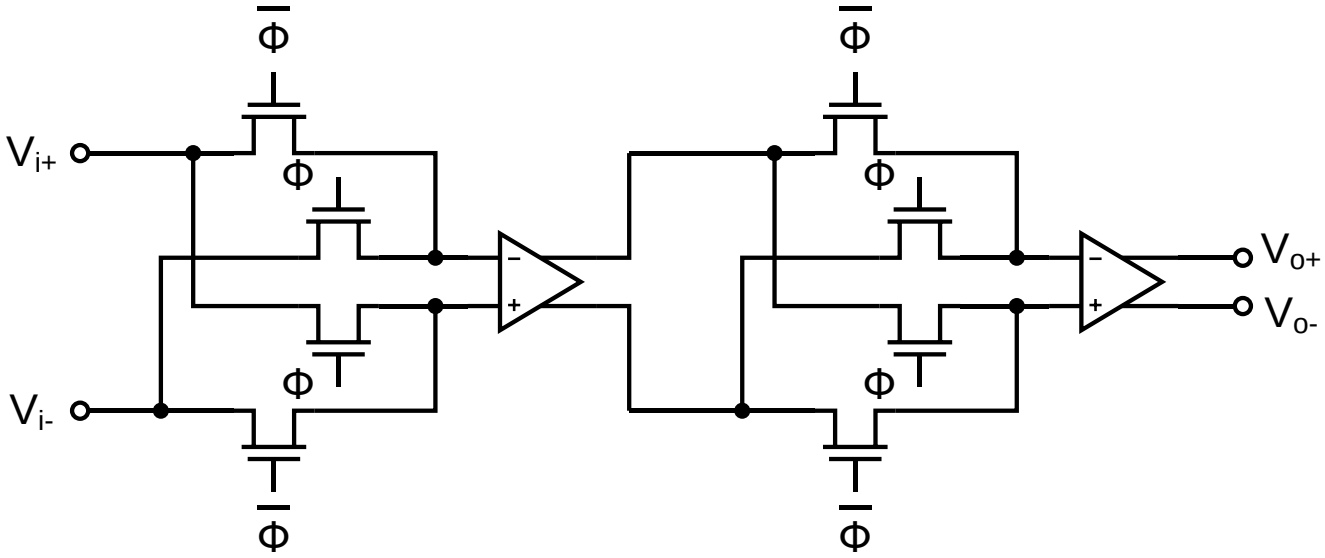
Chopper Stabilization



Also eliminates DC offset voltage of A_1

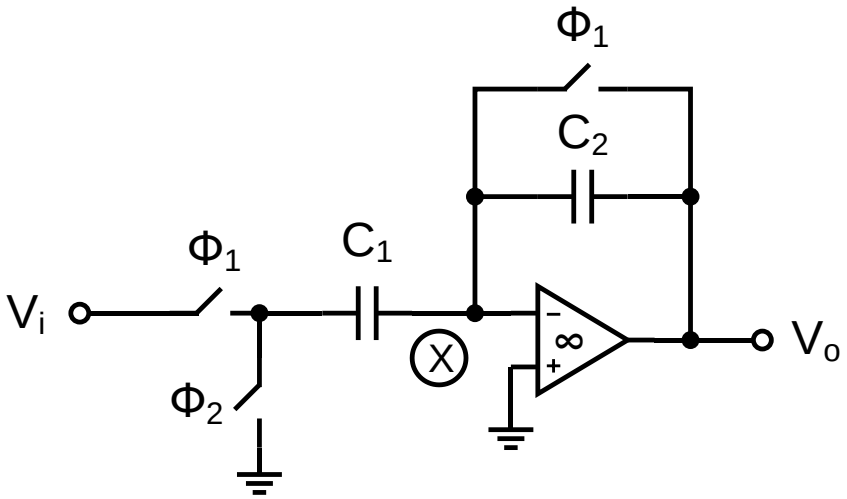


Chopper-Stabilized Diff. Op-Amp



- Integrators/amplifiers can be built using these op-amps
- Some oversampling is useful to facilitate the implementation

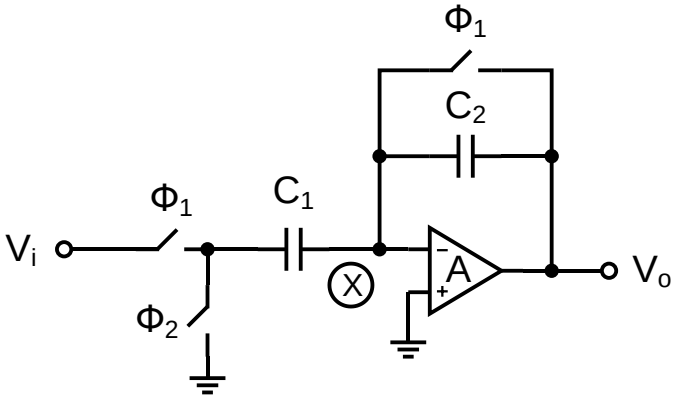
Ideal SC Amplifier



$$A_{CL} = \frac{C_1}{C_2}$$

- Closed-loop gain is determined by the capacitor ratio by design
- But this is assuming X is an ideal summing node (the op-amp is ideal)

Finite-Gain Effect in SC Amplifier



$$A_{CL} = \frac{V_o}{V_i} = \frac{C_1}{C_2} \cdot \frac{1}{1 + \frac{C_1 + C_2}{C_2 A}} \approx \frac{C_1}{C_2} \cdot \left(1 - \frac{C_1 + C_2}{C_2 A}\right)$$

$$\sum Q(\phi_1) = \left[V_i(\phi_1) - V_x(\phi_1)\right] \cdot C_1 + 0 \cdot C_2 \qquad \sum Q(\phi_2) = -V_x(\phi_2) \cdot C_1 + \left[V_o(\phi_2) - V_x(\phi_2)\right] \cdot C_2$$

$$V_x(\phi_1) = V_o(\phi_1) = -V_x(\phi_1) \cdot A \qquad V_o(\phi_2) = -V_x(\phi_2) \cdot A$$

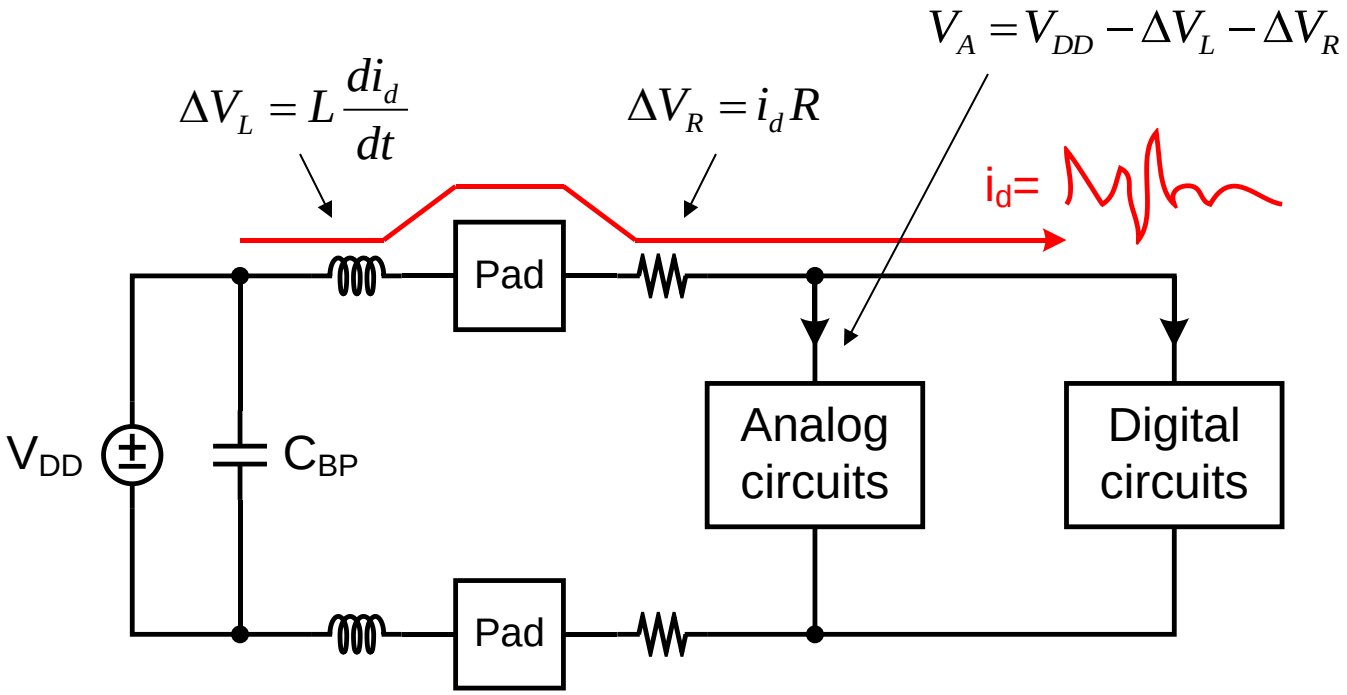
$$\sum Q(\phi_1) = \sum Q(\phi_2) \Rightarrow V_i \cdot C_1 = -V_x \cdot C_1 + (V_o - V_x) \cdot C_2$$

$$V_o = -V_x \cdot A$$

Outline

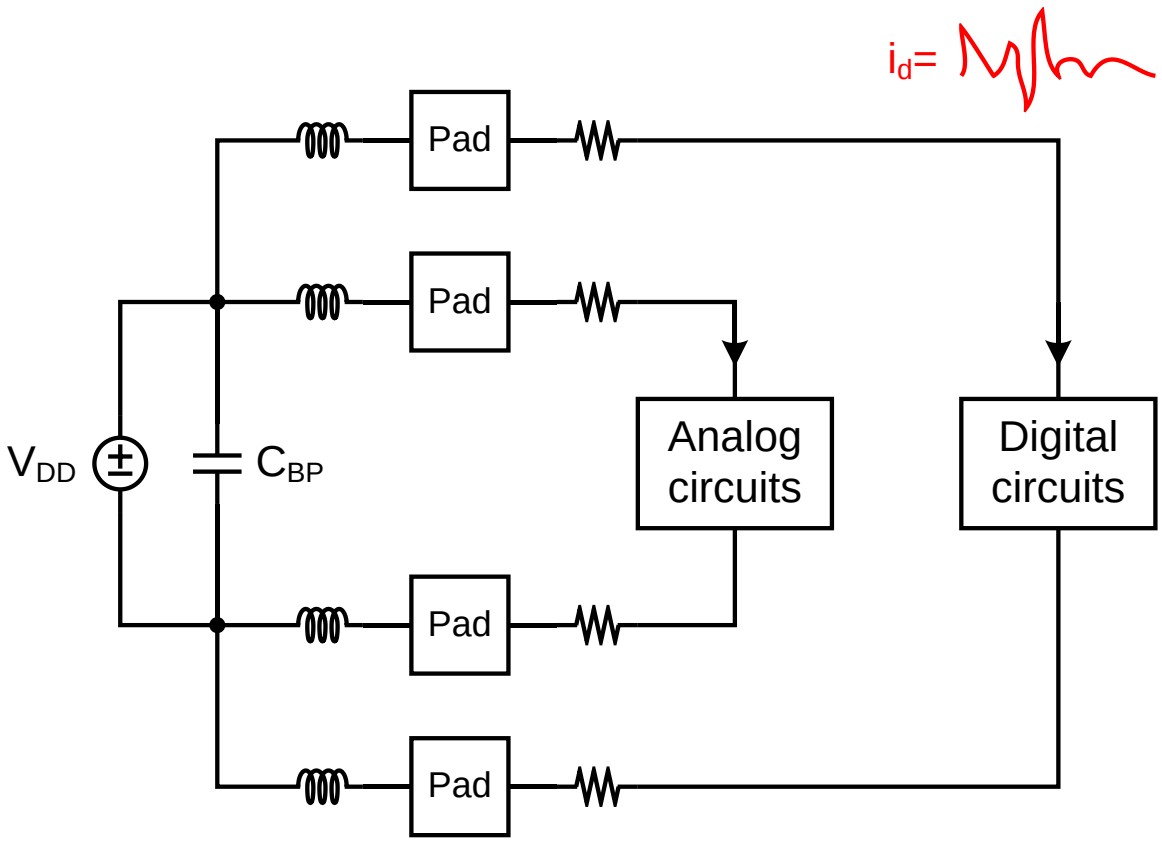
- 6.1 Introduction
- 6.2 Switched-Capacitor Circuit
- 6.3 SC Application
- 6.4 Noise in SC
- 6.5 Non-ideal Effects in SC
- 6.6 Practical Issues

Analog vs. Digital Supply Lines



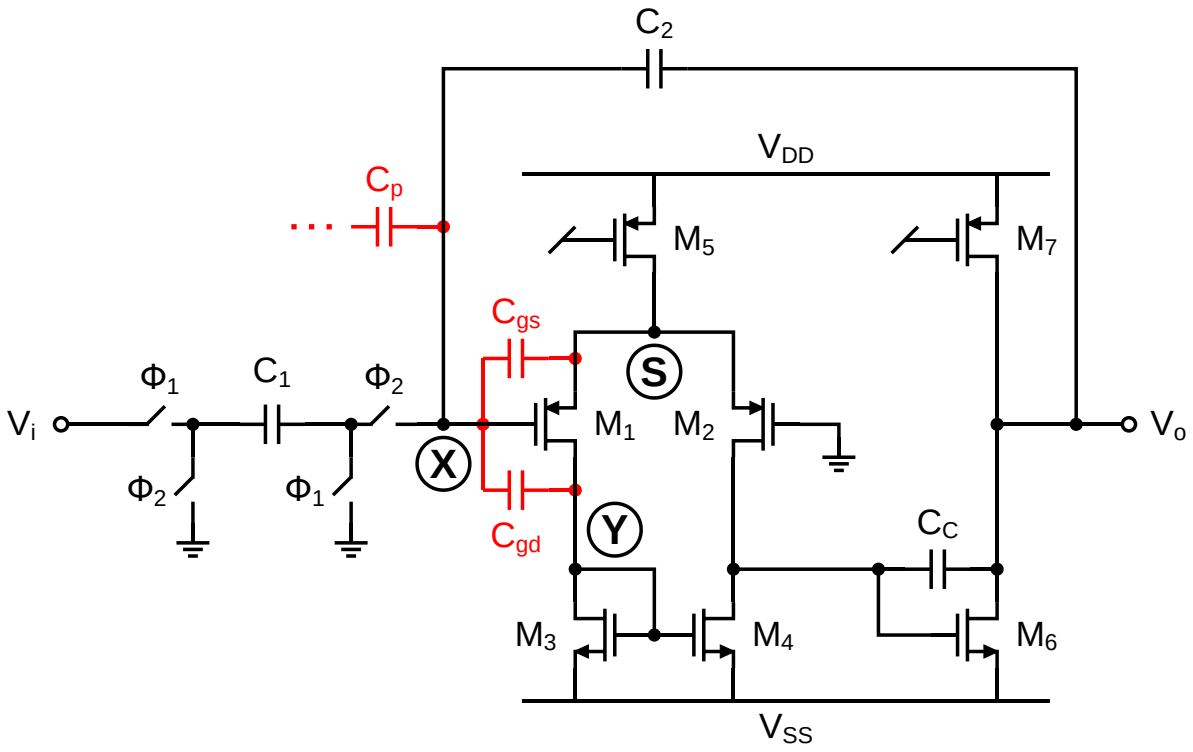
Sharing sensitive analog supplies with digital ones is a very bad idea.

Analog vs. Digital Supply Lines



- Dedicated pads for analog and digital supplies
- On-chip bypass capacitors help (watch ringing)
- Off-chip chokes (large inductors) can stop noise propagation at board level

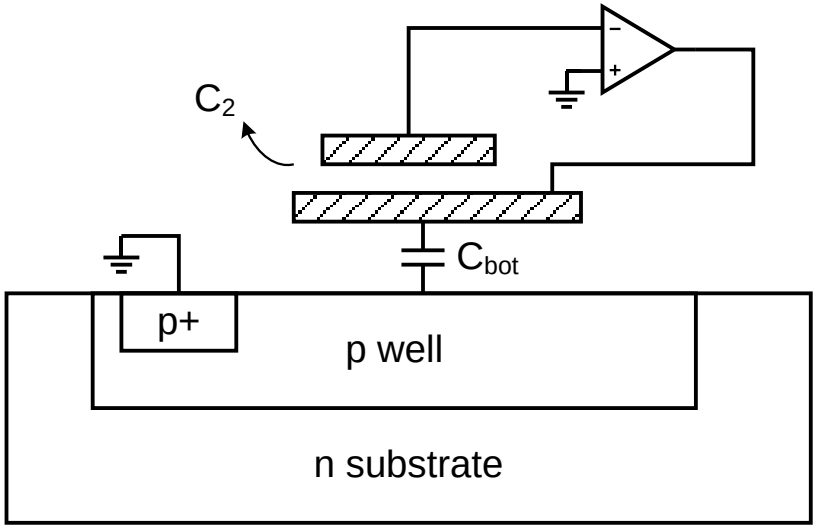
“Supply” Capacitance



$$\Delta V_o = \Delta V \cdot \frac{C_{stray}}{C_2}$$

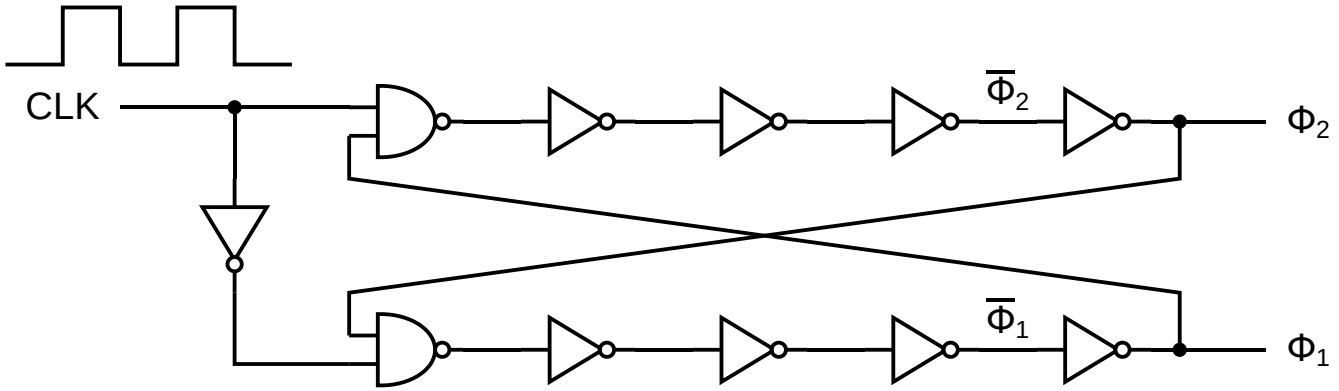
- Any summing-node stray capacitance can be a potential coupling path.
- V_{DD}, V_{SS}, substrate, clock line, and digital noises, body effect, etc.
- Fully differential circuits help to reject common-mode noise and coupling.

“Supply” Capacitance



- Avoid connecting bottom-plate parasitics to the summing node
- Avoid crossing other signal lines with the summing node
- Shielding can mitigate substrate noise coupling

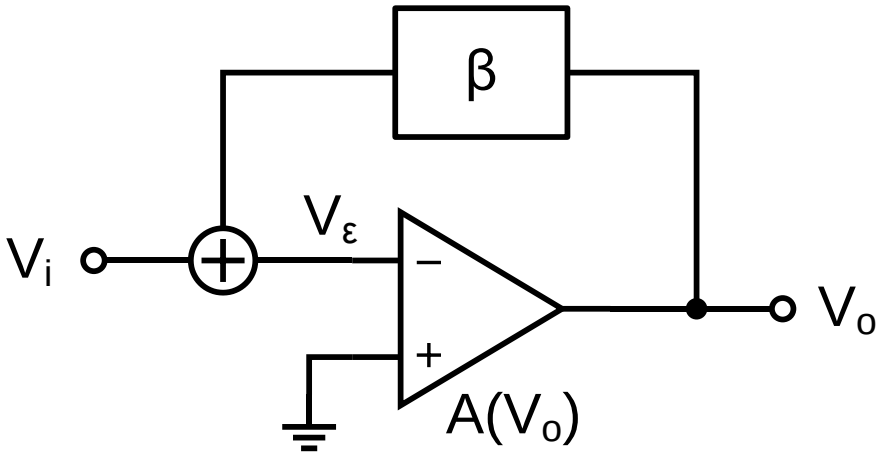
Clock Generation



- Clock-gated ring structure
- Non-overlapping time determined by inverter delays, sensitive to process, voltage, and temperature (PVT) variations
- DLL is an alternative, often used in high-speed designs

Review of CMOS Operational Amplifiers

Negative Feedback



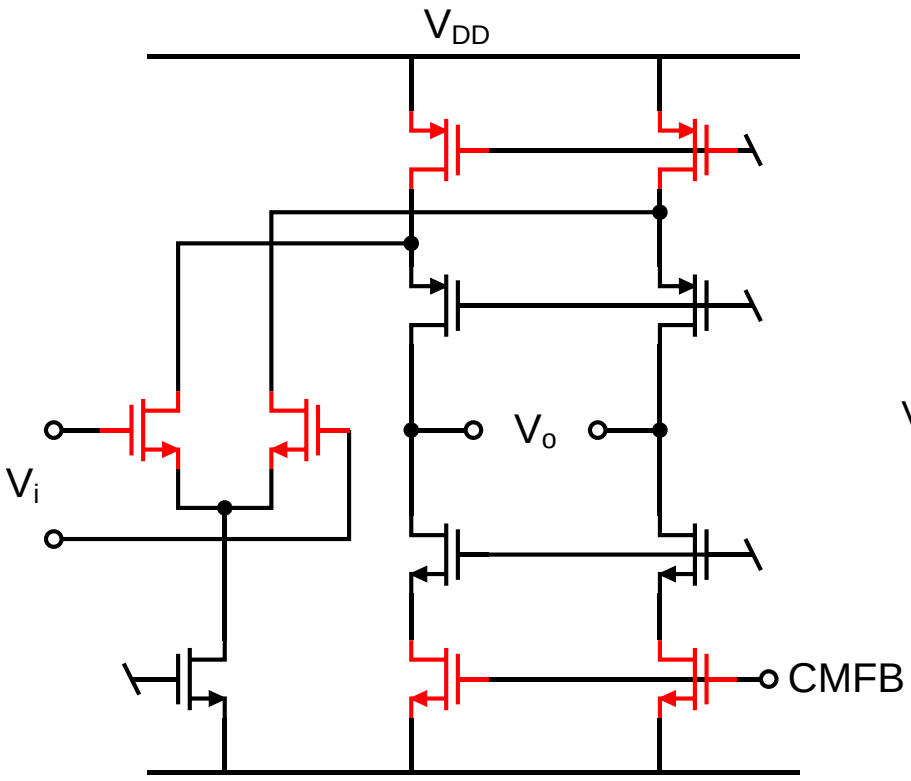
$$\frac{\delta A_{CL}}{A_{CL}} = \frac{\delta A(V_o)}{A(V_o)} \cdot \frac{1}{\beta A(V_o)} = \frac{\delta A(V_o)}{A(V_o)} \cdot \frac{1}{T}$$

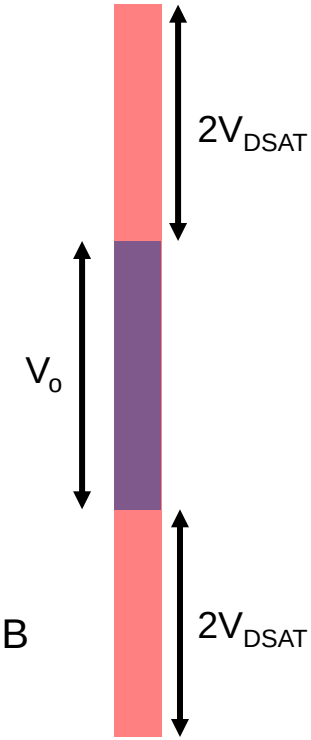
$$THD \sim \frac{1}{\beta A(V_o)} = \frac{1}{T}$$

$$A_{CL} = \frac{V_o}{V_i} = \frac{A(V_o)}{1+\beta A(V_o)} \overset{A(V_o)=\infty}{=} \frac{1}{\beta}$$

- Closed-loop linearity is achieved by negative feedback with large loop gain
- Negative feedback reduces gain sensitivity and harmonic distortion

Folded-Cascode Op-Amp

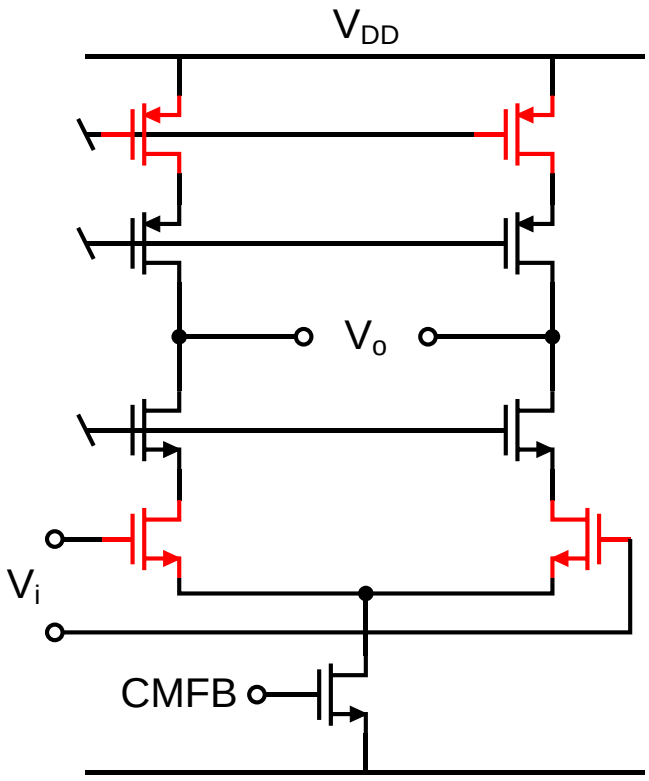


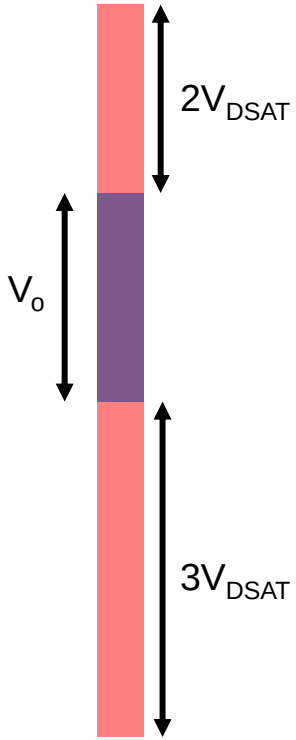


- Differential
- $A_0 \sim (g_m \cdot r_o)^2 \sim$ 40-50dB
- $V_{o,pp} \sim 2(V_{DD}-4V_{DSAT})$
- Noise factor ~ 3
- $\omega_{p2} \sim f_T/3$
- Efficiency ~ 50%
- Load-compensated
- Flexible input CM

Most often used single-stage topology, easy to bias

Telescopic Op-Amp

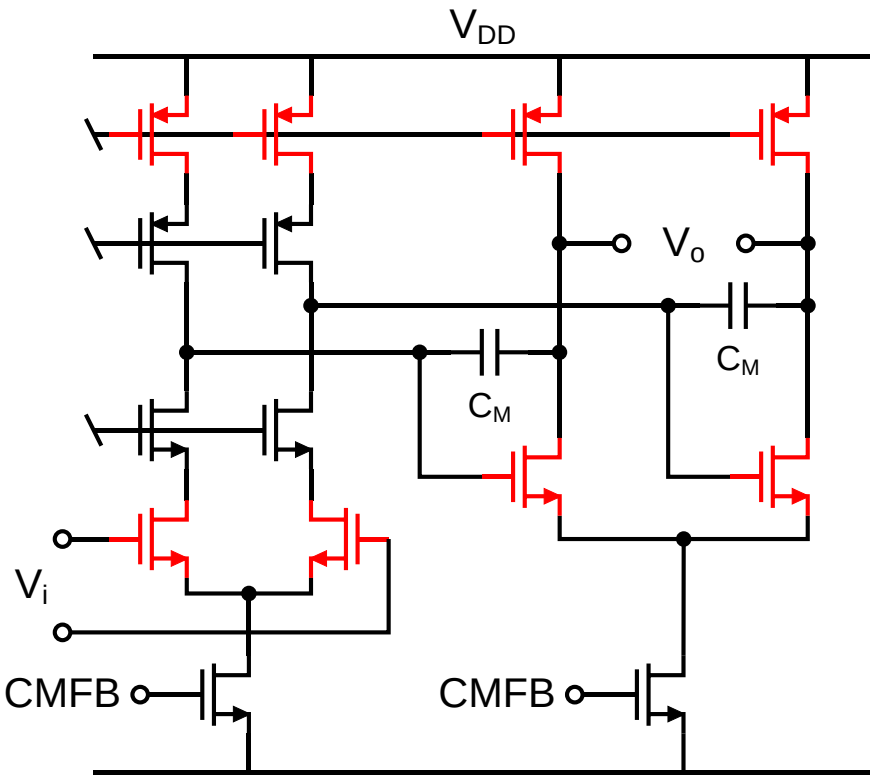


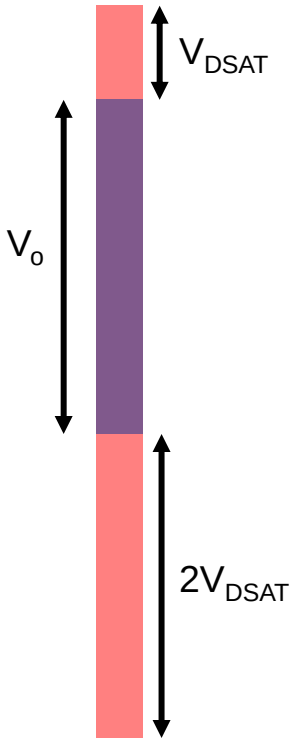


- Differential
- $A_0 \sim (g_m \cdot r_o)^2 \sim$ 40-50dB
- $V_{o,pp} \sim 2(V_{DD}-5V_{DSAT})$
- Noise factor ~ 2
- $\omega_{p2} \sim f_T/2$
- Efficiency ~ 100%
- Load-compensated
- Fixed input CM

2X more power-efficient than the folded-cascode topology, fast

Two-Stage Op-Amp

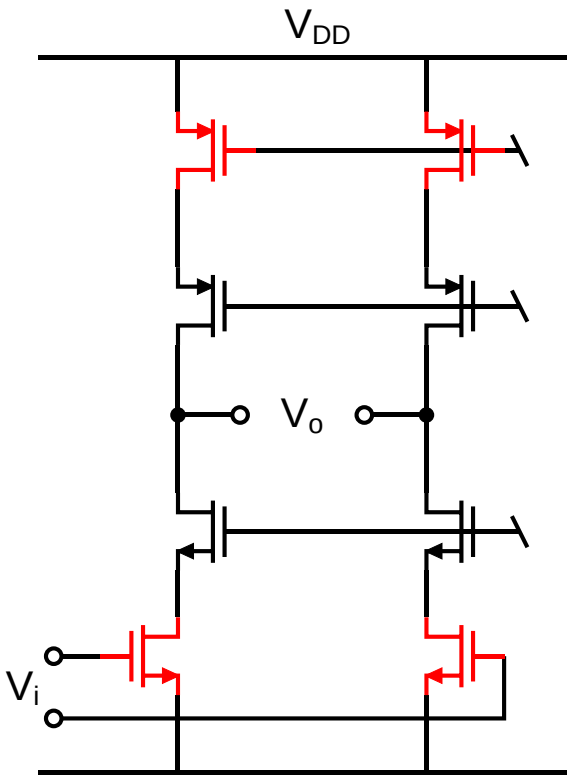


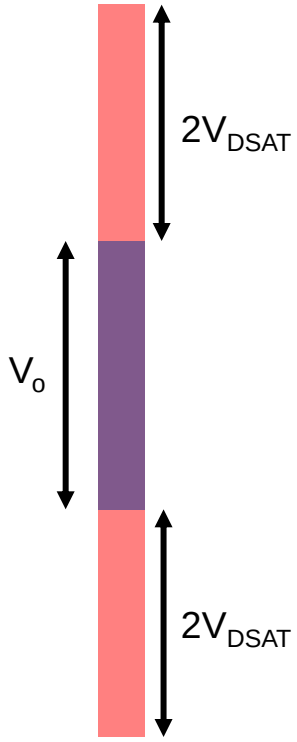


- Differential
- $A_0 \sim (g_m \cdot r_o)^3 \sim$ 60-70dB
- $V_{o,pp} \sim 2(V_{DD}-3V_{DSAT})$
- $N_2 = N_1 \cdot \beta \cdot C_M/C_L$
- Noise factor ~ 2+2β
- $\omega_{p2} \sim g_{m2}/C_L$
- Efficiency < 50%
- Miller-compensated
- Fixed input CM

Not as power-efficient as single stage, suitable for low V_{DD}

Pseudo-Differential Op-Amp

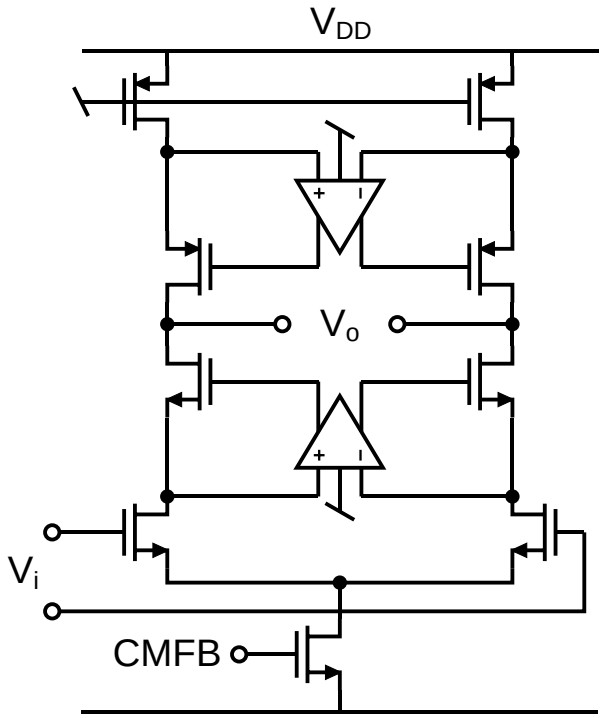


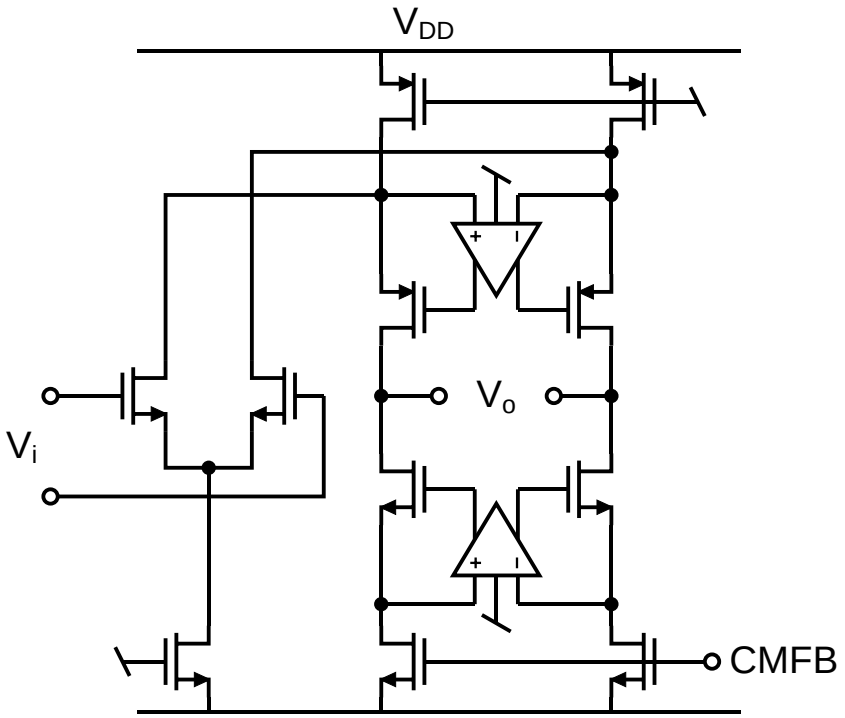


- Differential
- $A_0 \sim (g_m \cdot r_o)^2 \sim$ 40-50dB
- $V_{o,pp} \sim 2(V_{DD}-4V_{DSAT})$
- Noise factor ~ 2
- $\omega_{p2} \sim f_T/2$
- Efficiency ~ 100%
- Load-compensated
- Fixed input CM
- No CMFB point

As power-efficient and fast as telescopic, but V_{ocm} is a problem

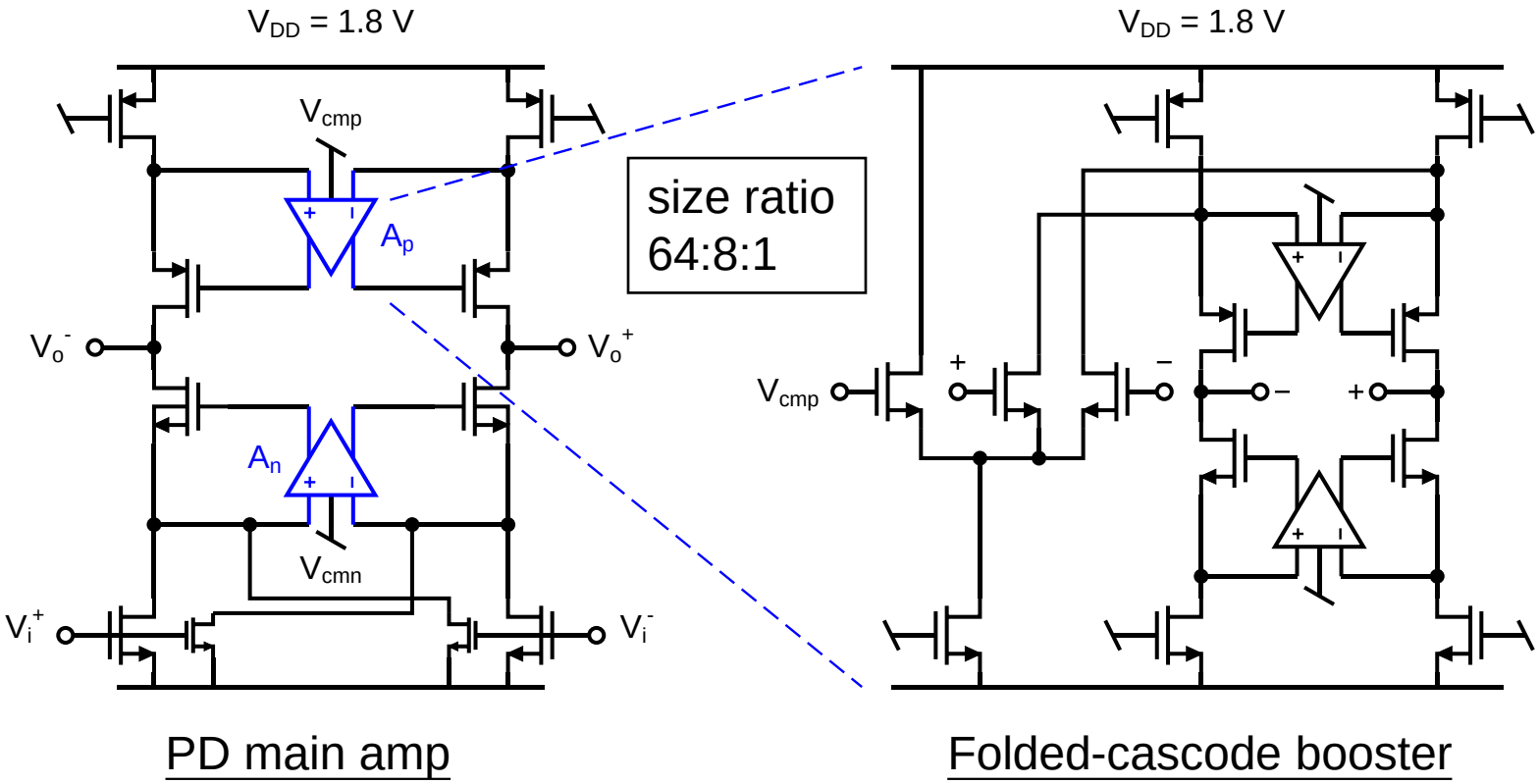
CMOS Gain-Boosting





- $A_0 \sim A_a \cdot (g_m \cdot r_o)^2 \sim$ 60-100dB, limited by substrate current
- Single-stage design, same output swing, suitable for SC circuits
- Auxiliary amplifiers introduce pole-zero doublet (slow settling), additional noise

Nested CMOS Gain-Boosting



- Two levels of recursive gain-boosting → $A_0 \approx (g_m \cdot r_o)^6 \geq 120$ dB
- Pseudo-differential architecture → p-p differential output swing ≥ 2 V

Reference

- Y. Chiu, Data Converters Lecture Slides, UT Dallas 2012.
- Omnivision Product Datasheet
- J. Ohta, Smart CMOS Image Sensor and Applications, 2008