CHAPTER 5

Applications

Outline

- 5.1 Introduction
- 5.2 Information and communication applications
- 5.3 Biotechnology applications
- 5.4 Medical applications

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Introduction

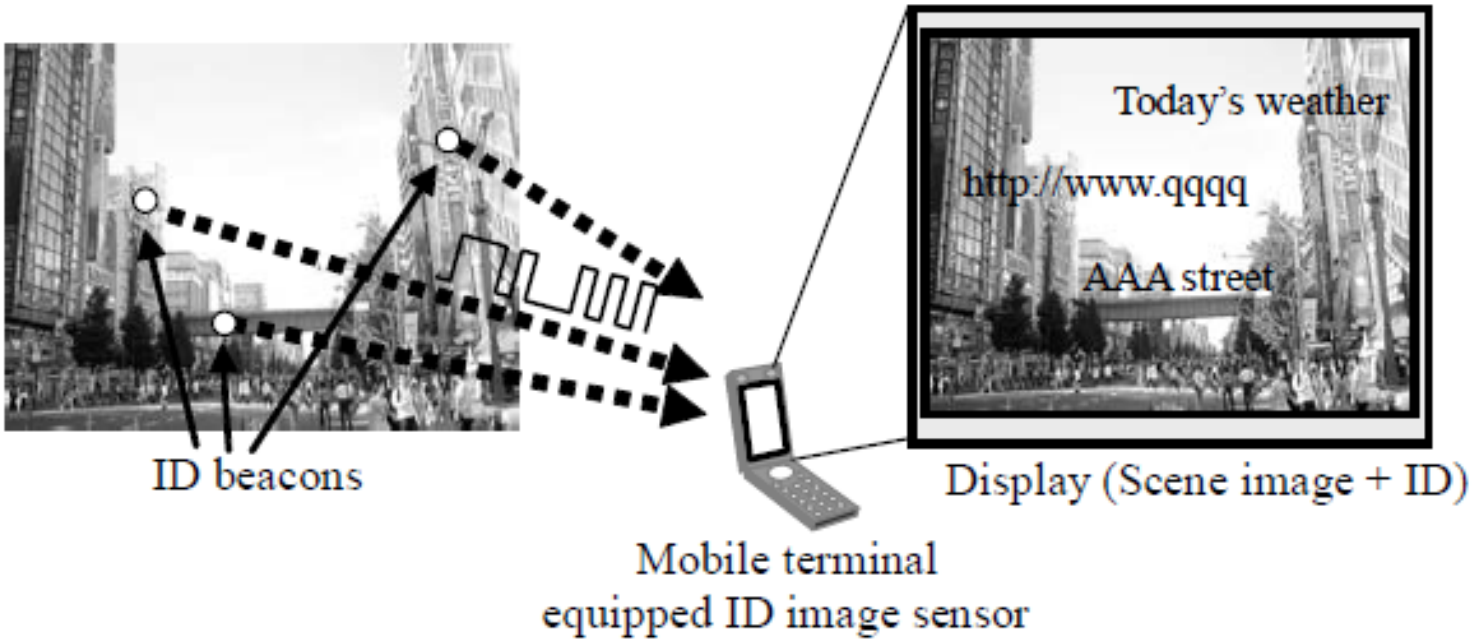
- Information and communication
  - human interfaces
    - communication speed & convenience
- Biotechnology fields
  - improve in performance compare to CCD : compact & highly integration
- Medical
  - require compact imaging systems
    - for swallowing or being implanted

Outline

- 5.1 Introduction
- 5.2 Information and communication applications
  - optical ID tag
  - optical wireless communication
- 5.3 Biotechnology applications
- 5.4 Medical applications

Optical ID tag

- LED displays send their own ID data, the user can easily get information about the contents on the displays.



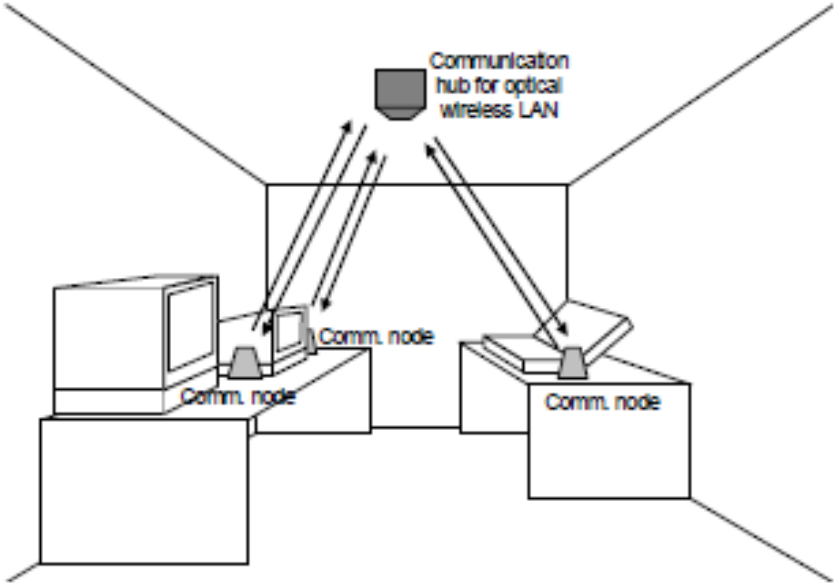
Smart CMOS Sensor for ID tag

Specifications of smart CMOS image sensors for optical ID tags

Affiliation	Sony	Univ. Tokyo	NAIST
Reference	[375]	[427]	[431]
ID detection	High speed readout of all pixels	In-pixel ID receiver	Readout of multiple ROIs
Technology	0.35-μm CMOS	0.35-μm CMOS	0.35-μm CMOS
Pixel size	$11.2 \times 11.2\ \mu m^2$	$26 \times 26\ \mu m^2$	$7.5 \times 7.5\ \mu m^2$
Number of pixels	320×240	128×128	320×240
Frame rate for ID detection	14.2 kfps	80 kfps	1.2 kfps
Power consumption	82 mW (@3.3 kfps, 3.3 V)	682 mW (@4.2 V)	3.6 mW (@ 3.3 V, w/o ADC, TG)
Issues	Power consumption	Large pixel size	Speed

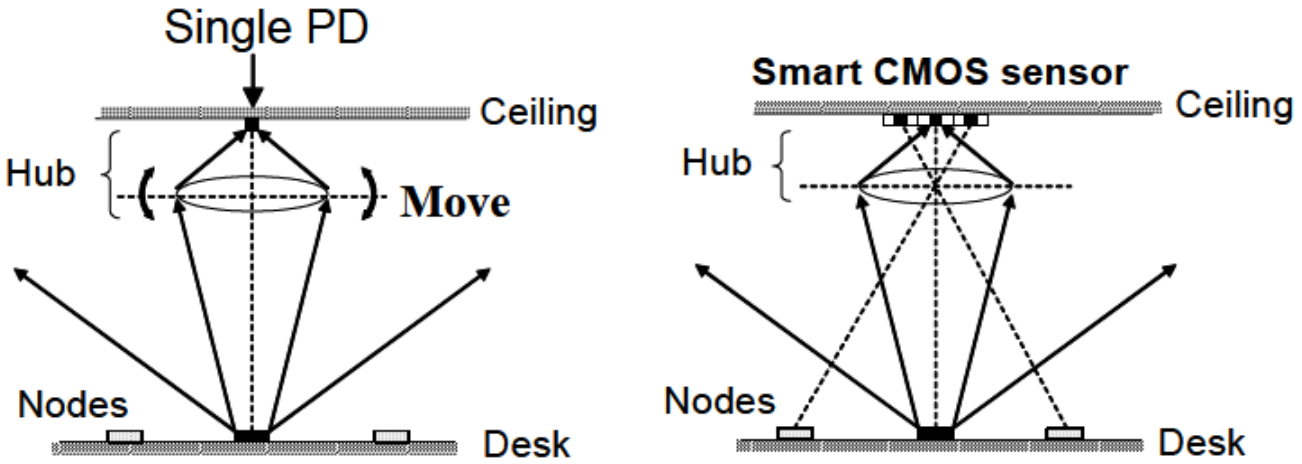
Optical Wireless Communication

- Classified into three categories:
  1. outdoor or long distances over 10 m
     - main application target is for LANs across buildings
     - fast
  2. near-distances (IrDA)
     - not fast
  3. indoor (LAN)
     - consists of a hub and multiple node stations
     - fast (>10 MHz)



CIS for Optical Wireless LANs

- CMOS image sensor is utilized as a photoreceiver as well as a two-dimensional position-sensing device.
- Conventional system:
  - node must be large in order to search for the hub
- Smart CMOS sensor:
  - easy to specify the positions



(a) convention (b) smart CMOS image sensor

Dual Mode Operation

- Image sensor (IS) mode
  - search for the node
- Communication (COM) mode
  - emit a collimated beam carrying the data toward the node

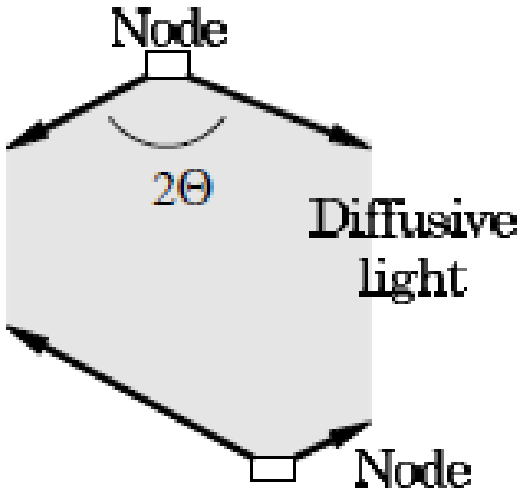
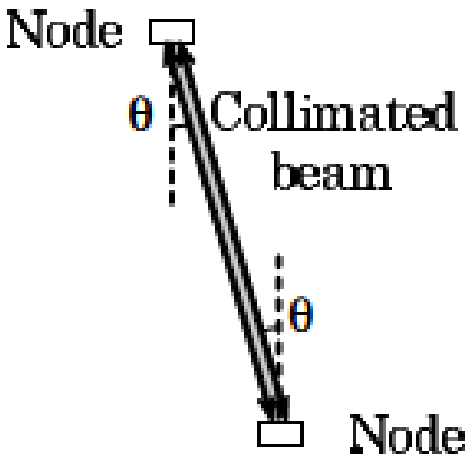


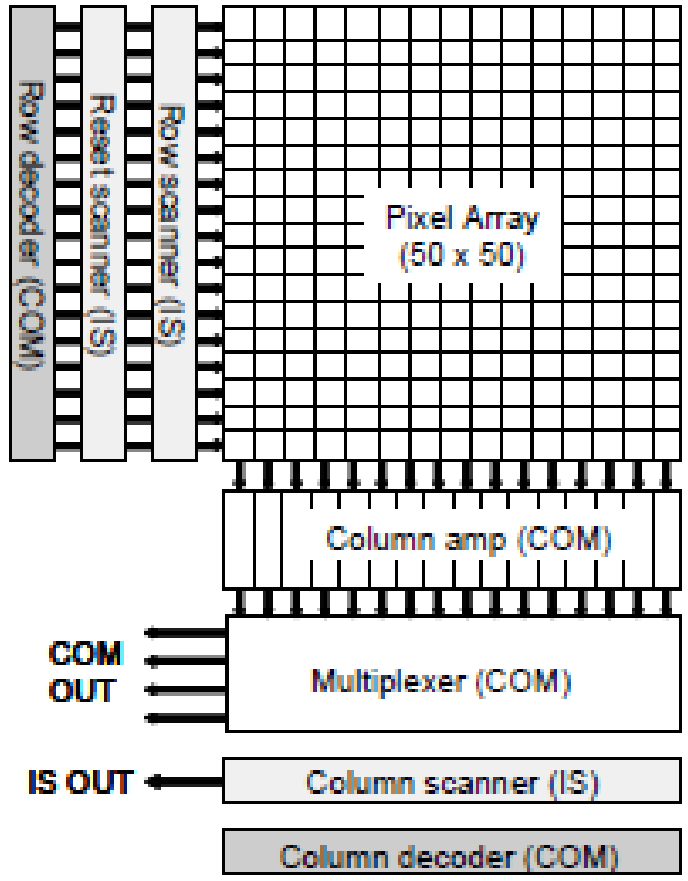
Image sensor mode



Communication mode

Implementation

- Consists of 3T-APS, a transimpedance amp, digital circuits for mode switching, and a latch memory
- One IS mode output
- Four COM mode output



Outline

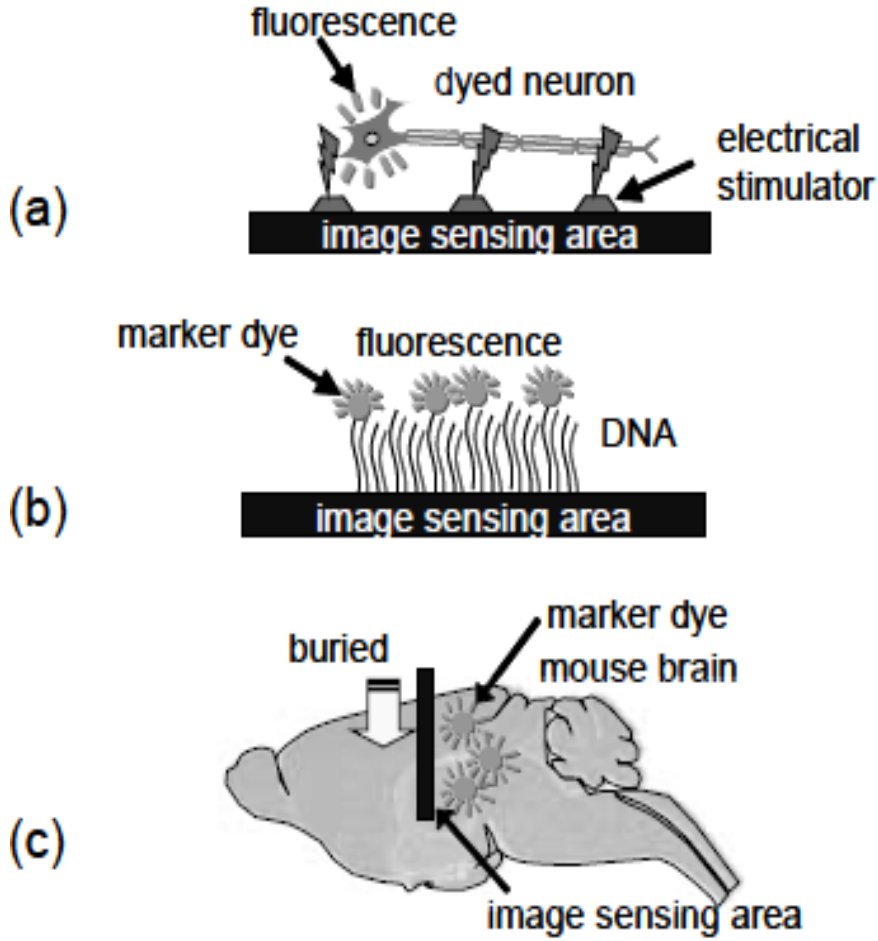
- 5.1 Introduction
- 5.2 Information and communication applications
- 5.3 Biotechnology applications
  - fluorescence detection
- 5.4 Medical applications

Fluorescence Detection

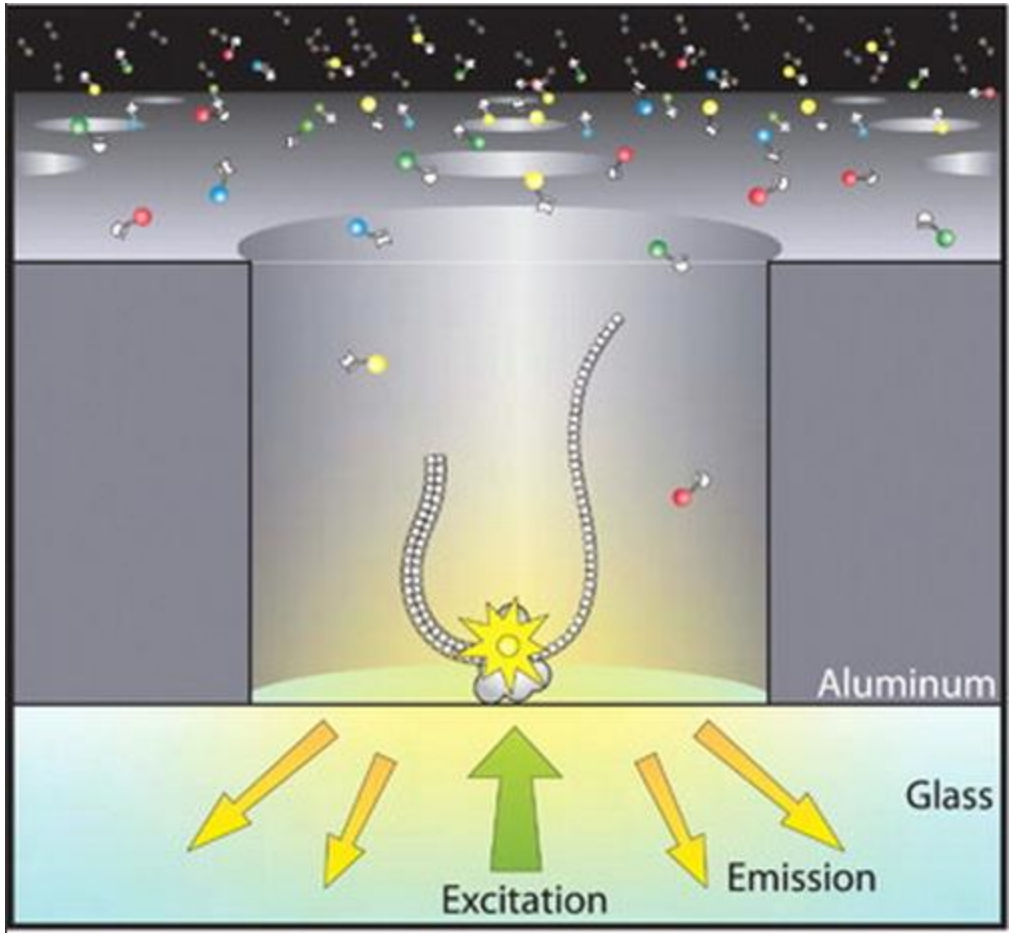
- Fluorescence detection is a widely used measurement in biotechnology.
- Conventionally performed by a CCD camera.
- Introducing smart CMOS image sensor would bring the benefits of integrated functions and miniaturization.

Fluorescence Detection

- The sensor can stimulate neurons and detect the fluorescence.
- The DNA with fluorescence dyes hybridize with complementary strands on the sensor surface.
- In a mouse brain, sensor can detect fluorescence as well as stimulate neurons around it.



DNA Sequencing



Outline

- 5.1 Introduction
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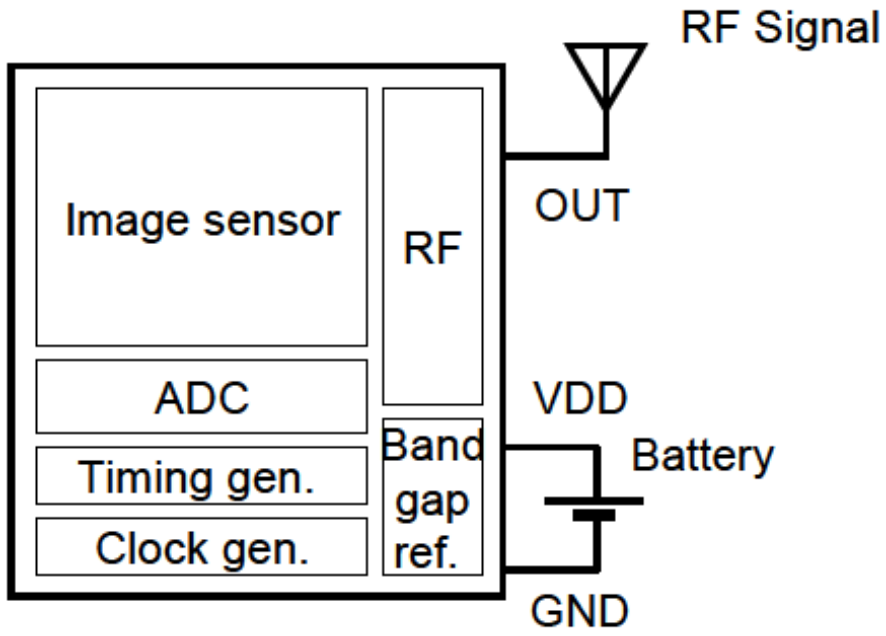
- 5.3 Biotechnology applications
- 5.4 Medical applications
  - capsule endoscope
  - retinal prosthesis

Capsule Endoscope

- An endoscope is employed with a CCD camera, light guide, small forceps, a tube for injecting water to clean tissues, and an air tube for enlarging affected regions.
- Smart CMOS image sensor for capsule endoscope
  - small volume
  - low power consumption
  - system-on-chip (SoC)



Capsule Endoscope

- Another desirable function for capsule endoscope:
  - on-chip image compression
  - electro-mechanical systems (MEMS)
  - micro total analysis system (μTAS)
  - lab-on-chip (LOB)
  - monitor other physical values such as potential, pH, and temperature

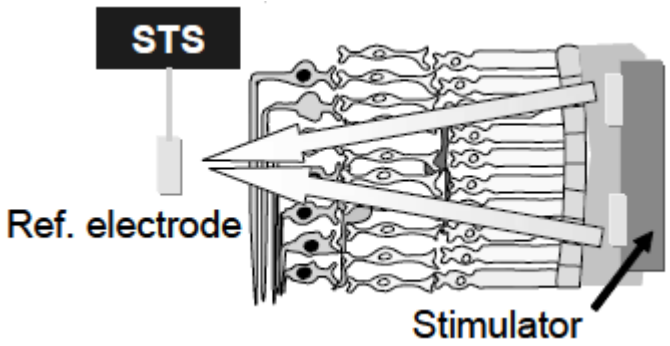
Length: 26 mm; Diameter: 11 mm

Retinal Prosthesis

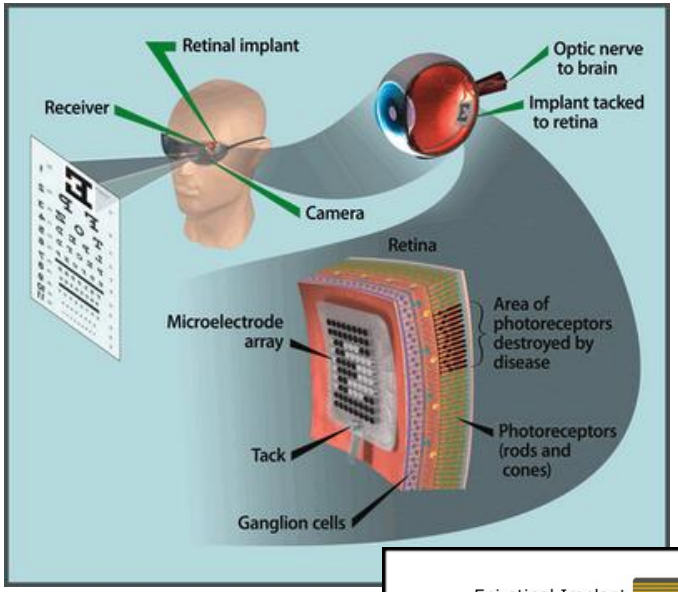
- Optacon, or optical-to-tactile converter, is the first use of a solid-state image sensor for the blind.
- Retinal prosthesis is an implantable version of Optacon.
- The blind perceive an object through:
  - Optacon: tactile sense
  - Retinal prosthesis: electrical stimulation of vision-related cells by an implanted device

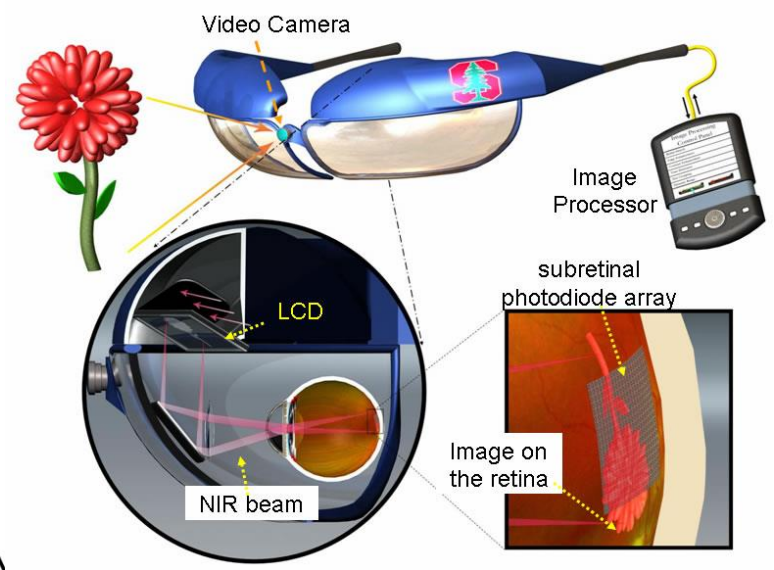
Retinal Prosthesis

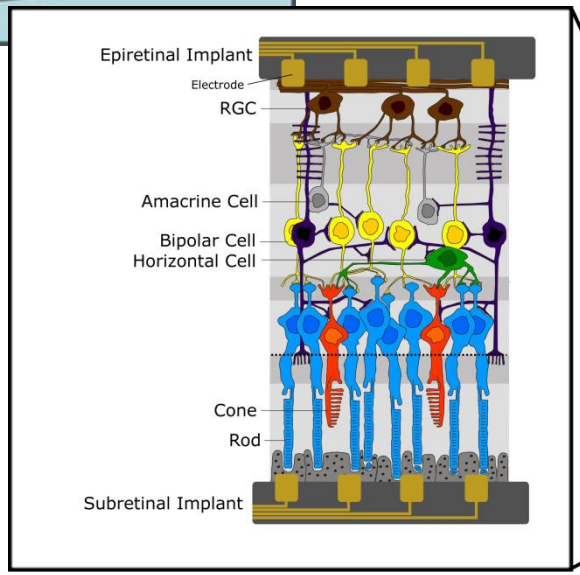
- Different implantation sites:
  - cortical region
  - optic nerve
  - epi-retinal space
  - sub-retinal space
- Recently another approach called suprachoroidal transretinal stimulation (STS) has been developed.

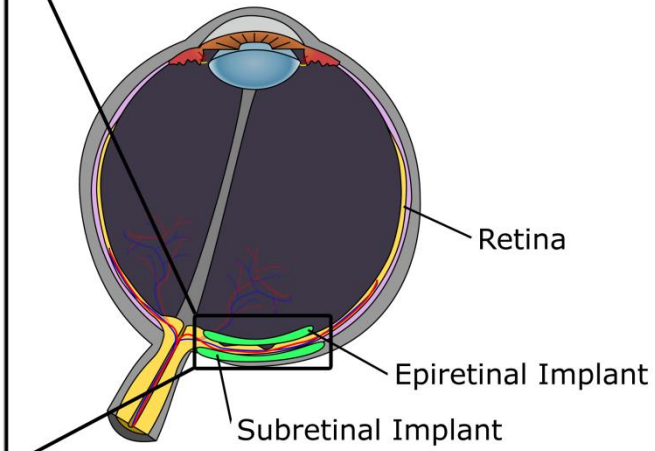


Retinal Prosthesis



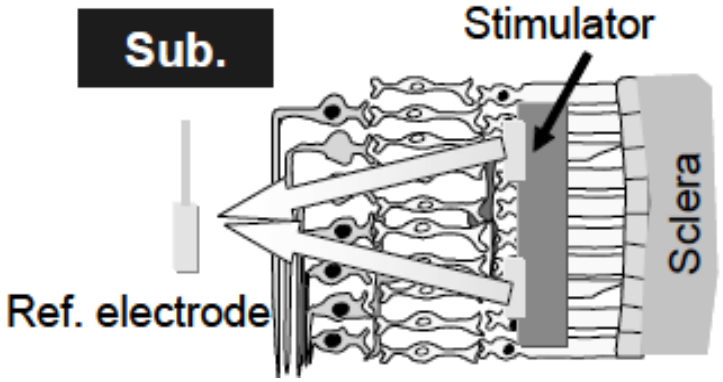






Sub-Retinal Approach

- A photosensor is required in order to integrate the stimulus electrode.
  - a simple photodiode array (solar cell mode)
- The photocurrent is directly used as the stimulus current into the retinal cells.
- Sub-retinal approach is natural because imaging can be done on the same plane of stimulation.

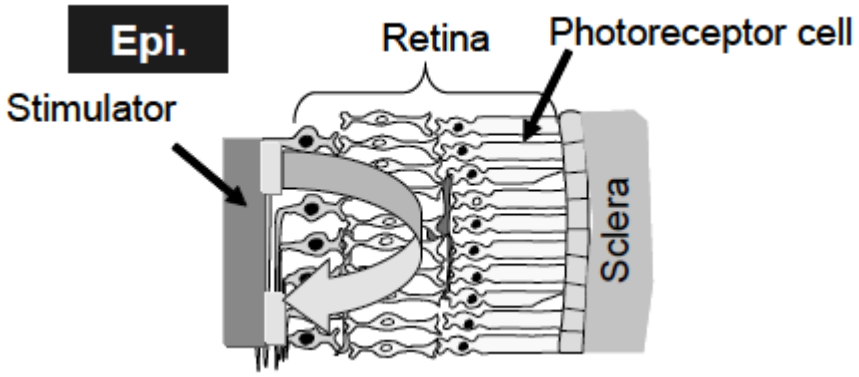


Sub-Retinal with PFM Sensor

- Why PFM?
  - In order to generate sufficient stimulus current
  - pulse streams is effective for stimulating cells
  - pulse form is compatible with logic circuits
    - enable highly versatile functions
  - Can operate at low voltage without decreasing SNR
  - high photosensitivity and dynamic range

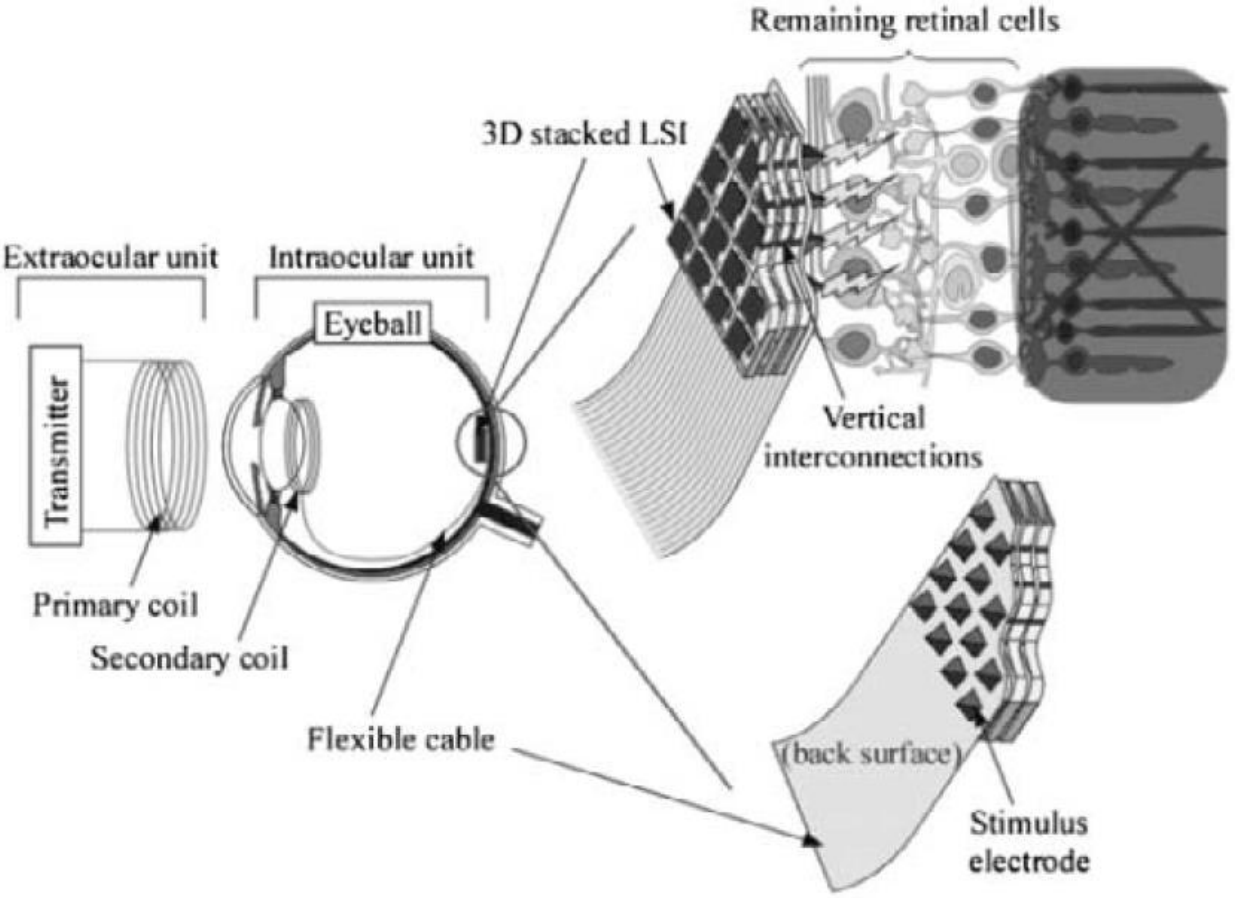
Epi-Retinal Approach

- Silicon-on-sapphire with back-illuminated image sensor has been demonstrated for the epi-retinal approach.
  - SOI is transparent
  - image area and stimulation can be placed on the same plane by using back-illuminated

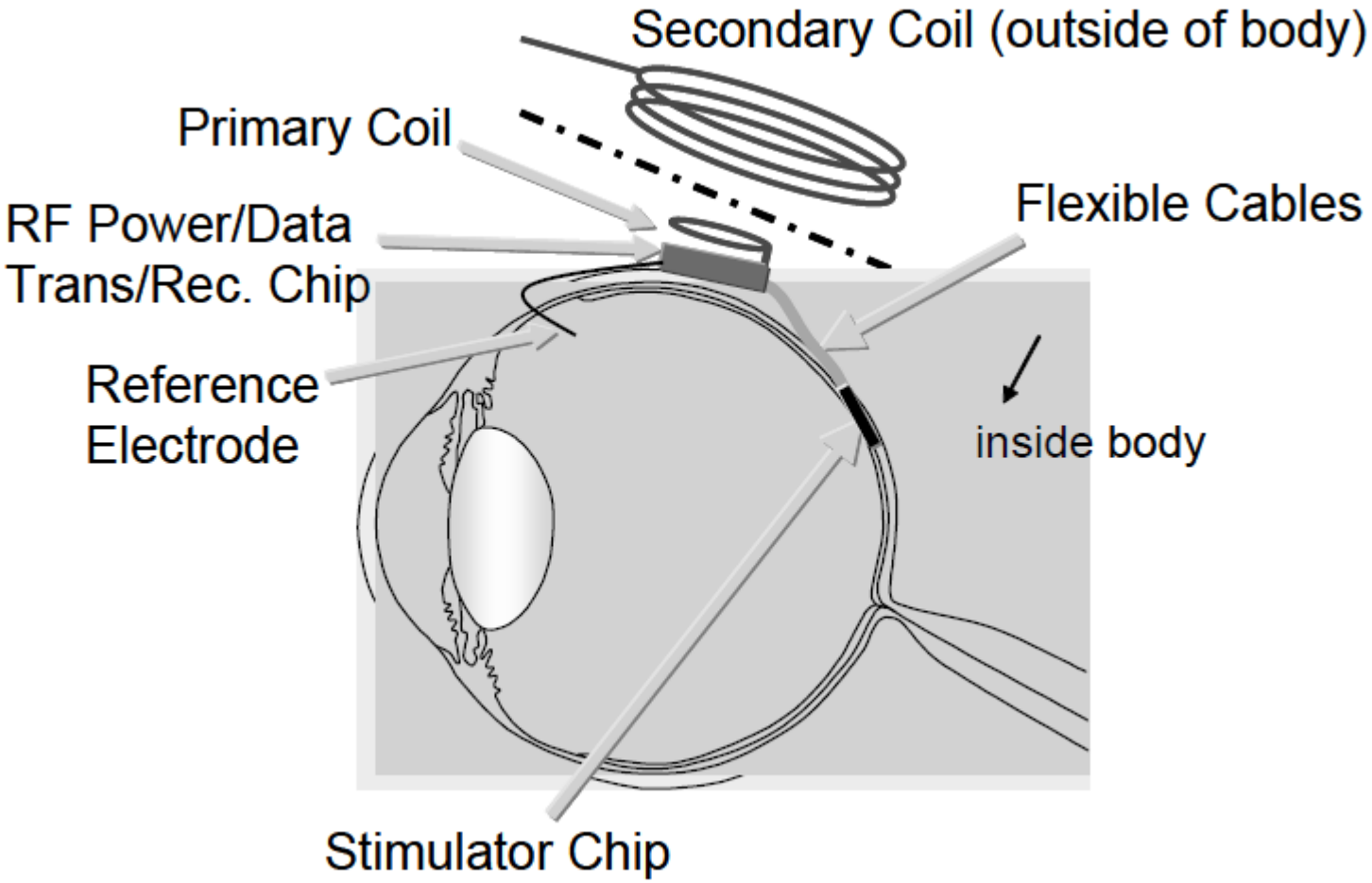


3D integration

- Another epi-retinal approach
  - 3D integration



Ocular Implantation



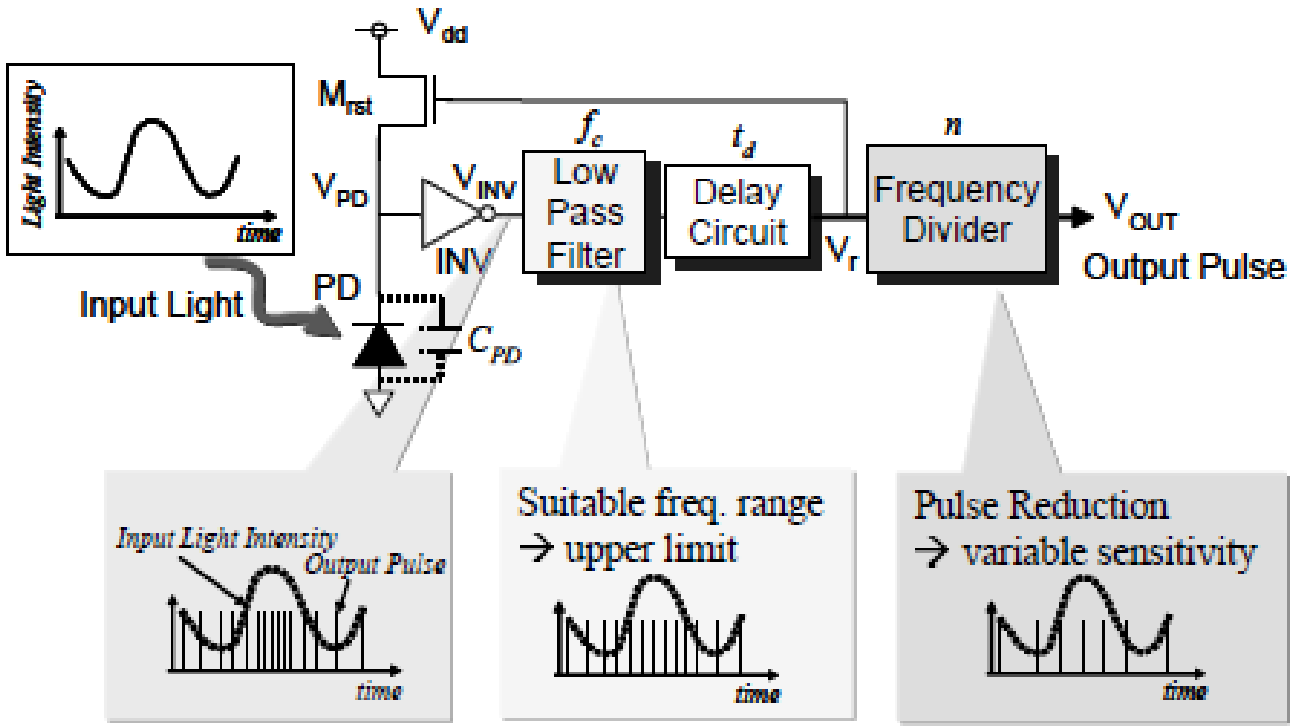
Need to Overcome - 1

- LSI for ocular implantation
  1. Bio-compatibility
     - The standard LSI structure will be damaged in a biological environment for long-time implantation
  2. Fabrication compatible with standard LSI
     - Wire-bonding pads, which are made of aluminum, would dissolve in a biological environment
  3. Shape of stimulus electrode
     - A convex shape is suitable for efficient stimulation, but the electrodes in LSI are flat

Need to Overcome - 2

- Modification of PFM for retinal cell stimulation
  1. Current pulse
     - The output of a PFM is a voltage pulse, whereas a current output is preferable for retinal cell
  2. Biphasic pulse
     - biphasic output for charge balance, because residue charges accumulate in living tissues may cause harmful effects to retinal cells.
  3. Frequency limit
     - high frequency may cause damage to retinal cells

Modified PFM Photosensor

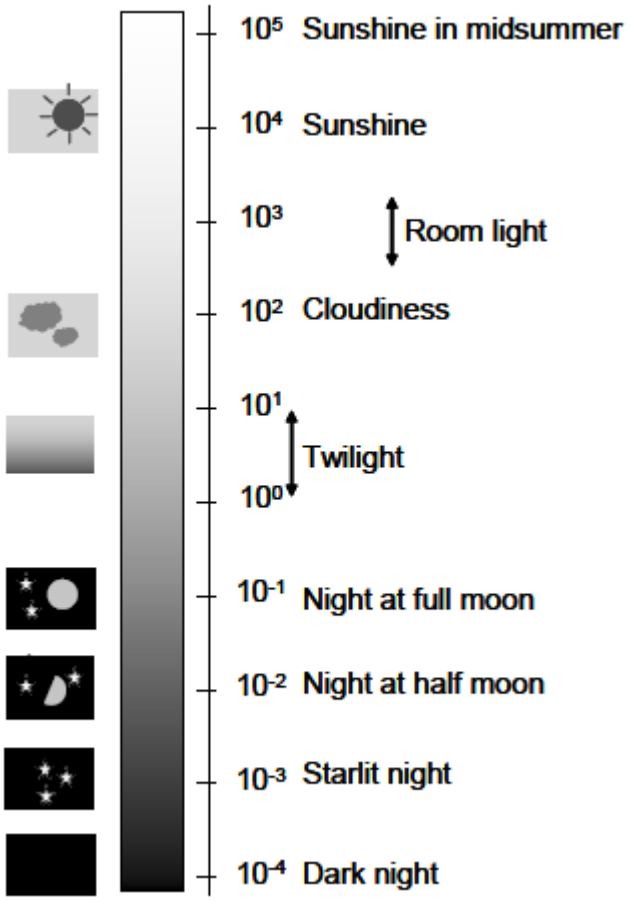


- Frequency limitation is achieved by low pass filter
- A biphasic current pulse is implemented by switching the current source and sink alternatively

Appendix

Illumination

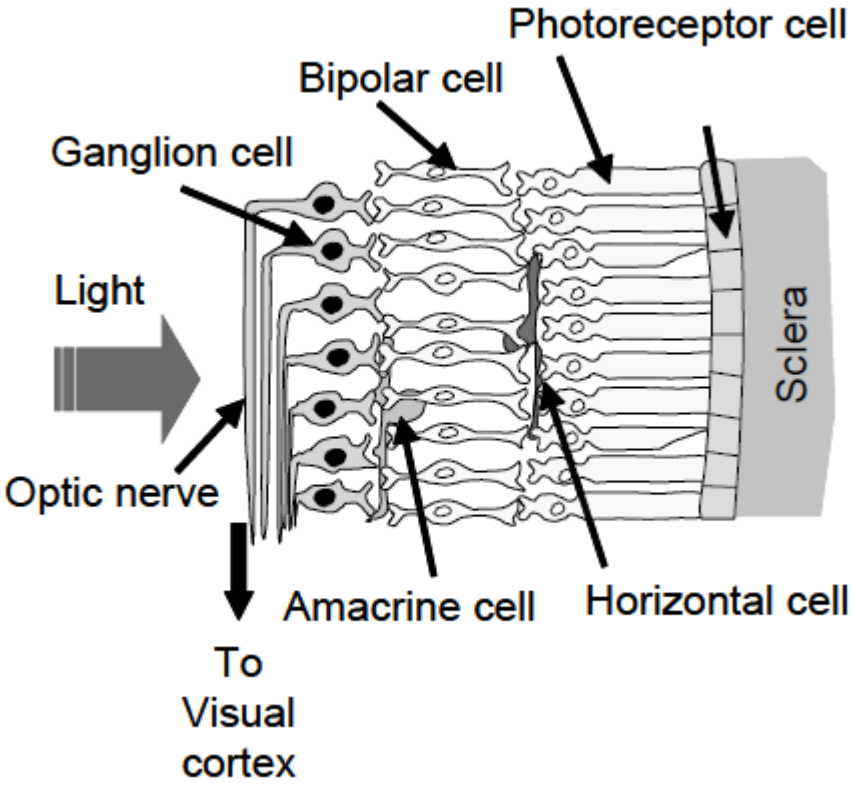
- Illumination
  - It is defined as the light power per unit area.
- Illumination unit : lux
  - A photometric unit related to human eye characteristics.
  - it is not a pure physical unit.



Typical levels of illuminance for a variety of lightning conditions

Human eye & CMOS image sensor

- Human eyes are an ideal imaging system and a model for CMOS imaging systems.
- Dynamic range : 200 dB with multi-resolution.
- Two eyes, which allows range finding by convergence and disparity.
- Area : 5 cm x 5 cm.
- Thickness : 0.4 mm.



Human eye & CMOS image sensor

Item	Retina	CMOS sensor
Resolution	Cones: 5×10^6 Rods: 10^8 Ganglion cells: 10^6	$1–10 \times 10^6$
Size	Rod: diameter 1 μm near fovea Cone: diameter 1–4 μm in fovea, 4–10 μm in extrafovea	2–10 μm sq.
Color	3 Cones (L, M, S) (L+M): S = 14:1	On-chip RGB filter R:G:B=1:2:1
Min. detectable illumination	~0.001 lux	0.1–1 lux
Dynamic range	Over 140 dB (adaptive)	60–70 dB
Detection method	Cis–trans isomerization →two-stage amplification (500 × 500)	e–h pair generation Charge accumulation
Response time	~10 msec	Frame rate (video rate: 33 m-sec)
Output	Pulse frequency modulation	Analog voltage or digital
Number of outputs	Number of GCs: ~1M	One analog output or bit-number in digital output
Functions	Photoelectronic conversion Adaptive function Spatio-temporal signal processing	Photoelectronic conversion Amplification Scanning

Recent Works

Recent Research Works

- Low-Voltage CIS Ref.[8] ISSCC2012
  - 0.5V PWM CIS with threshold-variation-cancelling
- High-Dynamic Range CIS Ref.[9] TED2012
  - Dual-exposure with illumination detection
- High-Speed CIS Ref.[10] JSSC2013
  - 100fps 3Mega CIS for 3D-stacking module
- CIS for Artificial Retina Ref.[11] TED2013
  - 64x64 CIS with sense-and-stimulus pixel
- CIS for Motion Detection ISSCC 2020
- CIS for Face Detection (embedded CNN) ISSCC 2022

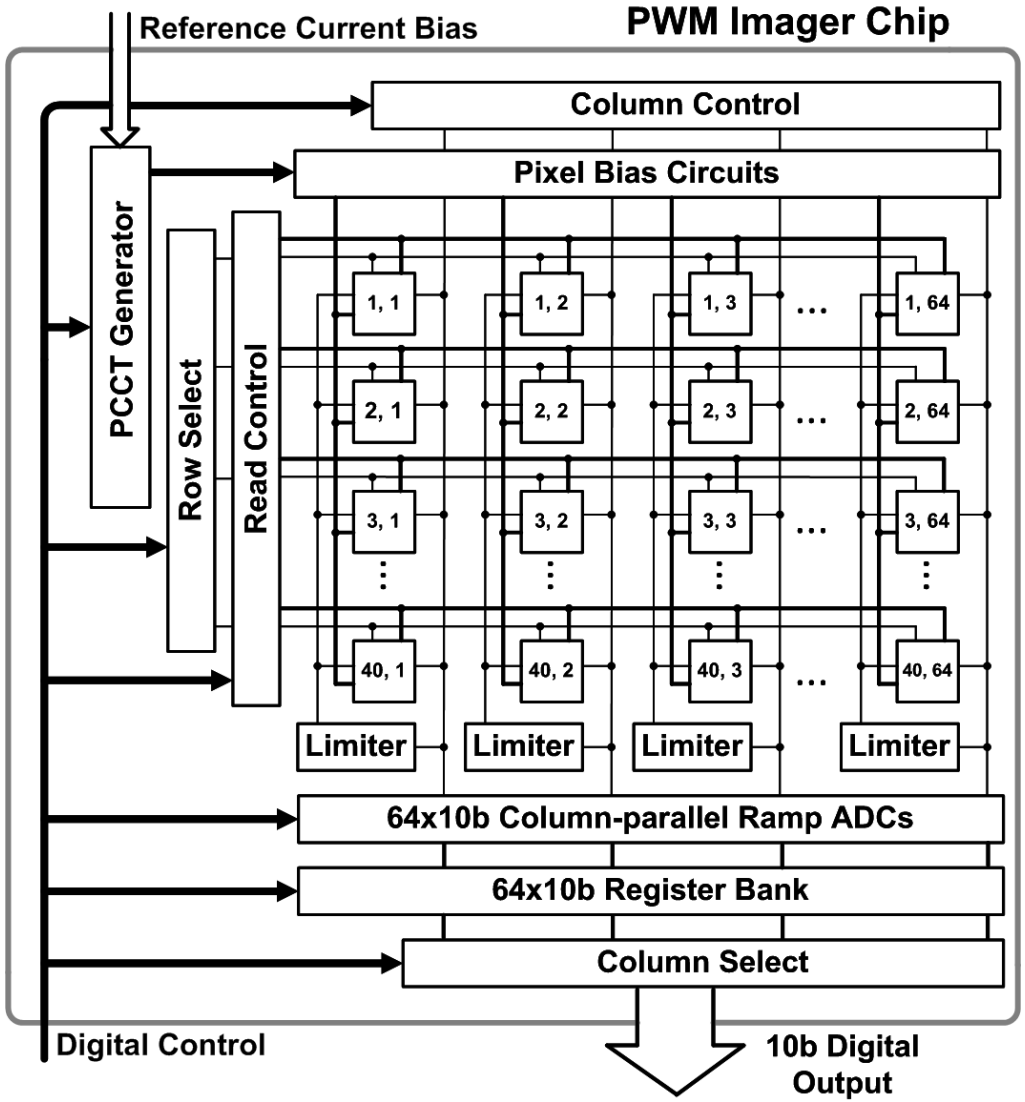
W1: Low Voltage CIS

- Motivation
  - To develop an ultra-low power image sensor with high dynamic range.
- Key Features
  - Low power & Low supply voltage
    - Lifetime & Safety
  - Low noise & High dynamic range
    - High accuracy & Operating in high contrast environment
  - Highly integrated
    - Small size & Low cost

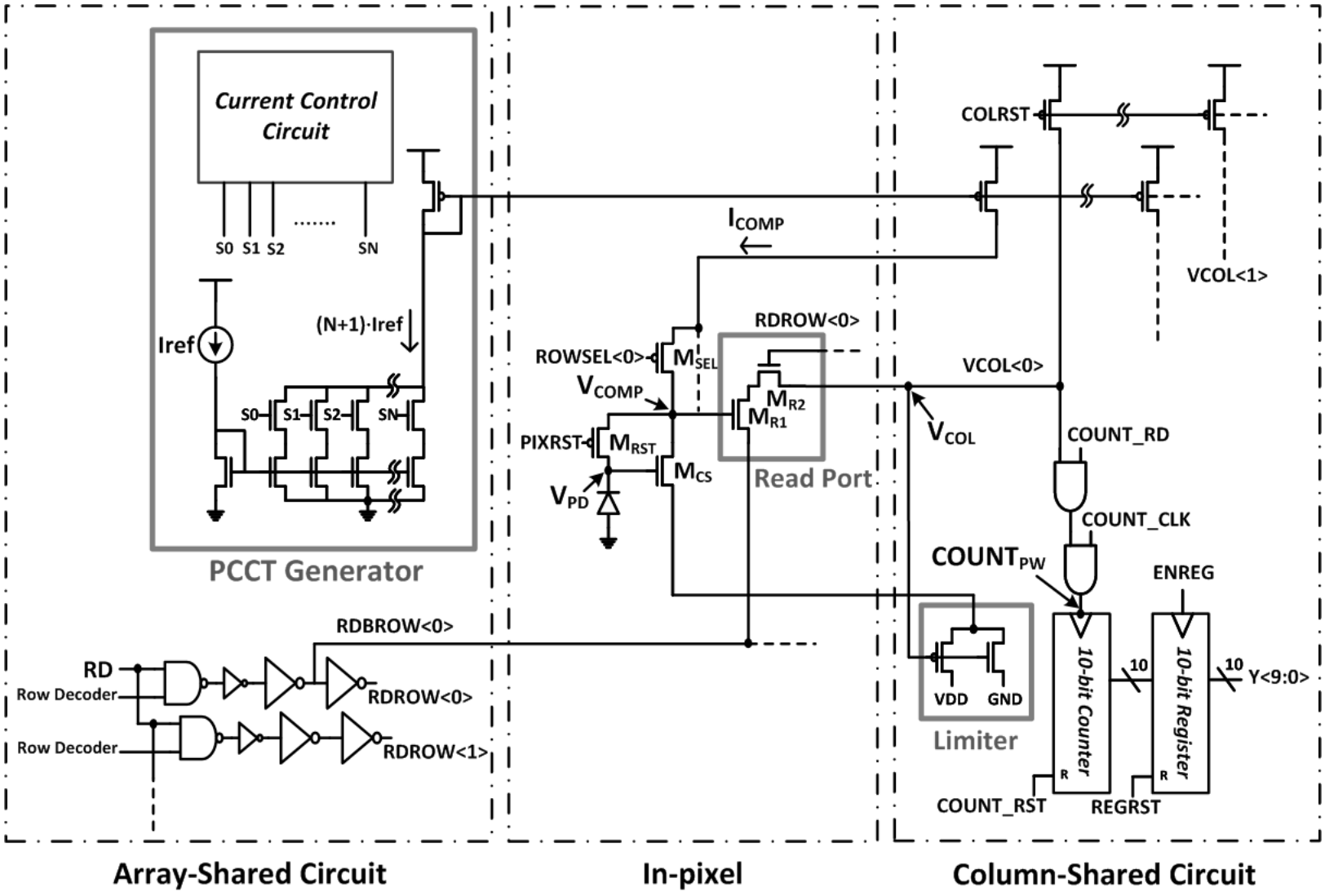
Problem & Solution

- Low-voltage operation
  - Pulse width modulation (PWM) image sensor
- Subthreshold operation
  - Dynamic range extension
  - Programmable current-controlled threshold (PCCT) scheme
- Comparator variation
  - Threshold-variation-canceling (TVC) scheme

Architect of PWM Imager

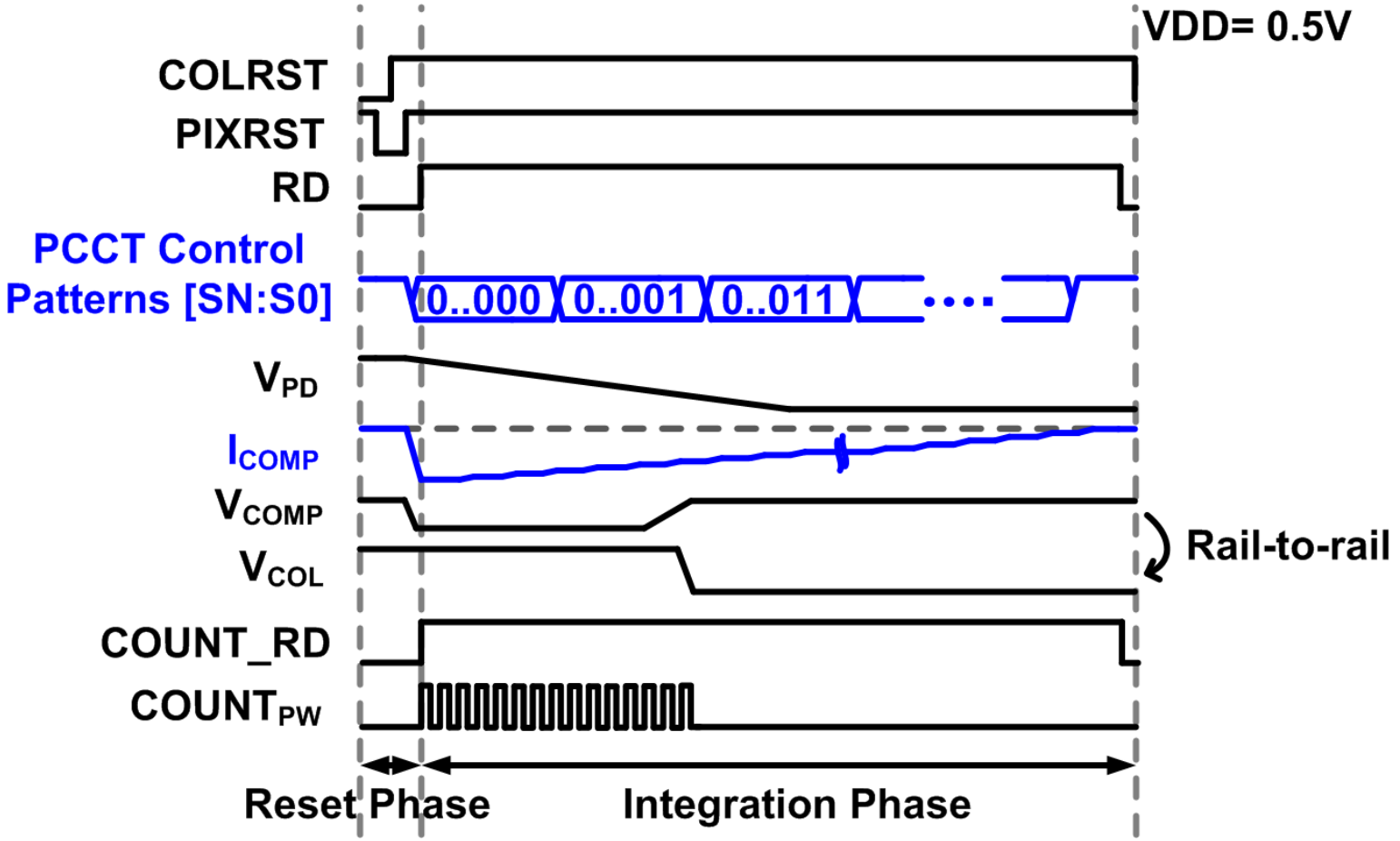


Proposed PWM Imager



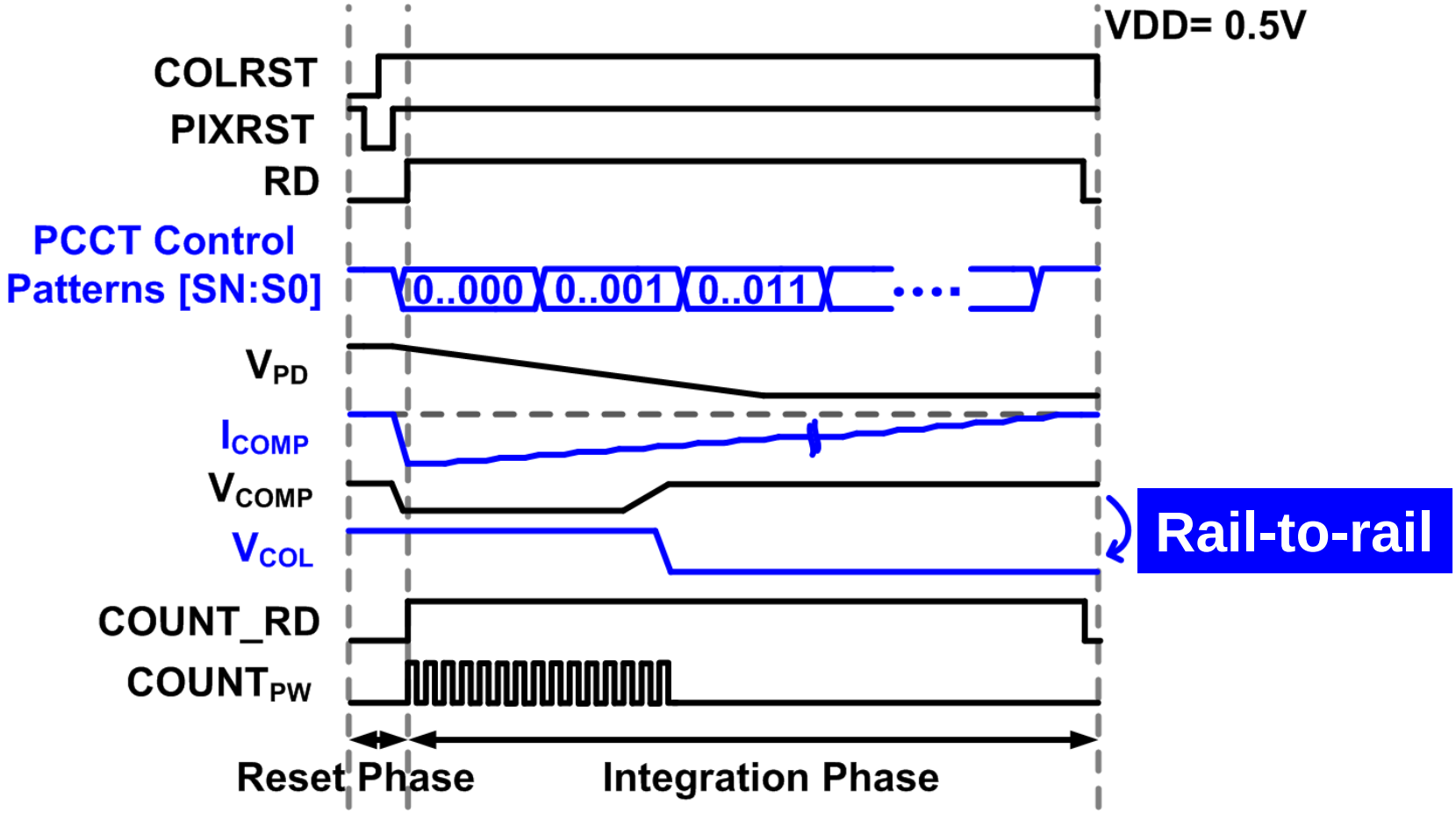
PCCT Scheme

- Timing diagram for one row



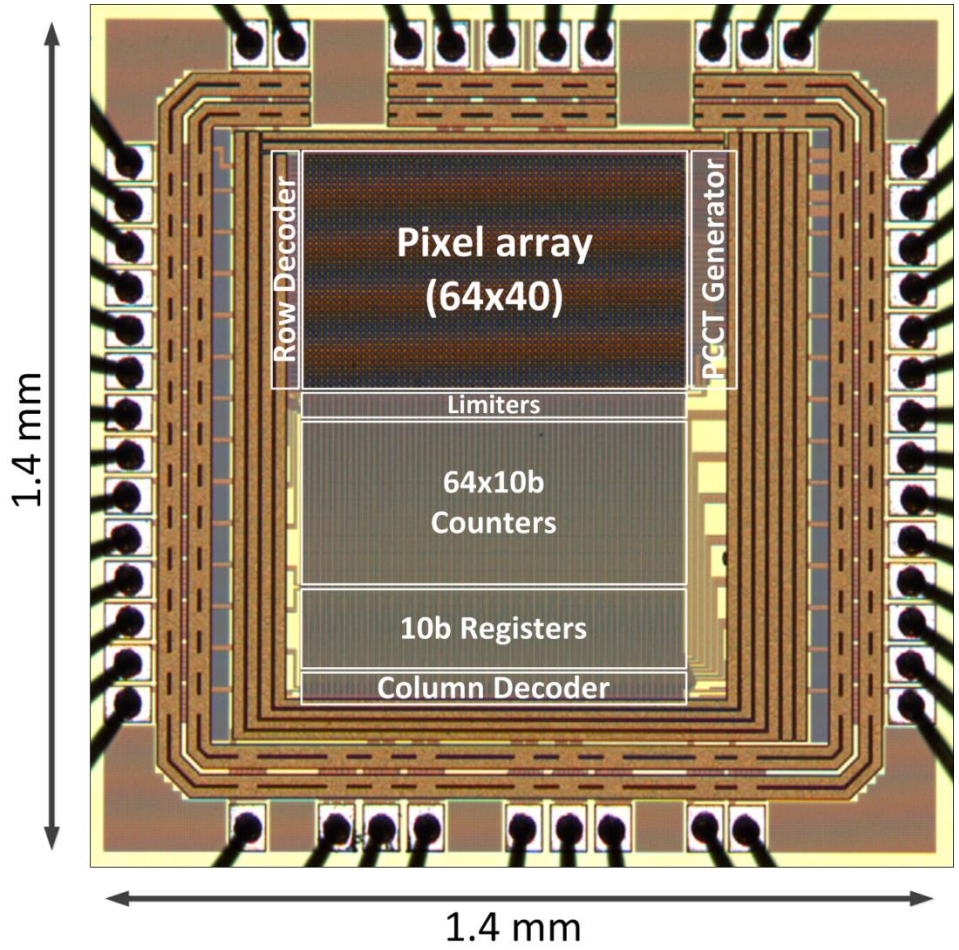
PCCT Scheme

- Timing diagram for one row

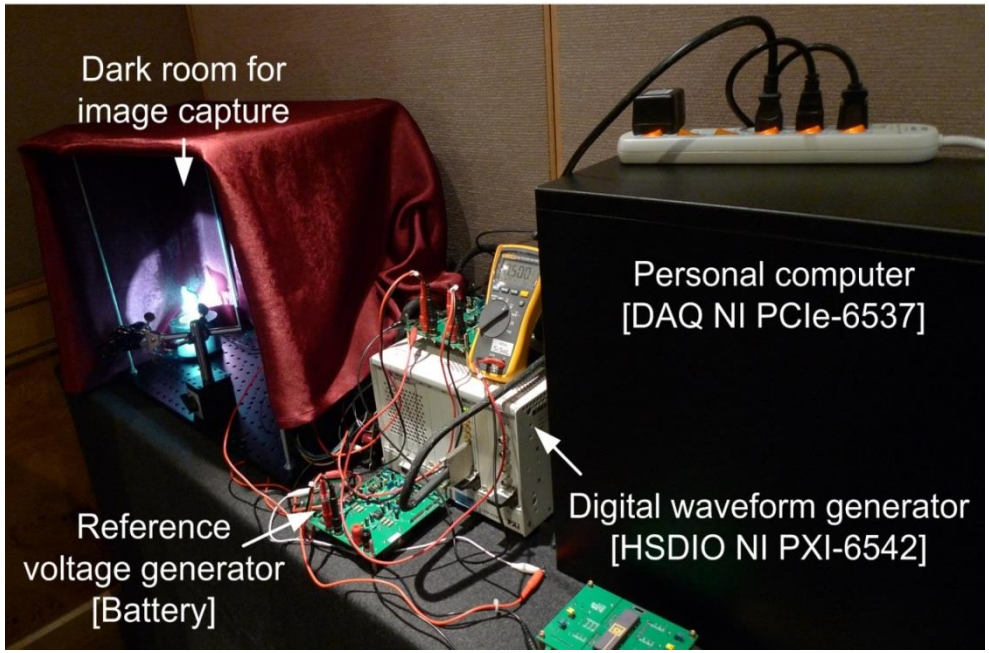


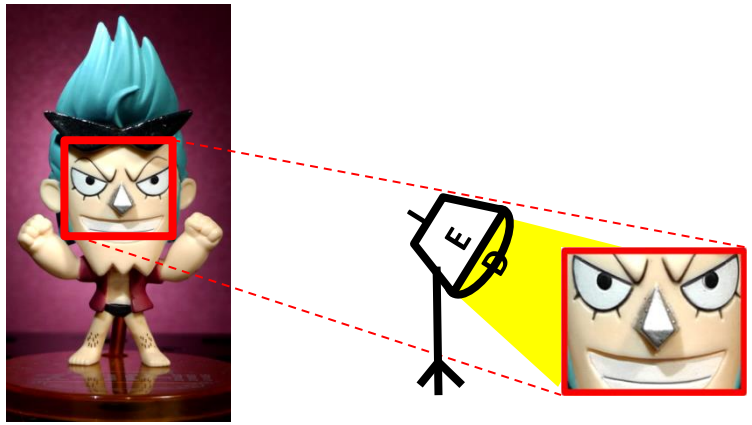
Chip Photo

- TSMC 0.18um 1P6M Standard Process

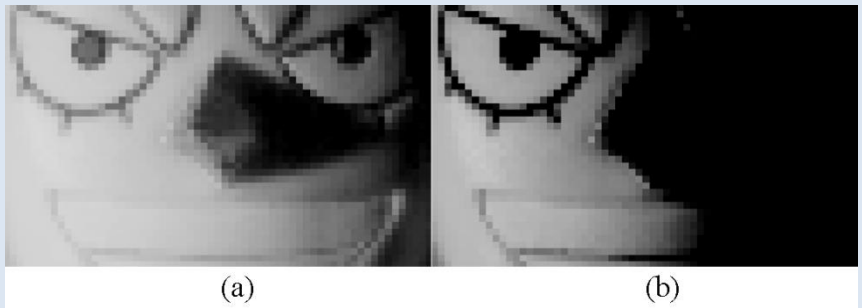


Setup & Captured Images





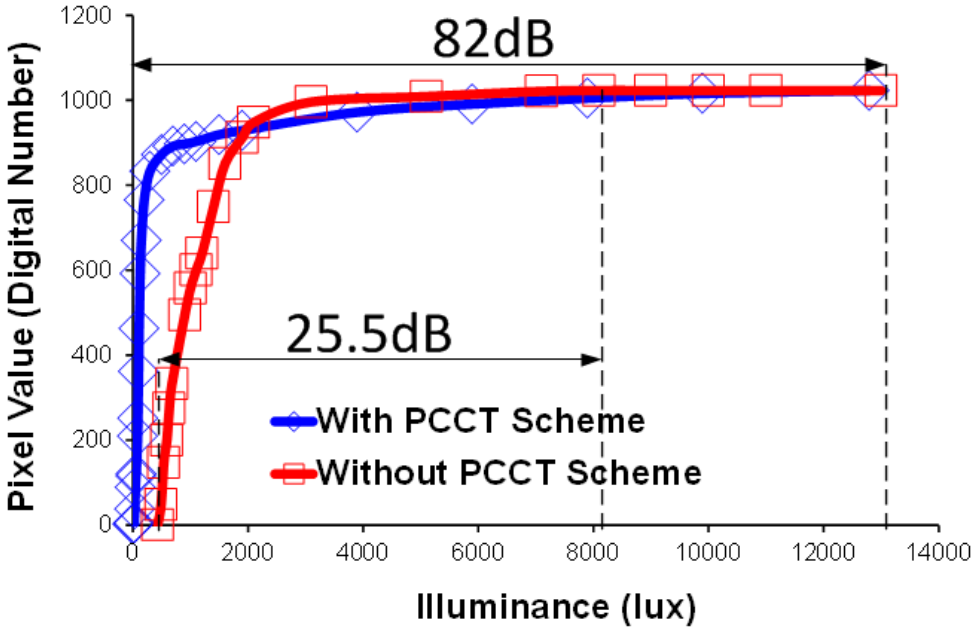
- **HDR Scene**



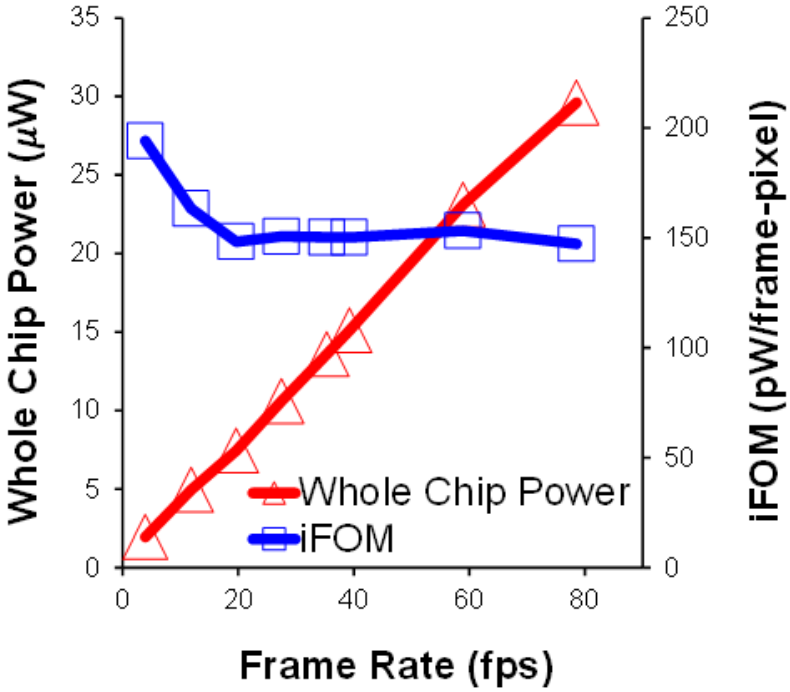
(a): With PCCT (b): Without PCCT

Measurement Result

- Photo-transfer-curve response



- Chip power and iFoM



Comparison Table

	[12] Kagawa (ISSCC-08)	[13] Cho (Symp. on VLSI Cir.09)	[14] Hanson (Symp. on VLSI Cir.09)	[15] Ay (ISSCC-11)	[8] This Work (ISSCC -12)
CMOS Technology	0.35-µm	0.13-µm	0.13-µm bulk	0.5-µm/5V	0.18-µm/1.8V
Pixel Count	128 x 96	128 x 128	128 x 128	54 x 50	64 x 40
Power Supply Voltage	1.35V	0.75V	0.5V (0.45-0.7V)	1.2V	**0.5V**
Dynamic Range	53.7 dB	54.2 dB	NA	NA	**82 dB**
Frame Rate	9.6 fps	15 fps	0.5 fps / 8.5 fps	7.4 fps	11.8-78.5 fps
Random Noise (dark)	0.95 LSBrms	1.92 LSBrms	NA	0.98 LSBrms	**0.65 LSBrms**
Pix. FPN (dark)	0.12%rms	0.66%rms	6.6%	NA	**0.055%rms**
Col. FPN (dark)	0.03%rms	0.06%rms	NA	NA	**0.016%rms**
Power Consumption (dark) (whole chip)	55.2µW	65.2µW	1.2µW@8.5fps 0.7µW@0.5fps	14.25µW	29.6µW@78.5fps 4.95µW@11.8fps
iFOM (whole chip) (pW/frame-pixel)	467.9	265.3	8.6@8.5fps 85.4@0.5fps	713.2	**147.3@78.5fps** **163.9@11.8fps**

W1: Summary

- A 0.5V 64x40 PWM CMOS imager with in-pixel comparator.
  - 0.5V supply voltage & power limiter
    - 4.95μW @ 11.8fps
  - Threshold-variation-canceling (TVC) scheme
    - CDS-like performed, 0.055% FPN
  - Programmable current-controlled threshold (PCCT) scheme
    - 56.5dB DR extension

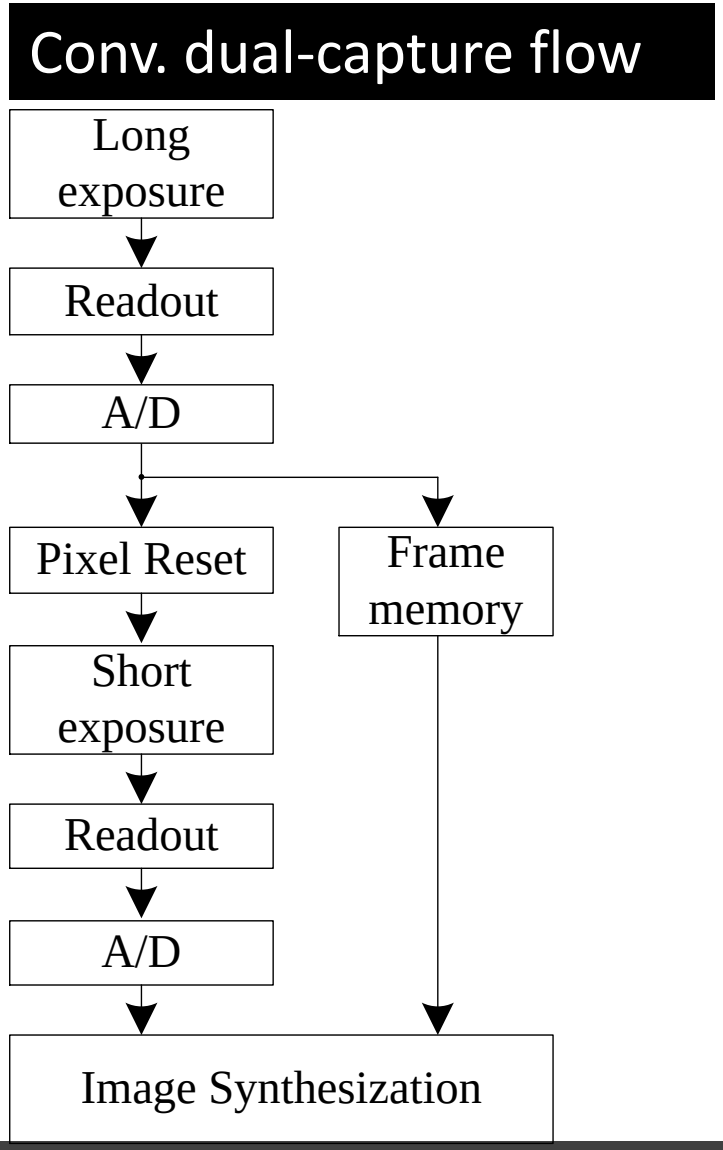
W2: High DR CIS

- Motivation
  - To develop an low-cost, compact HDR image sensor with on-chip synthesis capability.
- Key Features
  - High Dynamic Range
    - Dual-exposure with illumination detection operation
  - On-chip synthesis
    - Single frame output with HIP/LIP index
  - Low-cost & compact
    - No frame memory + embedded column-wised ADC

HIP: high illuminated pixel
LIP: low illuminated pixel.

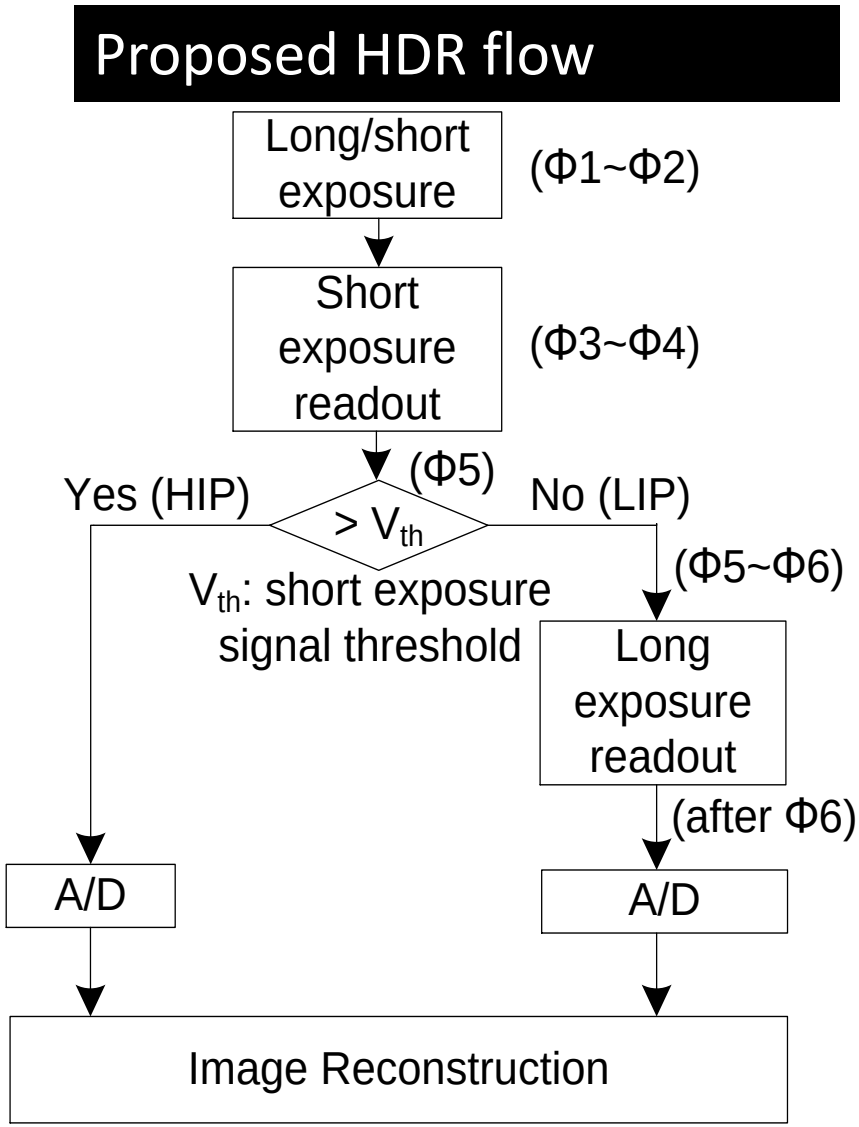
Conventional Approach

- Disadvantages
  - 2 A/D conversions.
  - Dual exposure and readout time.
  - Need frame memory

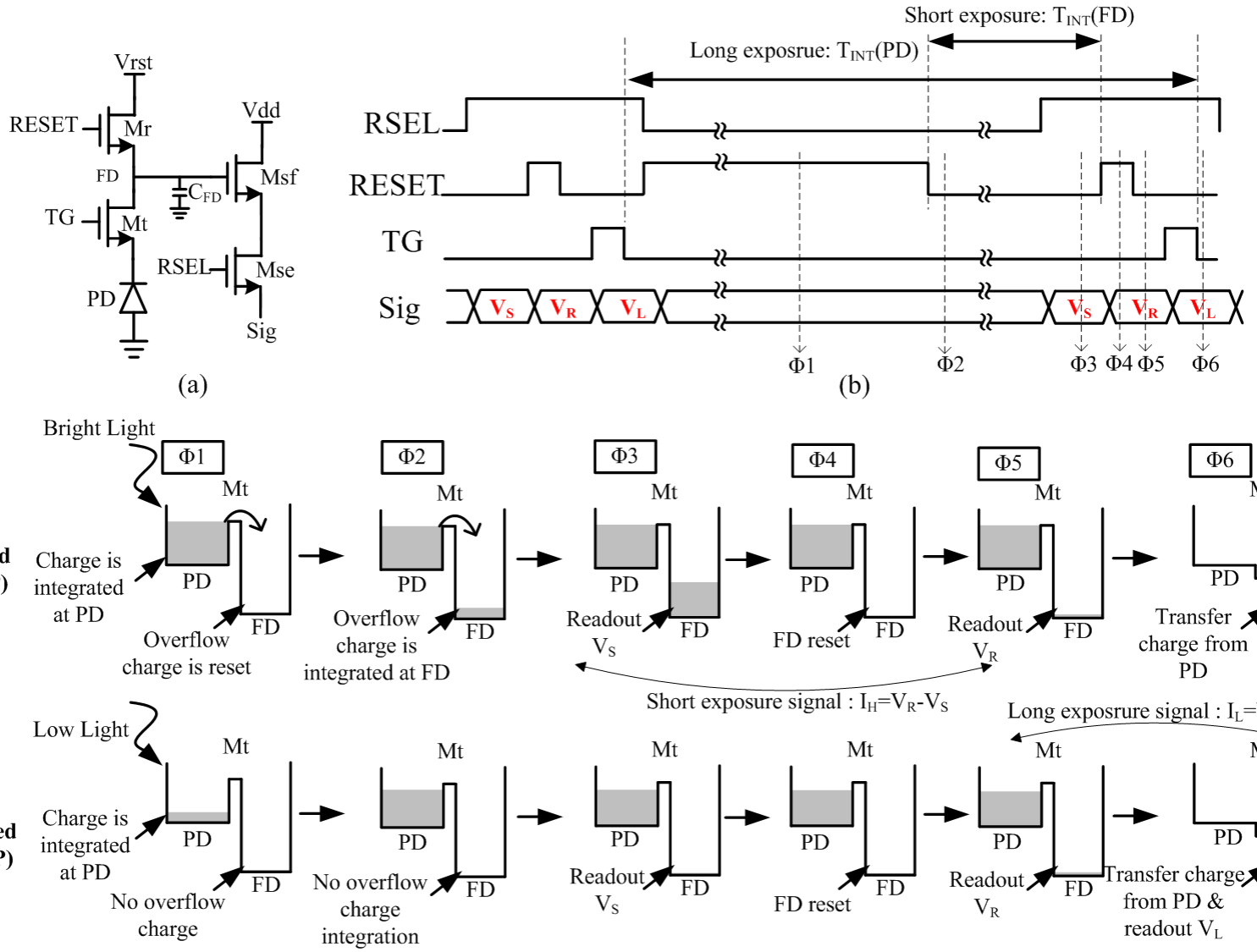


Proposed HDR Flow

- Features
  - Overlapped long/short exposure in a frame time
  - Overflow detection
  - HIP/LIP detection with index bit
  - Dual exposure, single A/D conversion
  - No frame memory

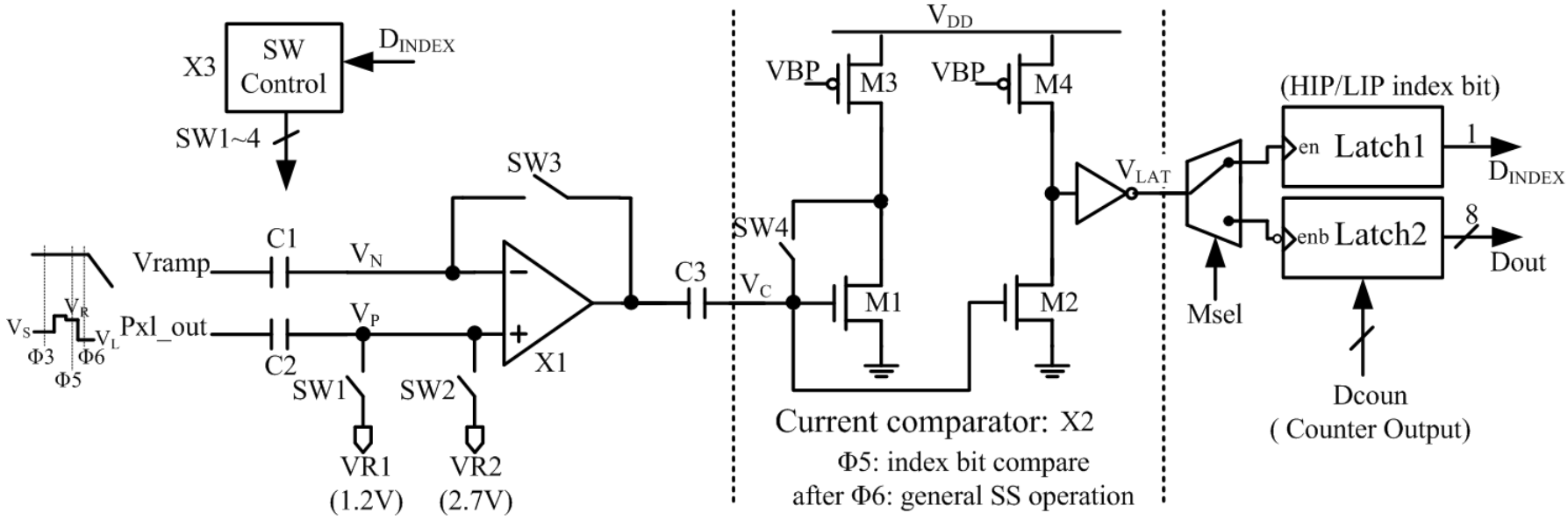


Pixel Operation

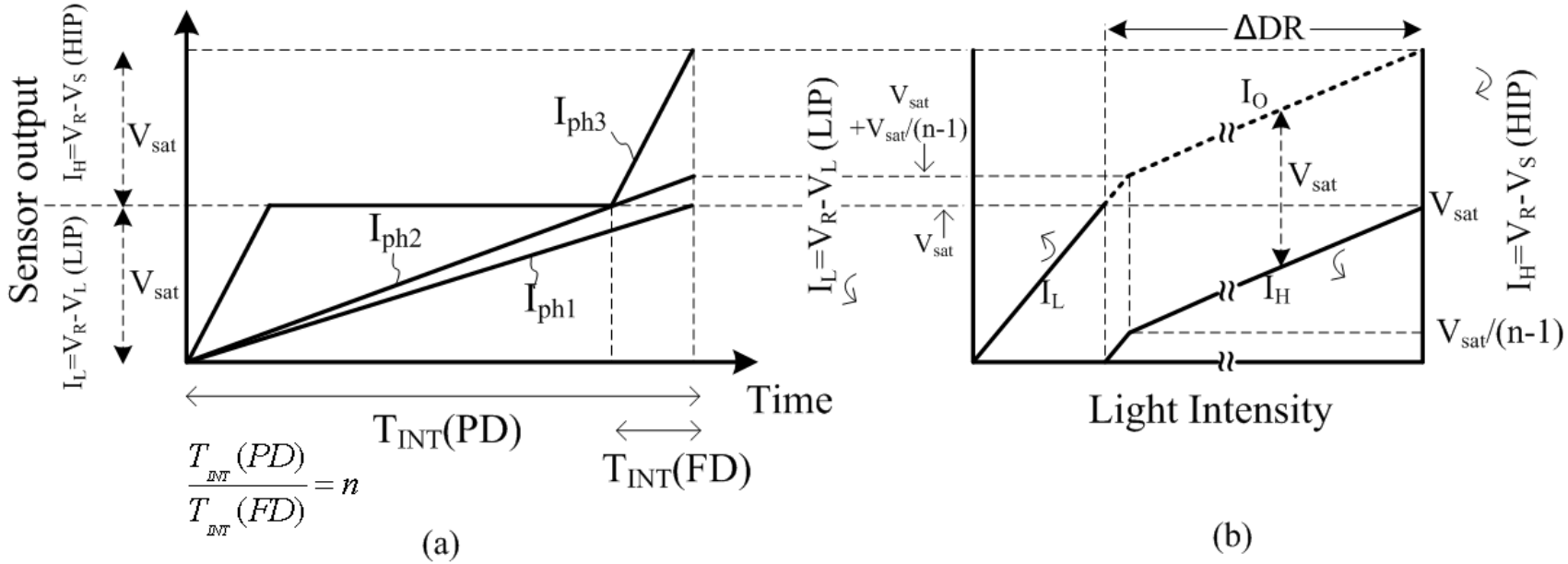


Column-wise ADC

- SS-ADC with integrated HIP/LIP detection and CDS readout operation
  - For HIP, signal (V_R-V_S) with T_{short} is readout
  - For LIP, signal (V_R-V_L) with T_{frame} is readout



Photoelectric Transfer



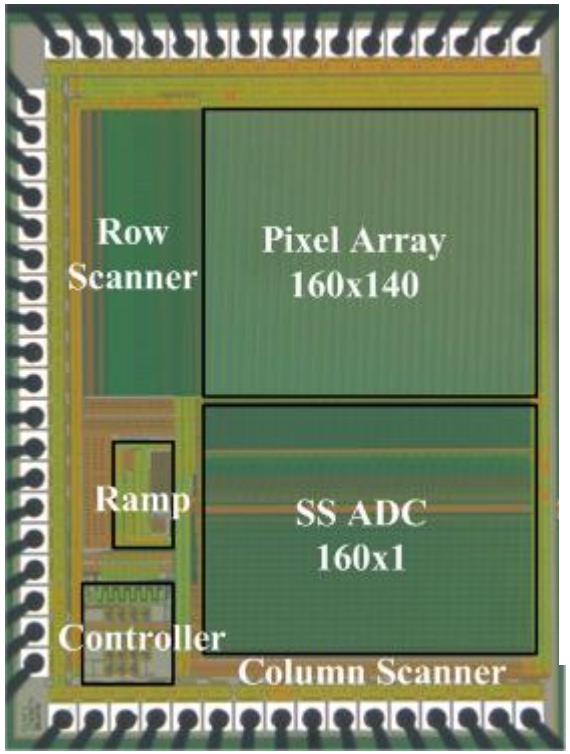
$$DR = 20 \times \log\left(\frac{Q_{sat} / T_{INT}(FD)}{Q_n / T_{INT}(PD)}\right)$$

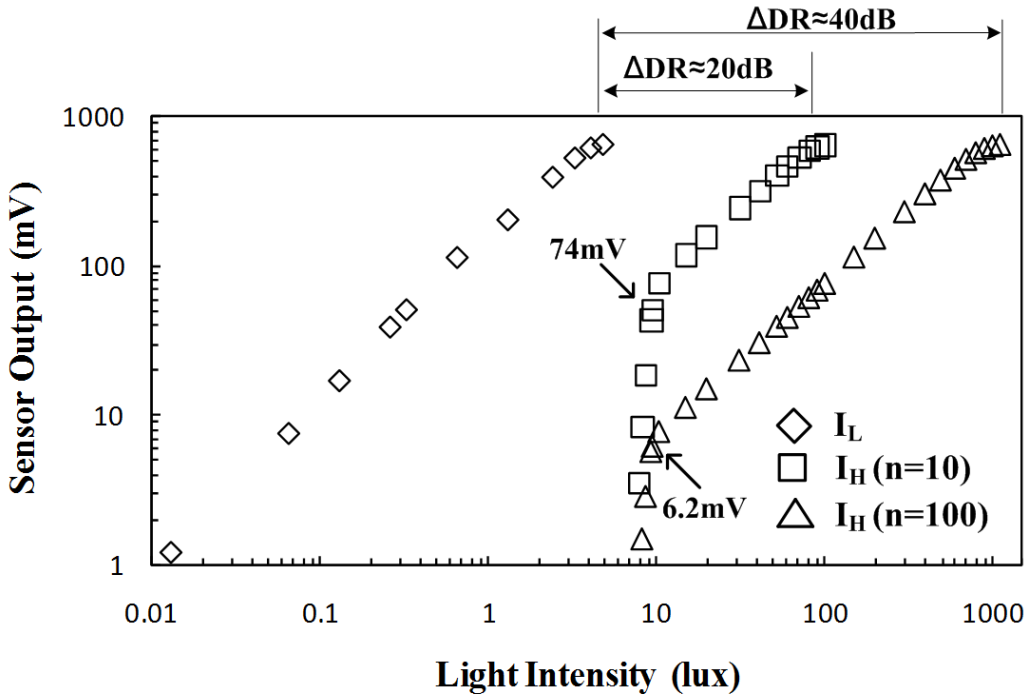
$$= 20 \times \log\left(\frac{Q_{sat}}{Q_n}\right) + 20 \times \left(\frac{T_{INT}(PD)}{T_{INT}(FD)}\right)$$

Qsat: saturation charges
Qn: noise floor
T_{INT}(PD): long exposure time
T_{INT}(FD): short exposure time

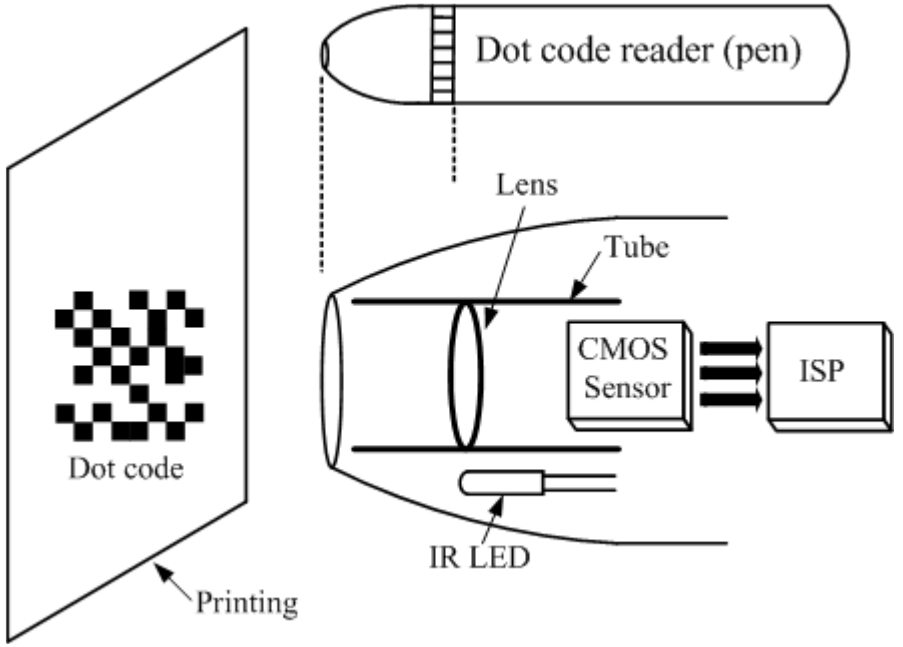
Measurement Results

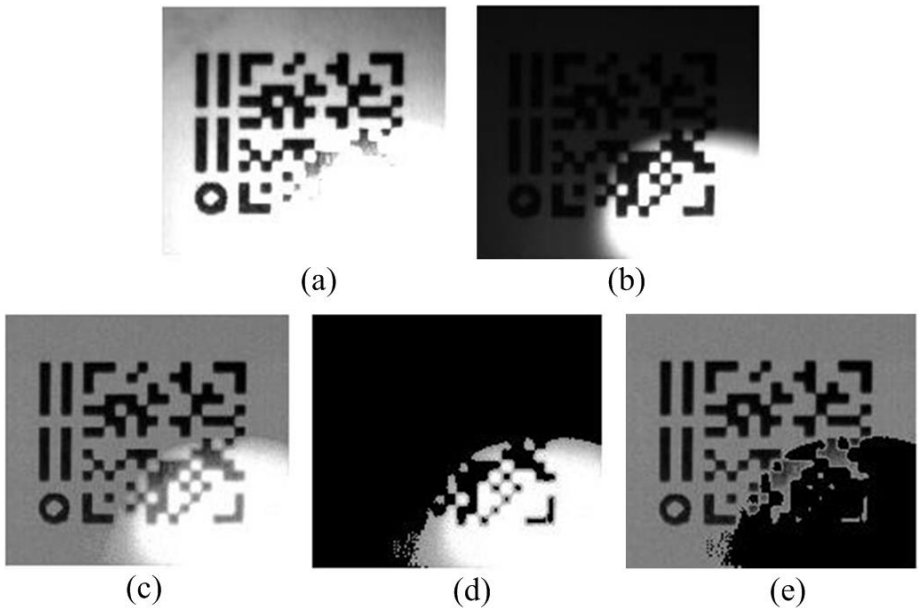
- TSMC 0.18um 1P6M CIS Process





Sample Images





(a) Long exposure.
(b) Short exposure.
(c) Proposed dual-exposure single capture method.
(d) HIP image.
(e) LIP image.

Chip Specifications

Process technology		0.18um 1P4M CIS
Die Size		2 x 1.5 mm^2
Pixel Size		5.6 x 5.6 um^2
Array Format		160 (H) x 140 (V)
Fill Factor		38%
Sensitivity		5.33 V/lx·s
DR	Without extension	51dB
	With extension	91dB
Frame rate		60fps
ADC resolutions		8 bits
ADC DNL/INL		(+0.16,-0.24) / (+0.28,-0.52)
Column FPN (@DN=125)		0.16%
Power Supply		3.3V
Power Consumption		6.4mW (@60fps)

Comparison Table

For single WDR image	This [9] (TED-12)	[16] Akahane (JSSC-06)	[17] Dongsoo (TED-08)	[18] Mase (ISSCC-05)
Array Format	160x140	640x480	320x240	664x488
# of A/D conversion times per pixel (@dual-exposure)	1	4	3	2
ADC Type	Column-wise SS	Off-chip ADC	Column-wise SS	Column-wise Cyclic
Column ADC Area (um^2)	5.6x713	NA	11.2x 928	20x1550
Column ADC Power (uW)	40	NA	37.5	149
FOM (mm^2*uW)	0.16	NA	1.17	9.24

W2: Summary

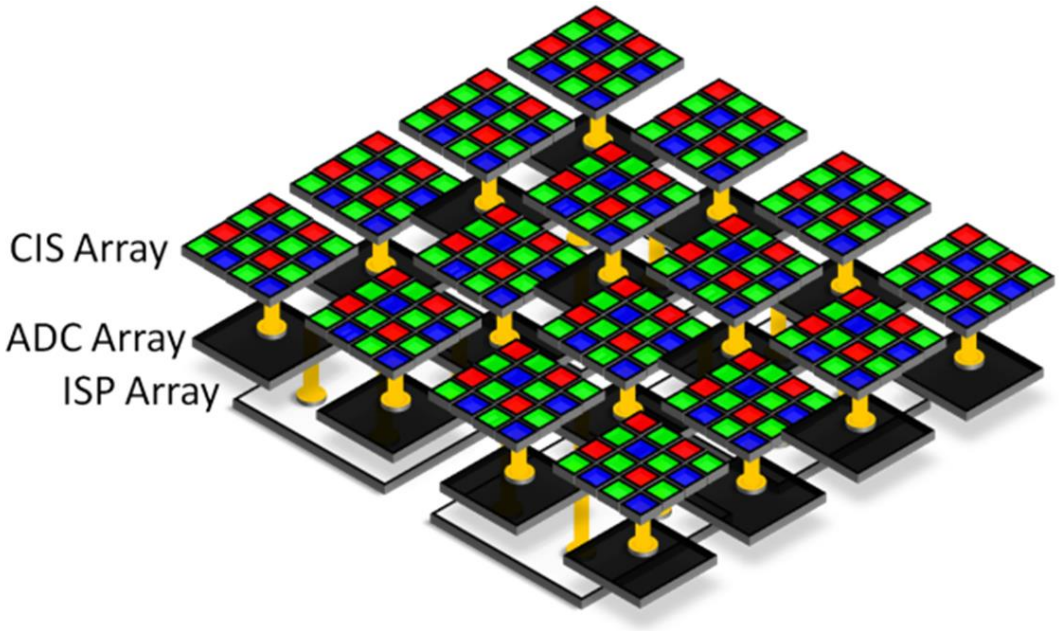
- A 3.3V 91dB Dual-exposure Single Capture CMOS imager
  - In-pixel illumination detection and index
    - No frame memory
    - No off-chip image synthesization
    - Low cost / high speed
  - Embedded column parallel SS ADC
    - DNL: +0.16/-0.24 LIB, Column-FPN: 0.16%

W3: High Speed CIS

- Motivation
  - To develop an high-frame-rate, high-resolution CIS with 3D-stacking architecture.
- Key Features
  - High resolution
    - 2.8um 4-shared pixel
  - High frame rate
    - Parallel readout through ADC array layer
  - Scalable architect for 3D-stacking
    - Modulized sub-array design and control

Application

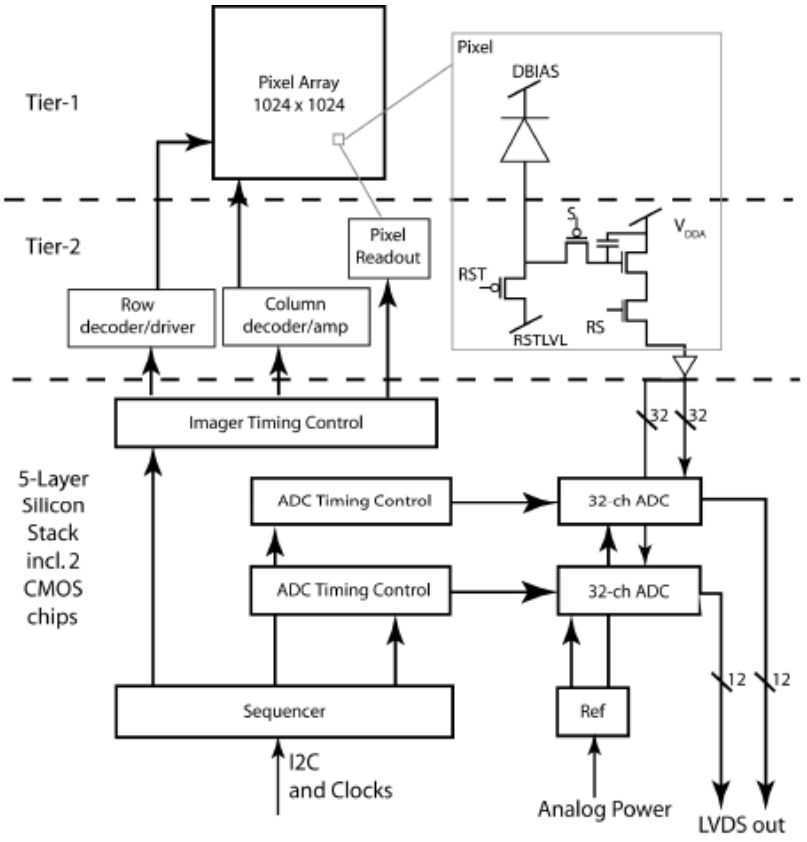
- 3D-Stacking Integrated CMOS Imagers.
  - Optimized technology for each layer
  - Wide IO: high resolution and high frame rate
  - Scalable modulized design



Problem

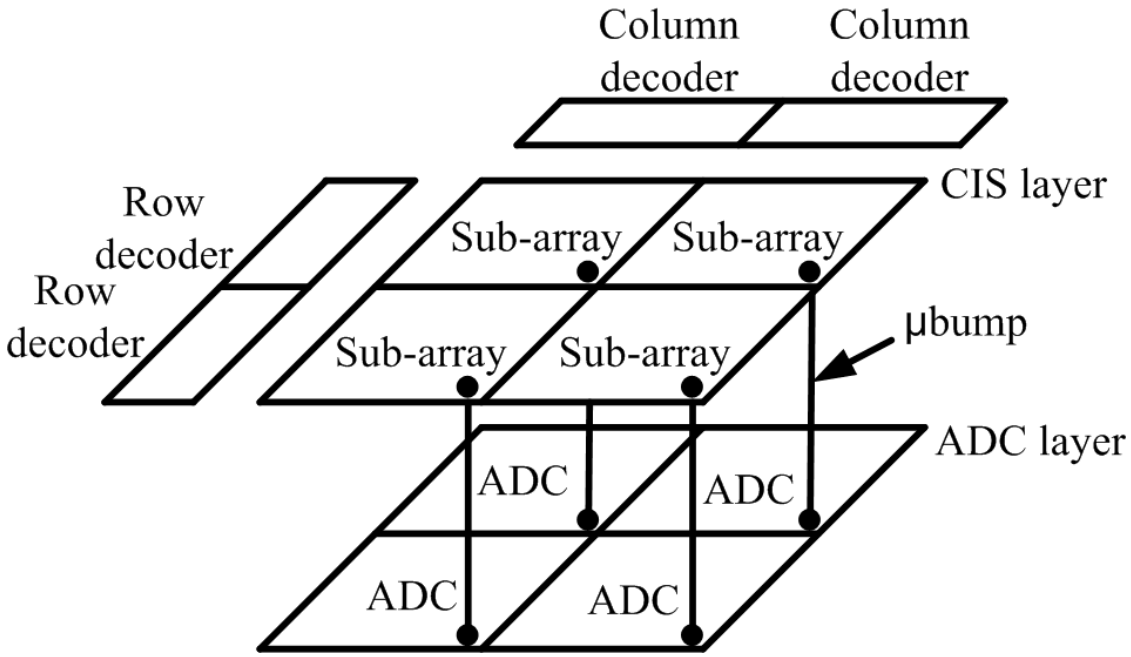
- Prior Art: 3D CMOS imager with TSV
  - Pixel pitch is restricted by via dimension.
  - Testing issue before stacking.

Ref. [19]



Proposed CIS Layer

- Composed of Scalable Sub-array Modules
  - Connected to ADC using a single µbump
  - Each sub-array works in parallel
  - Sub-array size depends on ADC area and bandwidth



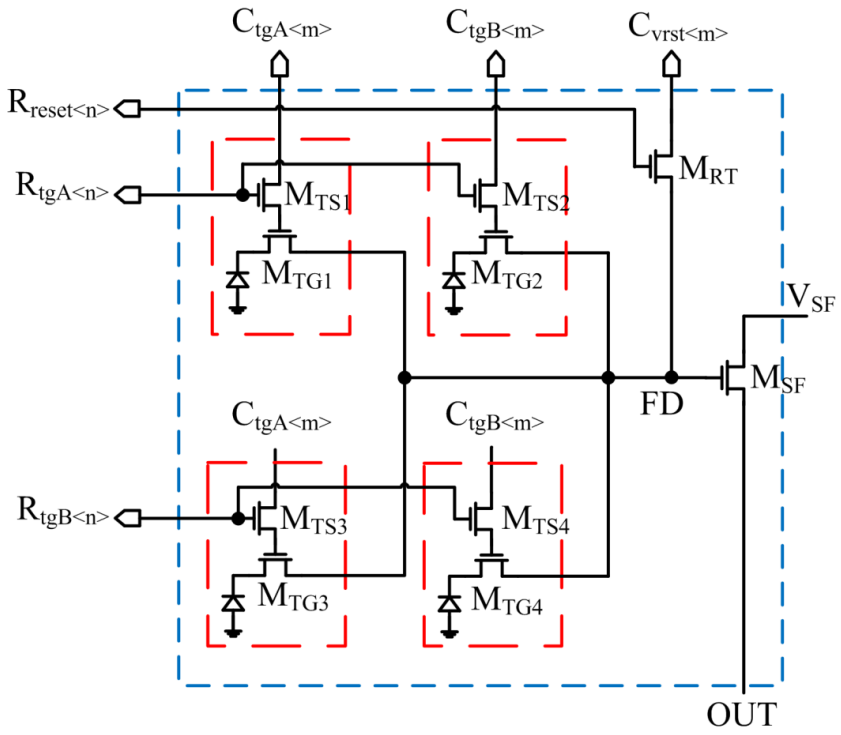
Design Challenges

- Array Parallel Instead of Row-Parallel
  - No CDS area/timing for readout
  - CDS in pixel rate → settling issue
  - New exposure and readout Control for module design
  - Small in-pixel area overhead allowed for extra devices
- Testing Issue in 3D-Stacking Solution
  - No I/O before stacking package
  - Need pre-stacking BIST function

4-Shared Pixel

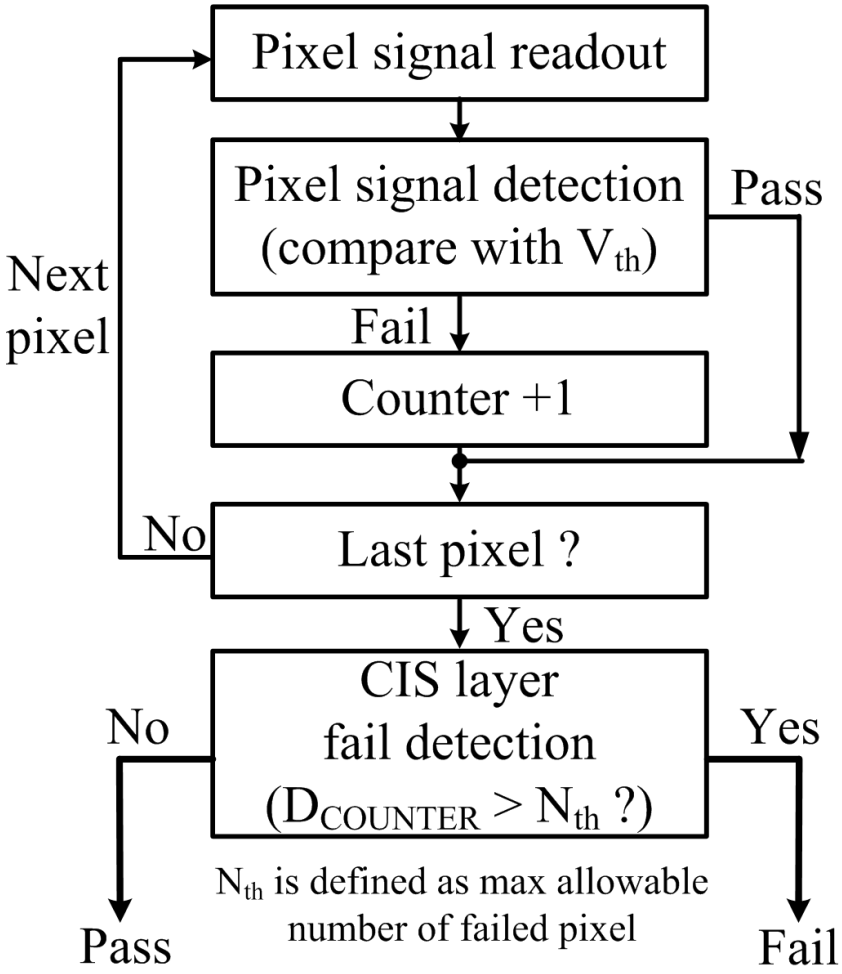
- Single Output in a Sub-array of 192x128
  - Need in-pixel X-Y decoding for Tg, Rst, and SF
  - Column: CtgA, CtgB, Cvrst
  - Row: Rreset, RtgA, RtgB
  - No in-pixel R_sel device
  - Pass-transistor logic
  - 10T/4-shared pixel

2.5T per pixel



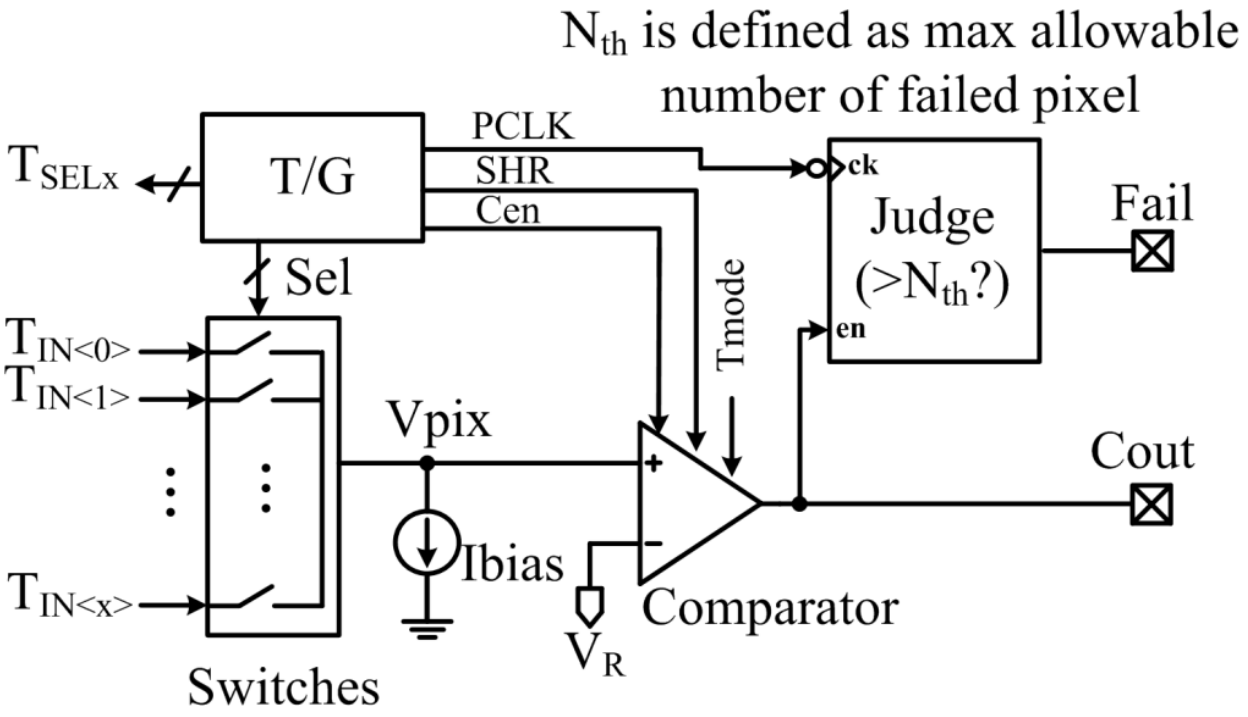
BIST Mode Flow

- BIST Operation
  - No additional in-array circuit.
  - Compare pixel output to a preset threshold sequentially.
  - Count up the number of failure pixels.
  - If Dcounter > Nth, this CIS layer is failed.



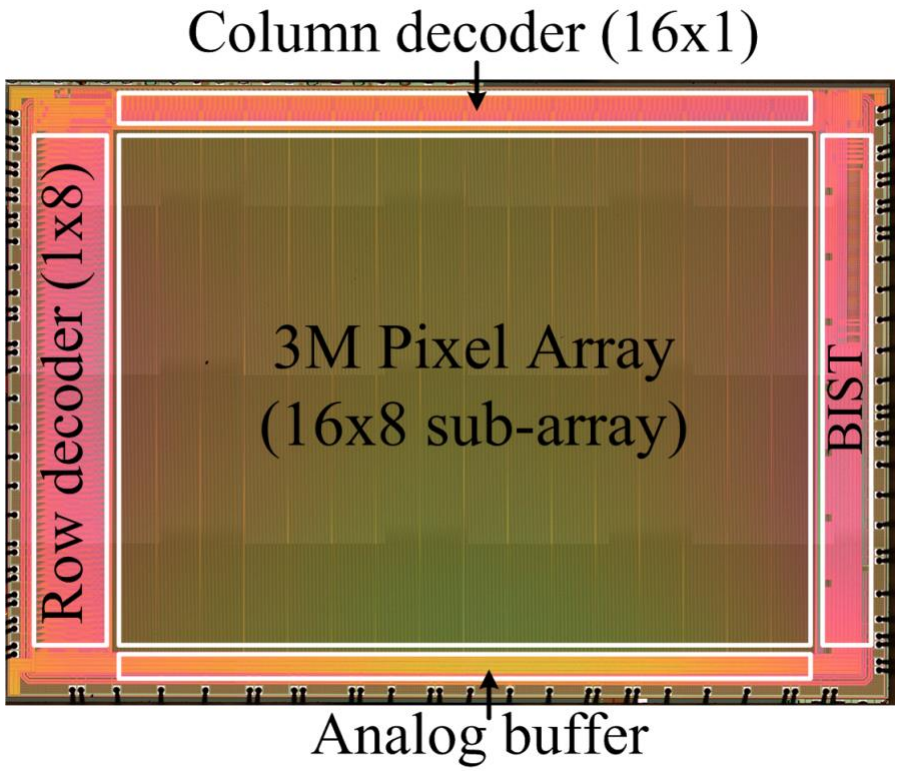
BIST Implementation

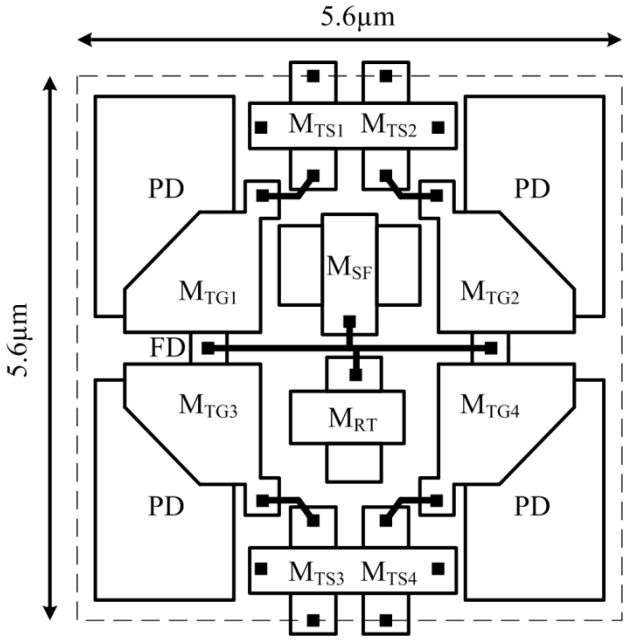
- Dark/Bright Test with Programming Criteria and Threshold



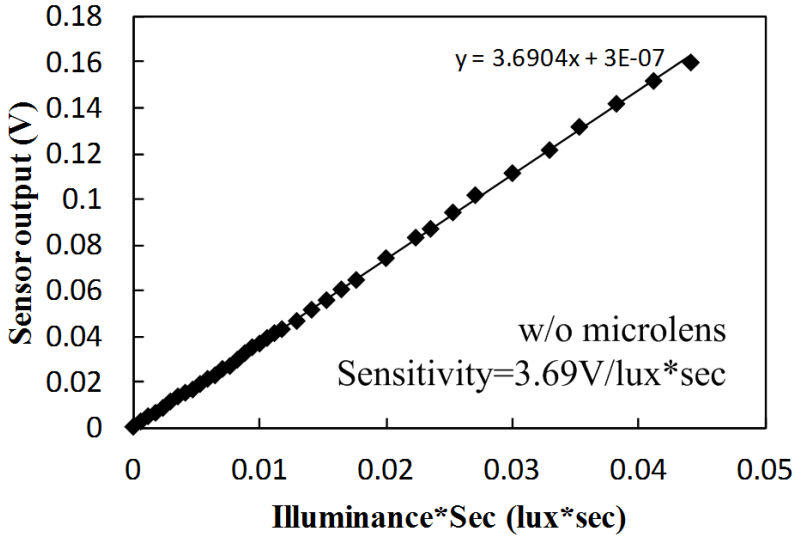
Chip Micrograph

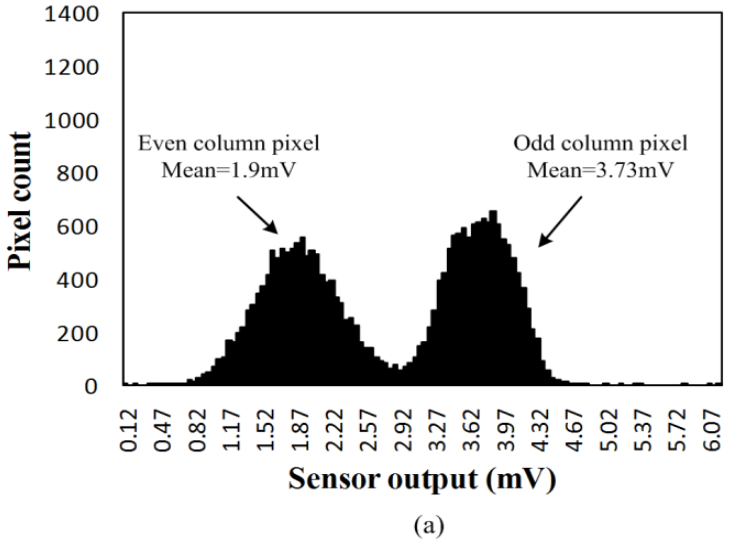
- TSMC 0.18um 1P6M CIS Process
  - 3Mega array, 2.8umx2.8um pixel, 16x8 modules



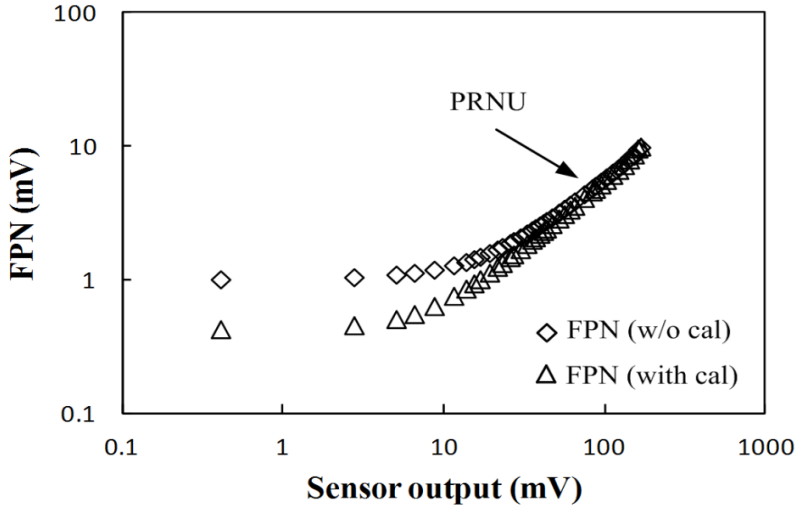


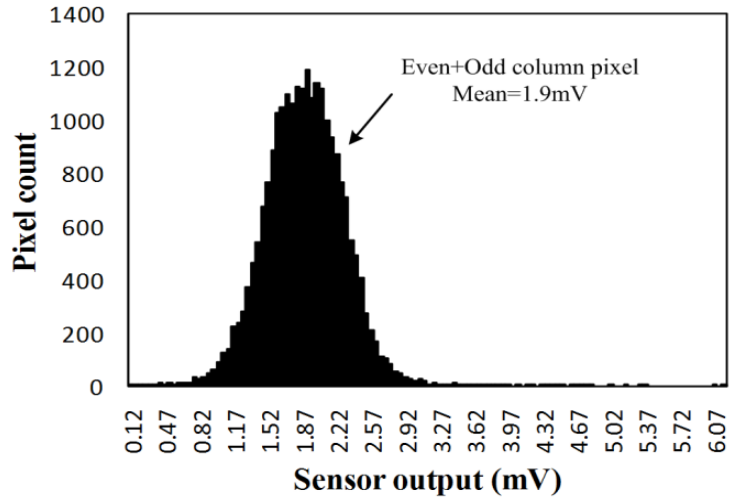
Measurement Results





(a)





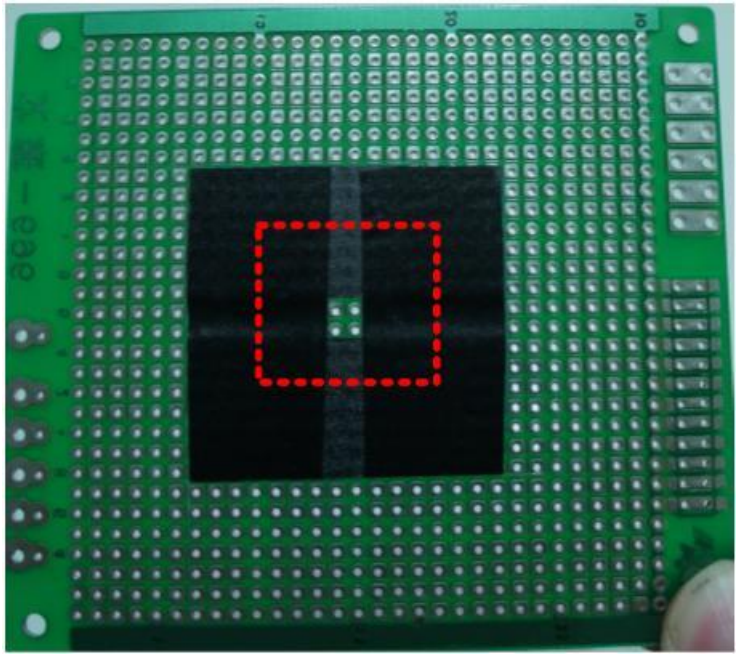
(b)

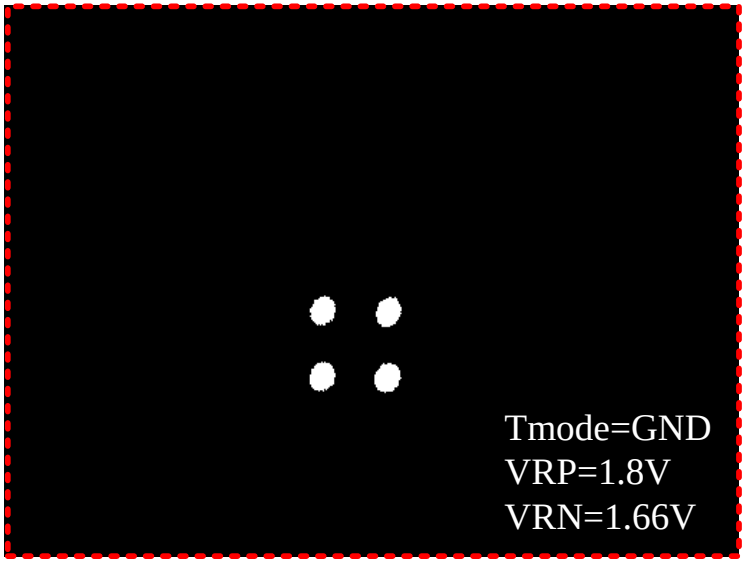
Captured Image

- 3Mega, 100fps

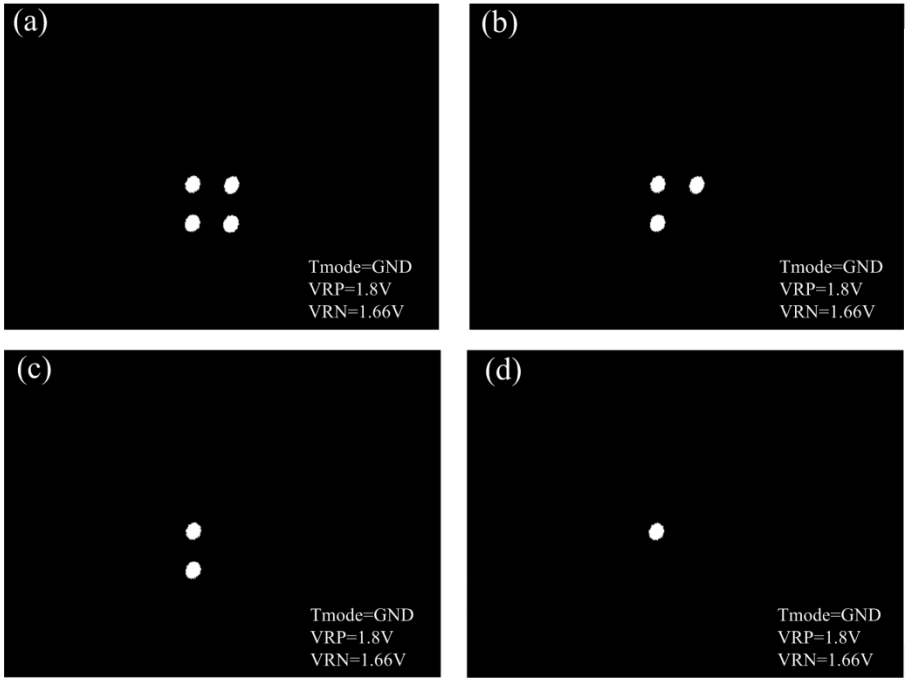
Captured Image (BIST)

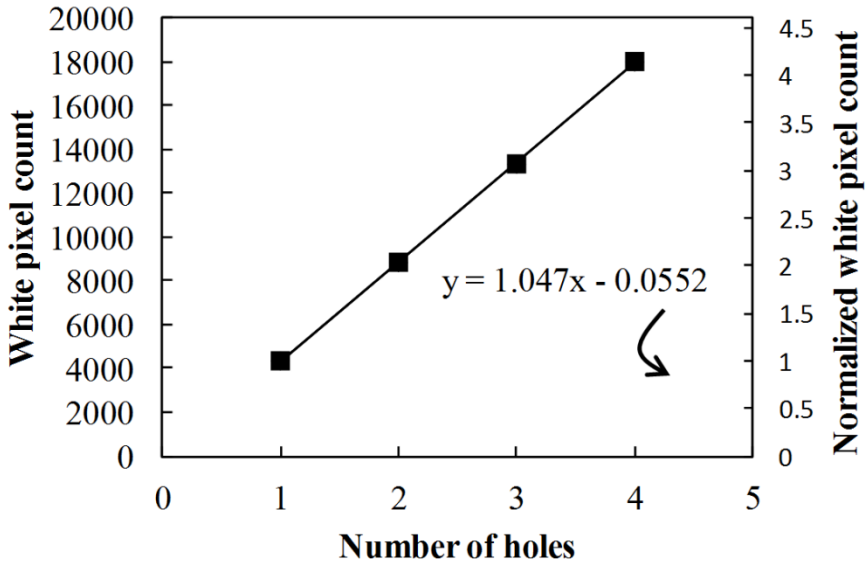
- Use Dotted Pattern to Simulate the Dead (Wounded) Pixels





BIST Measurement Result





Chip Specifications

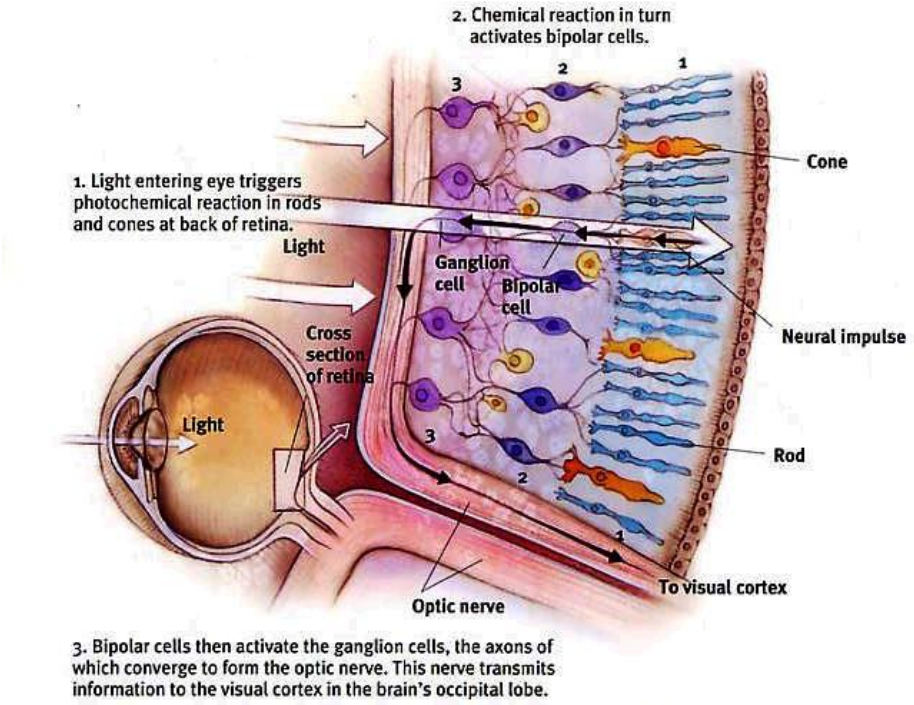
Technology	TSMC018 CIS
Light shielding layer	Metal 4
Chip size	$7.2^{H}x5^{V}mm^{2}$
Array format	$2048^{H}x1536^{V}$
Optical format	1/2.5”
Pixel size	$2.8x2.8um^{2}$
Pixel fill factor	28%
Transistor per pixel	2.5Transistors
Frame rate	100fps
Pixel rate	2.5Mhz
Conversion gain	$37\mu V/e^{-}$
Saturation	$6500e^{-}$
Sensitivity	3.69V/lx*sec
Random noise	$0.58mV_{rms}$
FPN (with calibration)	$0.43mV_{rms}$
Dark output voltage	$0.62mV/sec(@27^{0}C)$
Power (w/o analog buffer)	19mW (@100fps)

W3: Summary

- 2048x1536 (3Mega) 100fps CIS layer for 3D-stacking imager
  - 2.5T pixel with X-Y decoding
  - Module size: 192x128 array (530x360um^2)
  - One u-bond per module connected to ADC layer
  - Scalable design: 6x18 modules for 3Mega.
- Embedded BIST for Pre-Stacking Testing
  - No extra in-pixel circuit
  - Fail/Pass report with tunable testing criteria (signal threshold & defect count)
- Stacking package (CIS+ADC+ISP) is on-going…

W4: CIS for Artificial Retina

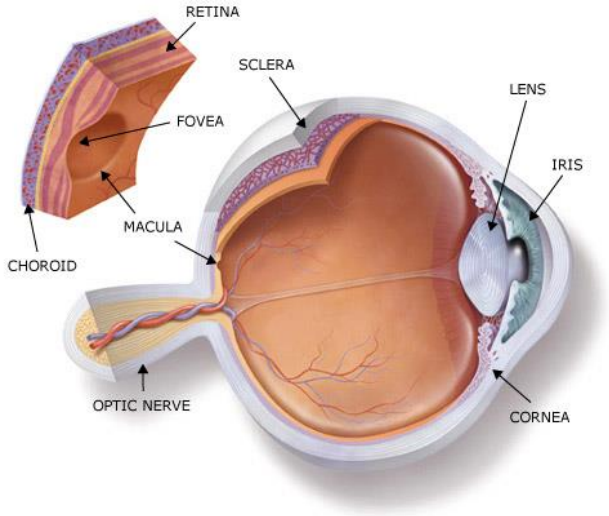
- Motivation
  - To replace the function of damaged neuron cell
- Key Features
  - High Resolution
    - Vision recovery
  - Low power
    - Lifetime & Safety
  - Highly integrated
    - Small size
    - Min. external components



Ref. [20]

Application

- Artificial Retina
  - Retinitis pigmentosa (RP)



  - Age-related macular degeneration (AMD)

Ref. [21] [22] [23]

Problem & Solution

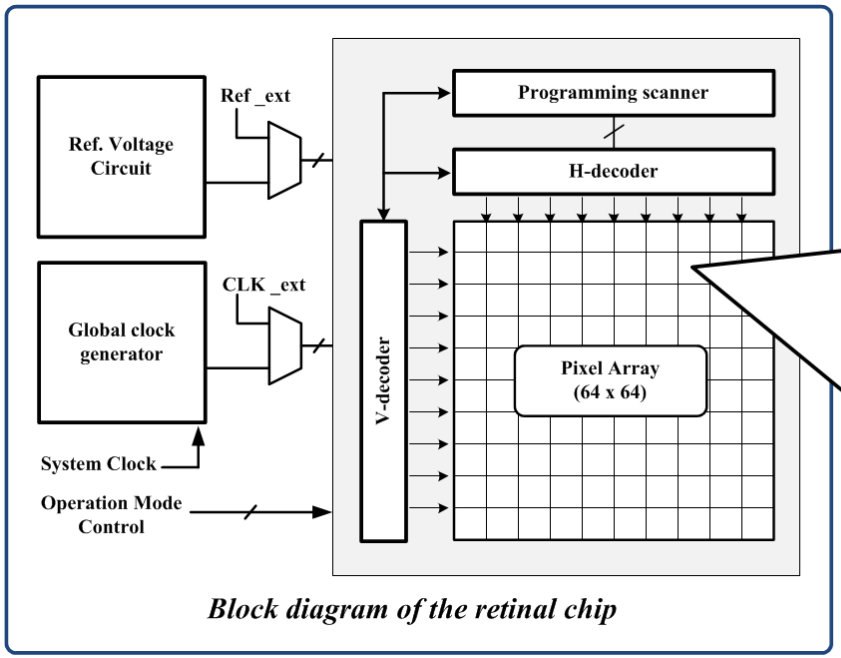
- Low-Power Solution
  - 0.8V operation
  - Power control
- Low-Voltage Operation
  - Pulse frequency modulation (PFM) image sensor
  - Frequency-to-voltage converter
- High Resolution & Integration
  - Sense-and-stimulus (SAS) pixel
  - Bendable silicon
  - Minimum external component & wiring

Operation Modes

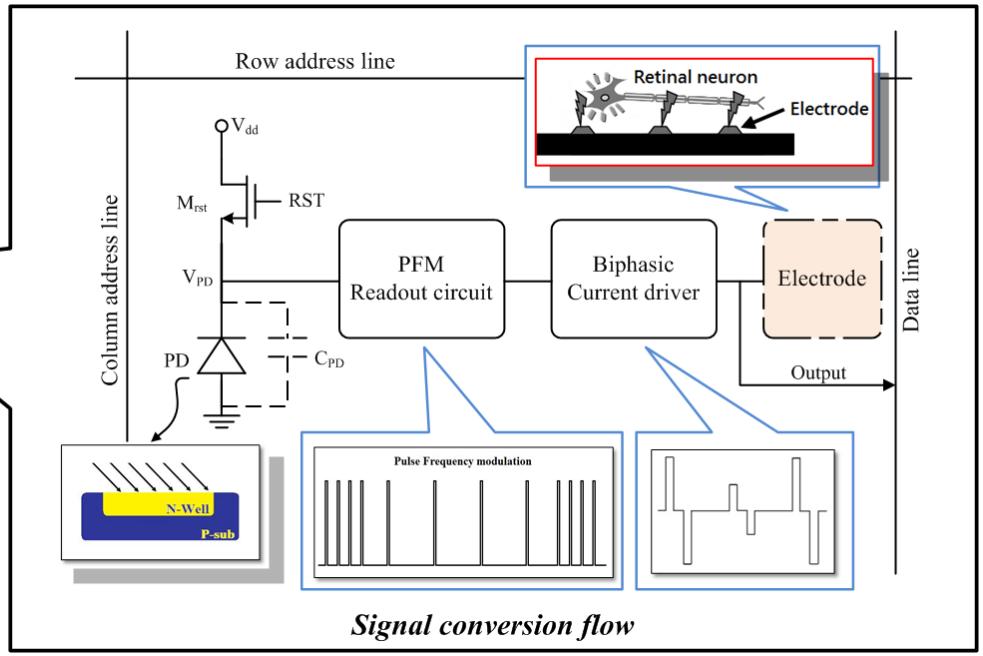
- Test Mode
  - Mux out in-pixel biphasic current sequentially
- Programming Mode
  - Patterned electrical stimulus array output
  - Programmable size of sub-array scan
- Implanted Mode
  - Parallel current output through in-pixel electrode
  - Minimized I/O number as 4 (power, gnd, clk, vref)

Retinal Chip

- A CMOS image sensor (CIS) array integrated sense-and-stimulus (SAS) pixel

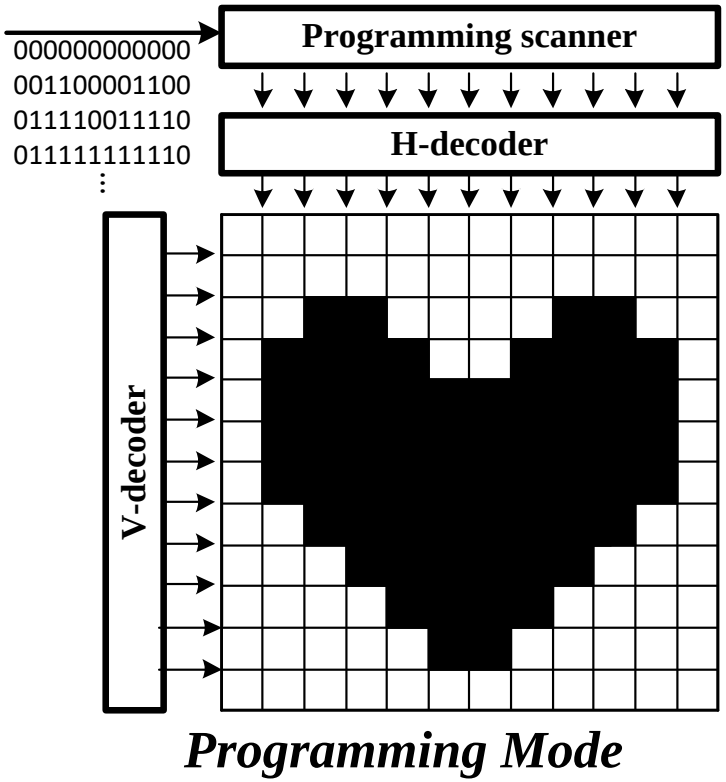


Block diagram of the retinal chip

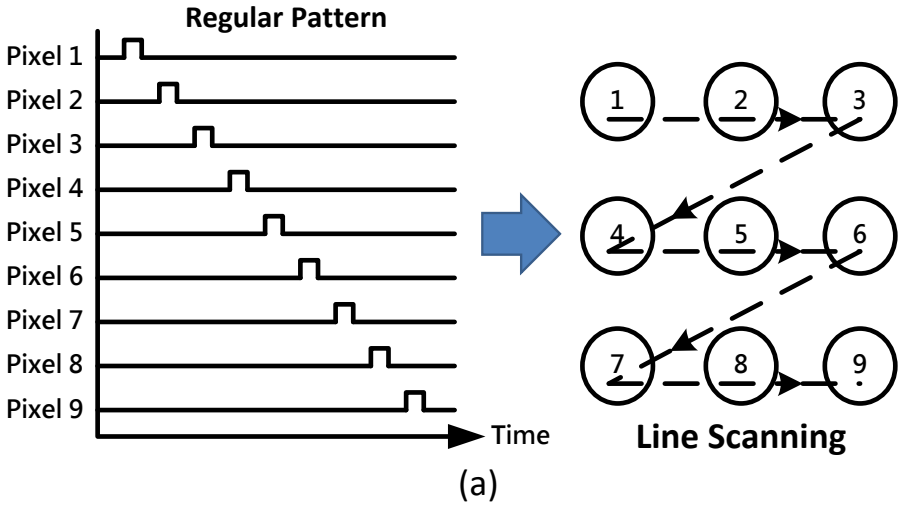


Signal conversion flow

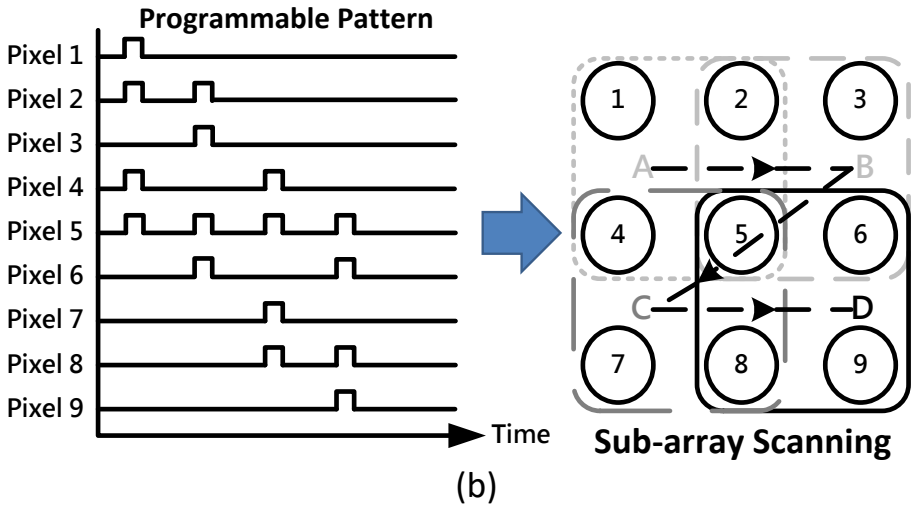
Programming & Scanning



Programming Mode



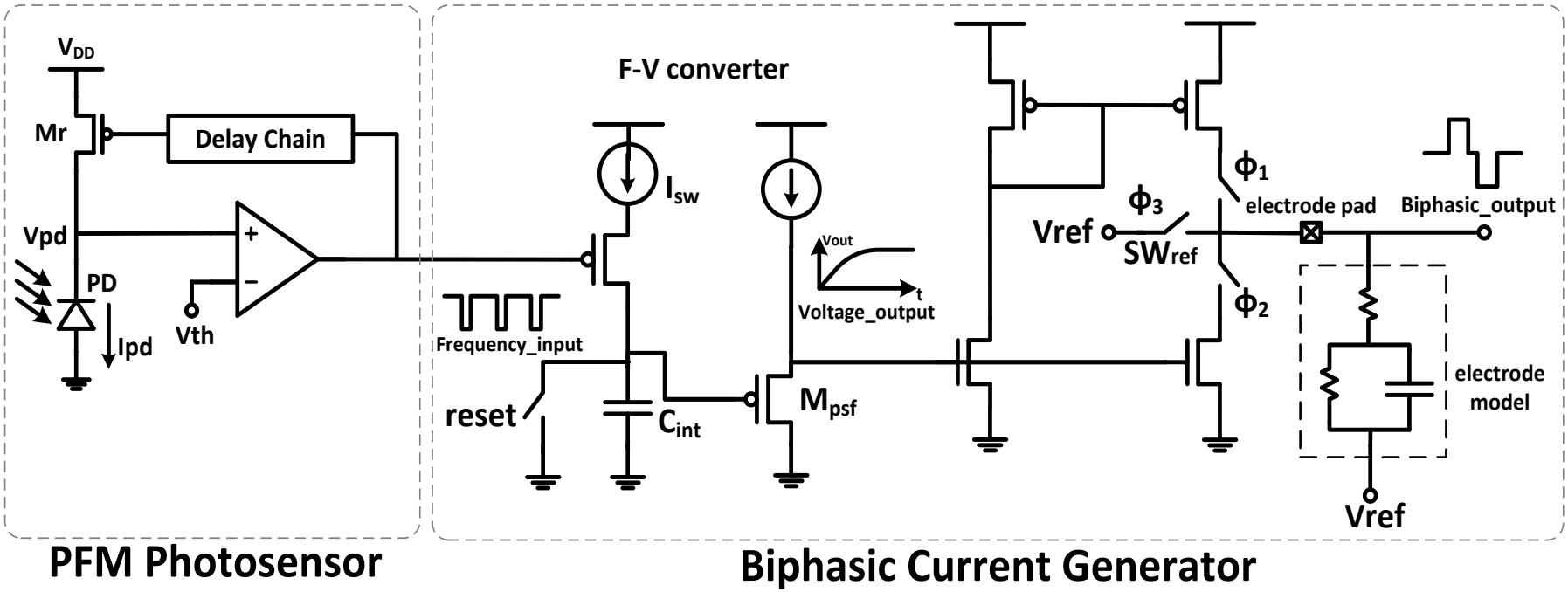
(a)



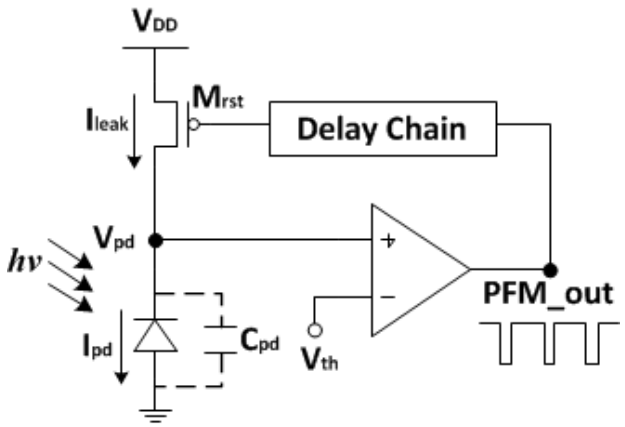
(b)

Sensing-and-Stimulus

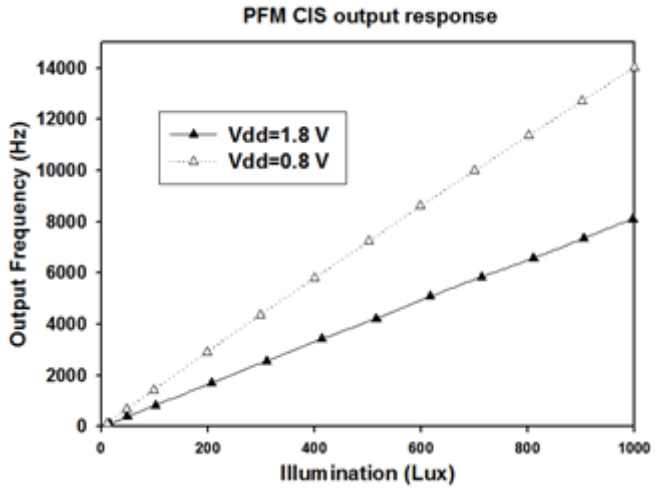
- Proposed SAS pixel

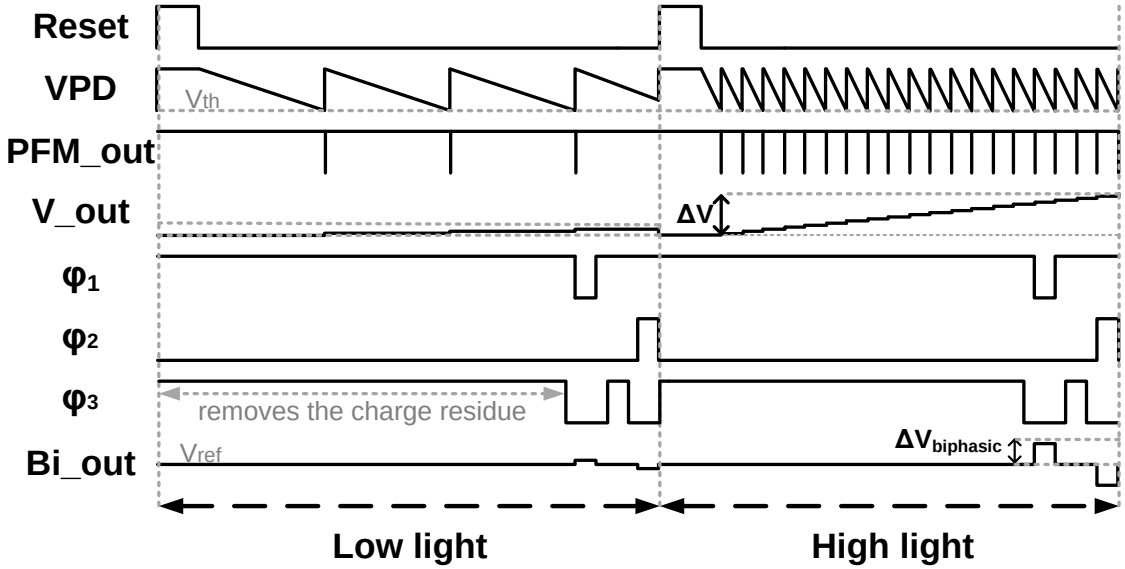


Lux to Biphasic



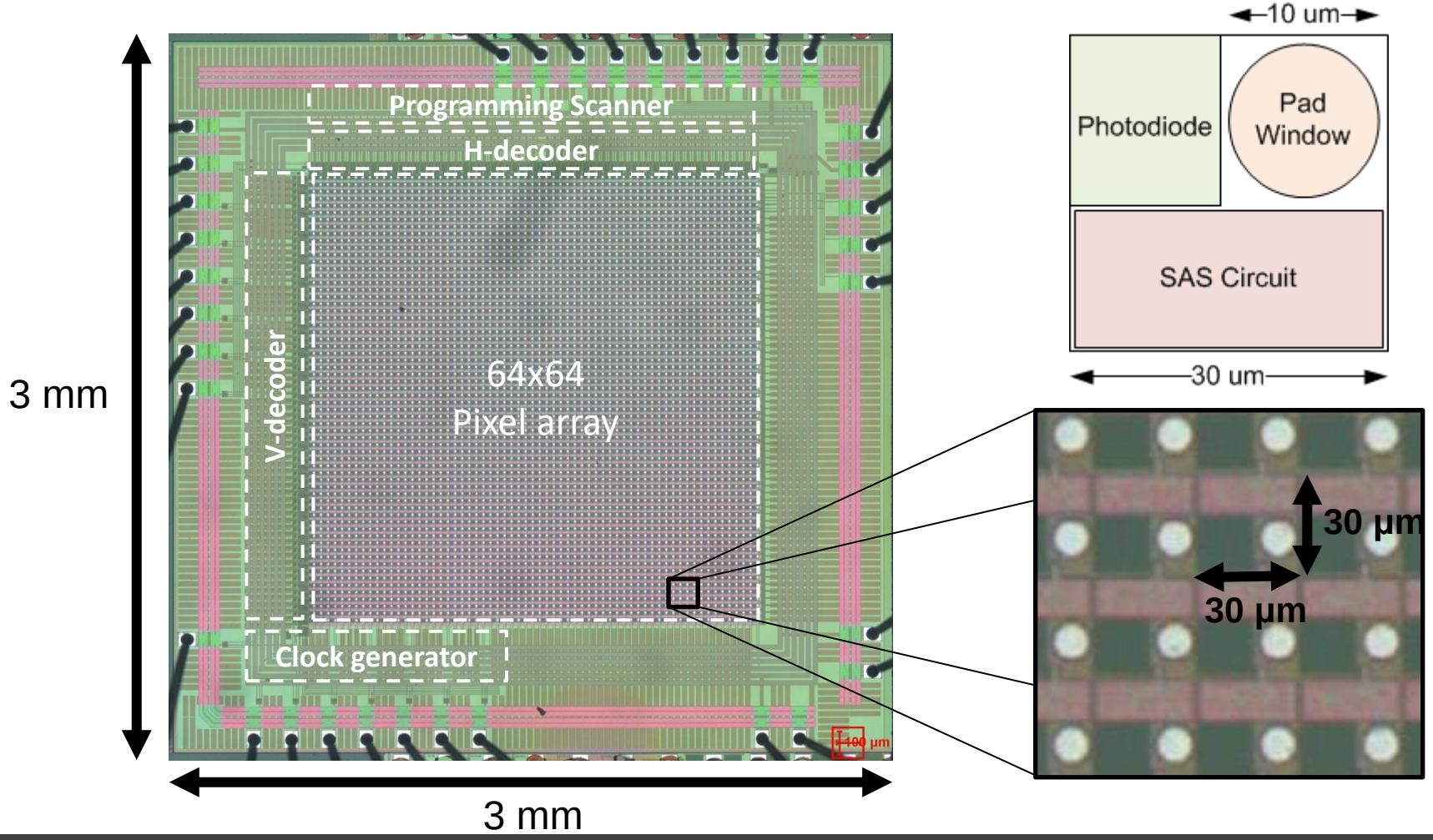
PFM Photosensor





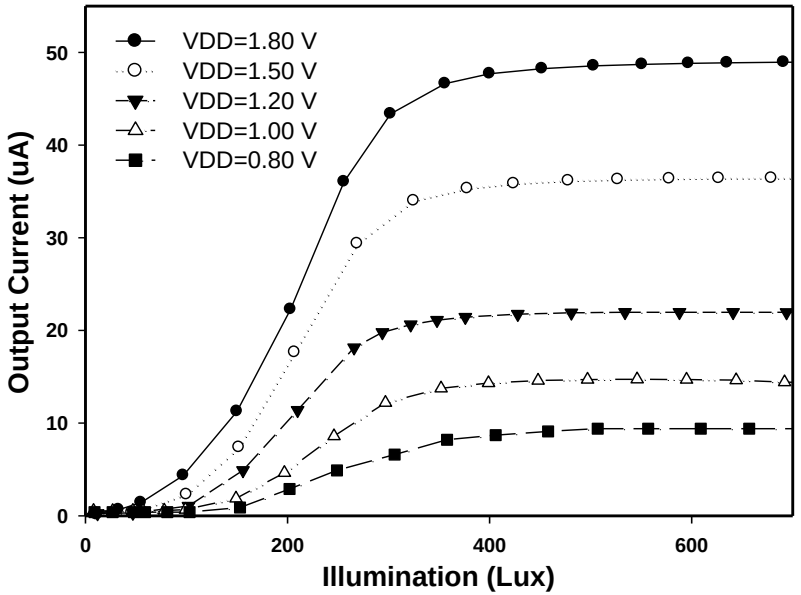
Chip Photo

- TSMC 0.18um 1P6M CIS Process

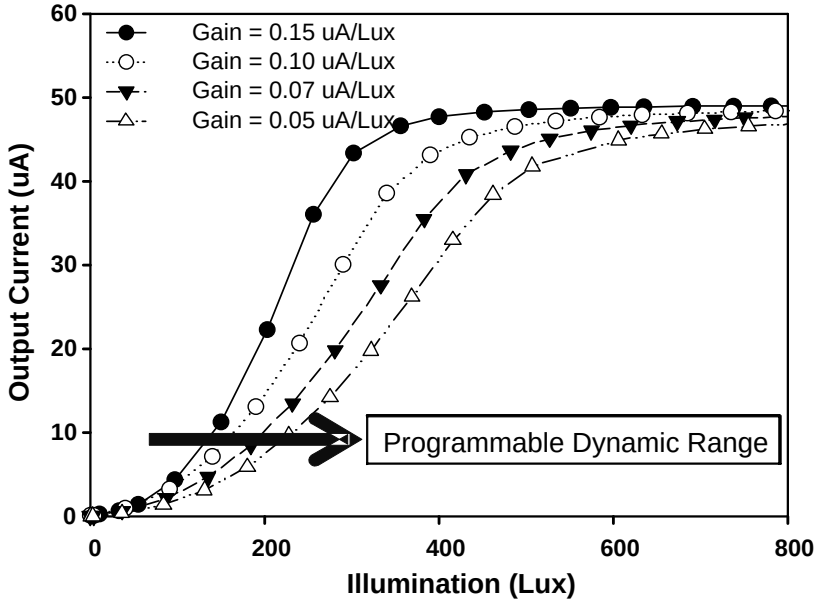


Measurement Result

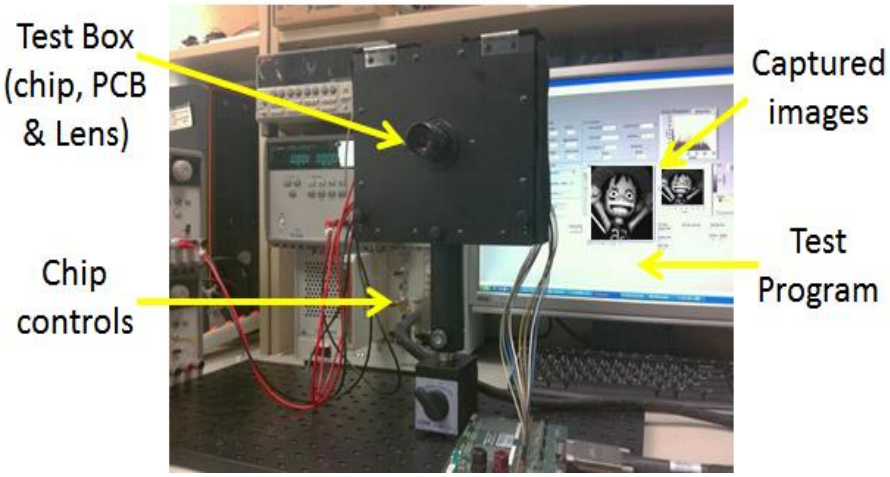
- I_{out} vs. Lux



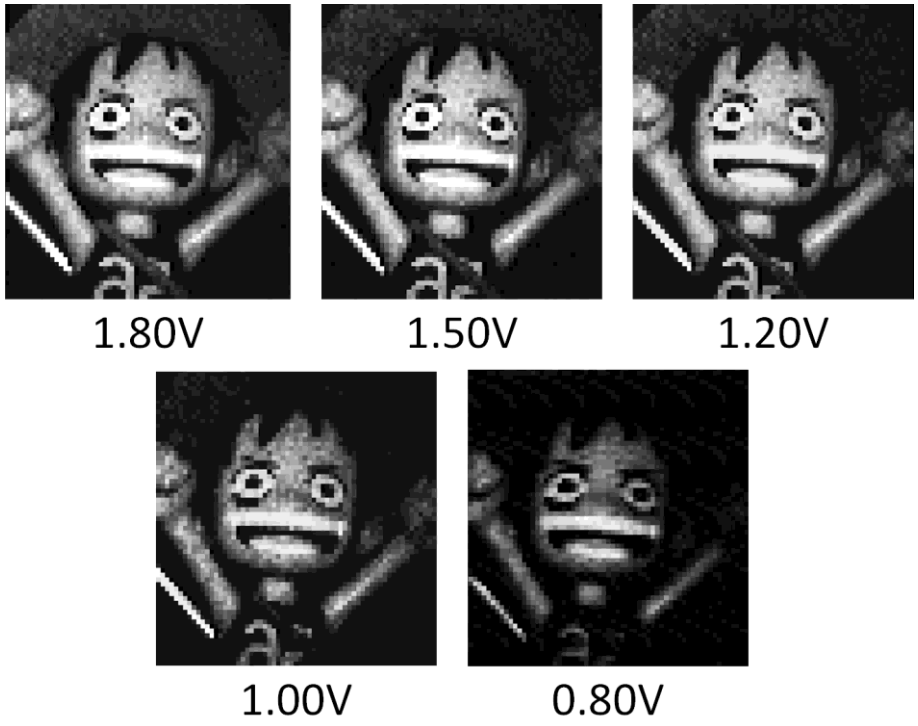
- Adjustable gain



Setup & Captured Images



The Setup for Chip Measurement



The captured image from prototype chip
at supply = 0.8V ~ 1.8V

Chip Specifications

Specifications			
Technology	CIS 0.18-um 1P6M		
Supply voltage	1.8V	0.8V	
Resolution	64x64		
Pixel size	30 × 30 μm^2		
Power consumption (w/o current generator)	IP mode, 300lux		
	14.85mW	0.18mW	
Biphasic conversion gain	0.144 uA/lux	0.021 uA/lux	
Dynamic Range	45.3 dB	27.5 dB	
Max. Biphasic current	(with 10kΩ loading)		
	±50μA	±10μA	
I/O number	Test mode	PG mode	IP mode
	33	14	4

Comparison Table

	[23] Kuafu Chen (JSSC-10)	[24] L.Theogarajan (JSSC-08)	[25]T. Tokuda (Trans.ED-09)	[26] A. Rothermel (JSSC-09)	This [11] (TED-13)
CMOS Technology	0.18-µm	0.5-µm	0.35-µm	0.35-µm	0.18-µm
Chip Size	4.2 x 4.9 mm^2 *	2.3 x 2.3 mm^2	200 x 200 μm^2 (one pixel)	3 x 3.5 mm^2	3 x 3 mm^2
Pixel Count	256	15	41	1600	4096
Power Supply Voltage	±12V, ±1.8V	±2.5V	5V	±2V	0.8-1.8V
Sensor Fill Factor	18.5%	N/A	0.06%	N/A	33.3%
Frame Rate	N/A	440 fps	N/A	10-333 fps	12.5 fps
Data Telemetry	Yes	Yes	No	No	No
DAC Resolution	4 bits	5 bits	5 bits	N/A	N/A
Stimulated Current	±500µA	0-930µA	50-1050µA	>100µA	±50µA @1.8V ±10µA @0.8V

W4: Summary

- A photon-to-biphasic current conversion system
  - High resolution (64x64)
  - Compact (4 I/O for Implanted operation)
  - Low power (180uW @ 0.8V)
- Programming mode
  - Programmable pattern and scanning for electrical stimulus experiment of in vitro retina

W5: Motion Detection Sensor

- Motivation
  - Processing-in-sensor to detect the temporal information
- Key Features
  - Temporal detection
    - Frame-difference operation
  - Intelligent vision
    - Processing-in-sensor
  - Low-power real-time
    - Event report
    - Saliency detection

Problem & Solution

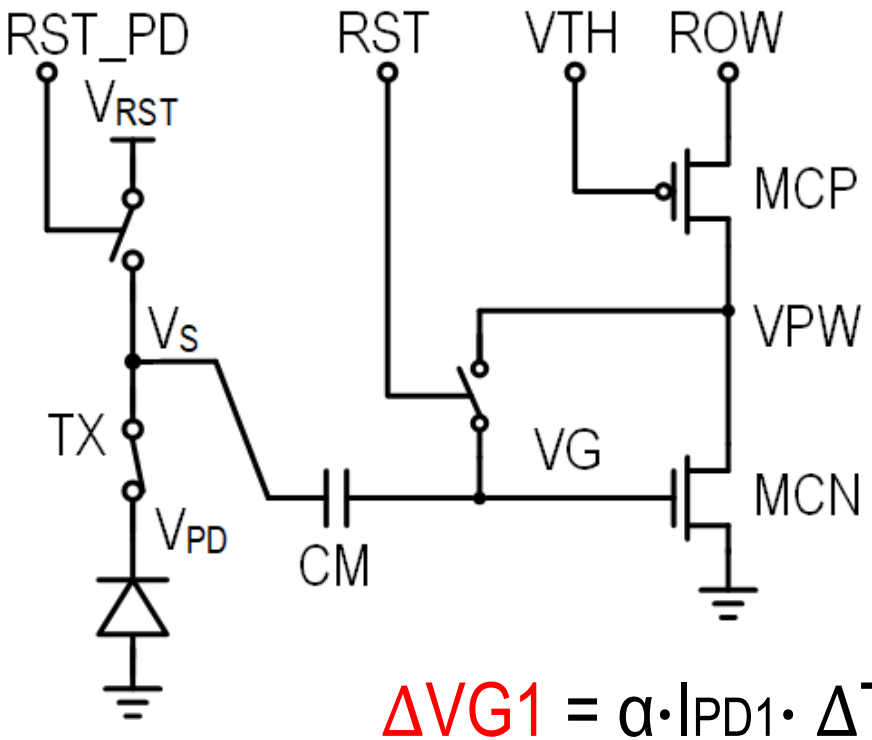
- Low-Power Solution
  - 0.8V operation
  - Multiple-mode supporting (RAW, FD, EVENT, SD)
- Motion detection
  - Frame-difference operation
  - Processing-in-sensor architecture
- Gain mismatch of frame-difference operation
  - Ping-pong PWM pixel

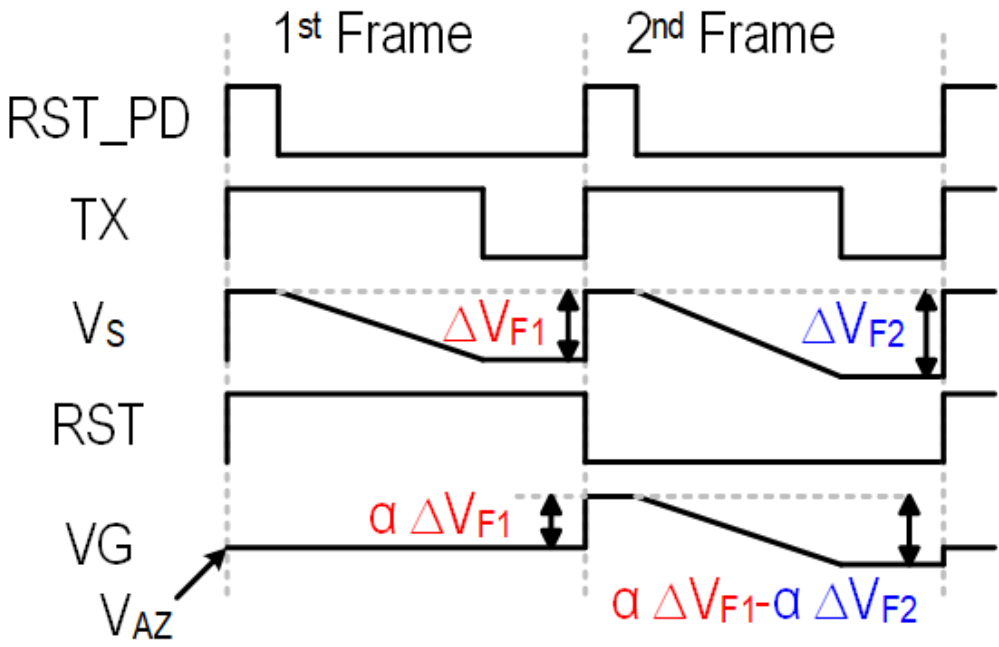
Operation Modes

- Image Capture(IC) Mode:
  - Rolling shutter/Global shutter
  - Column: Row-by-row pulse width counter
  - Output: 8-bit pixel signal
- Frame Difference(FD) Mode:
  - Global shutter
  - Column: Row-by-row pulse width counter
  - Output: 8-bit/2-bit pixel frame difference signal
- Saliency Detection(SD) Mode:
  - Global shutter
  - Column: 8-row current integrator + SS-ADC
  - Output: 8-row ON/OFF event count

Conventional Gain-Mismatch Issue

- Two frame signal sent to node VG with different transfer function, and all nodes reset for next differencing signal

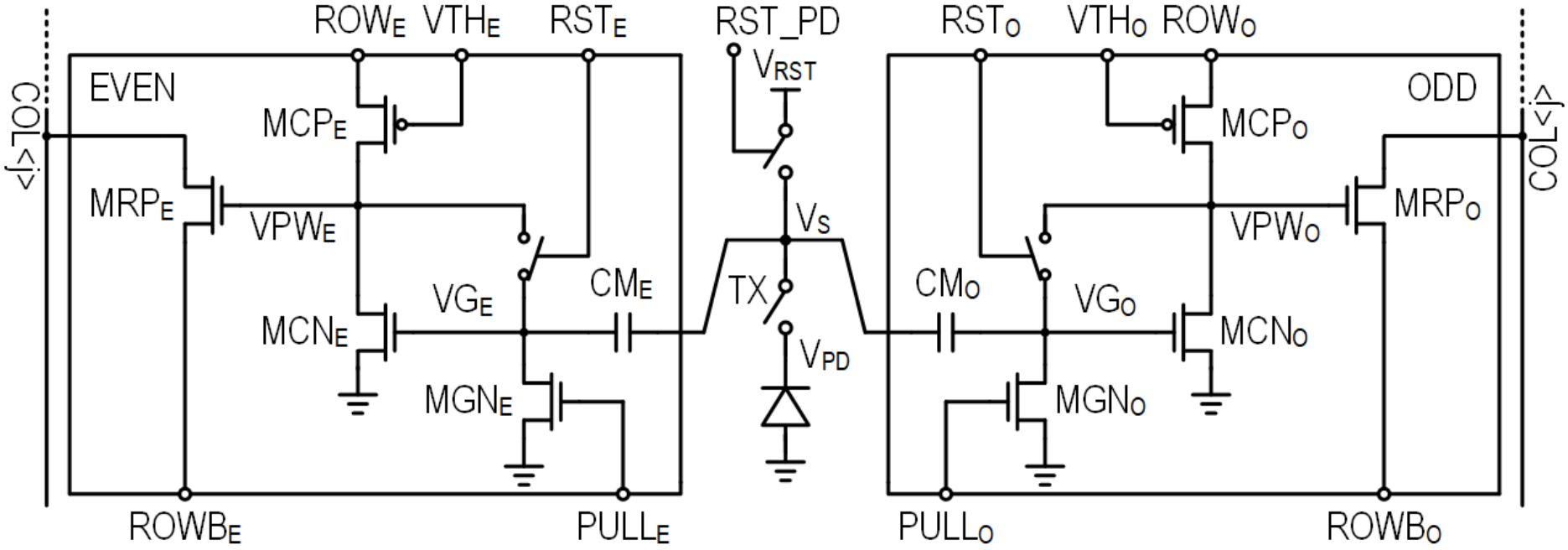




$$\Delta VG1 = \alpha \cdot I_{PD1} \cdot \Delta T/(C_{PD}+C_M)$$

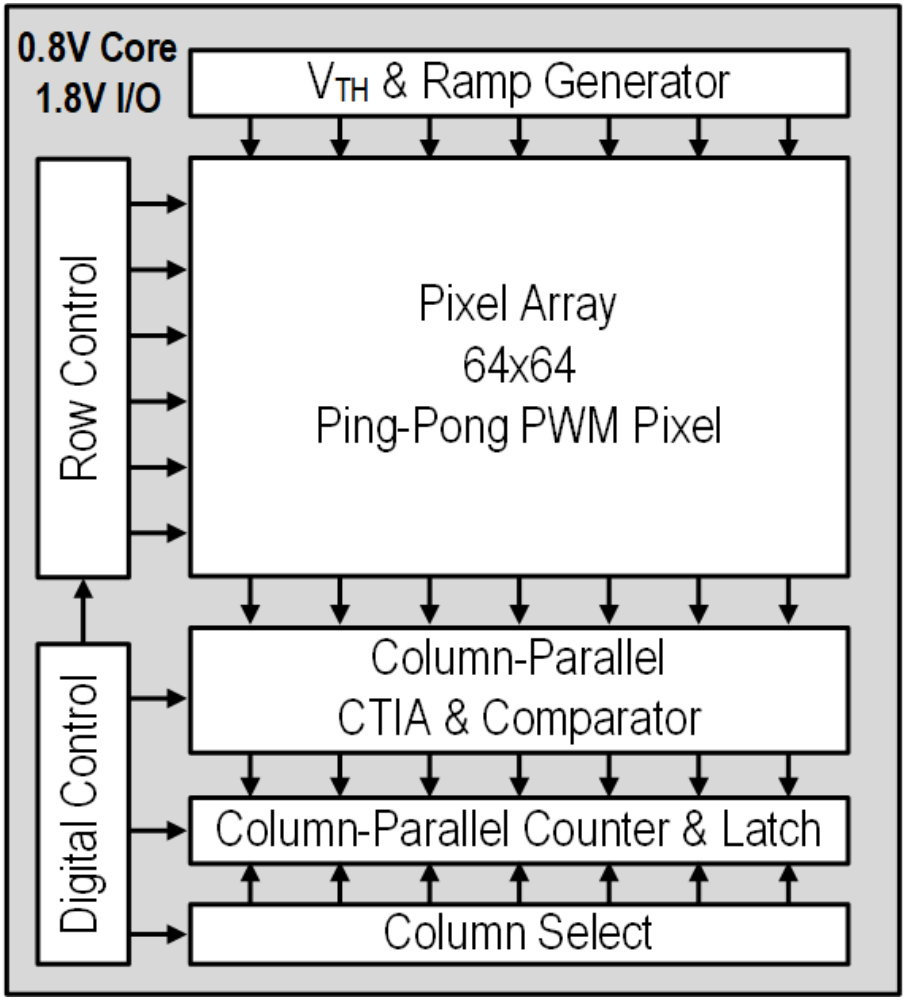
$$\Delta VG2 = \alpha \cdot I_{PD2} \cdot \Delta T/(C_{PD}+C_M \cdot C_{PAR}/(C_M+C_{PAR}))$$

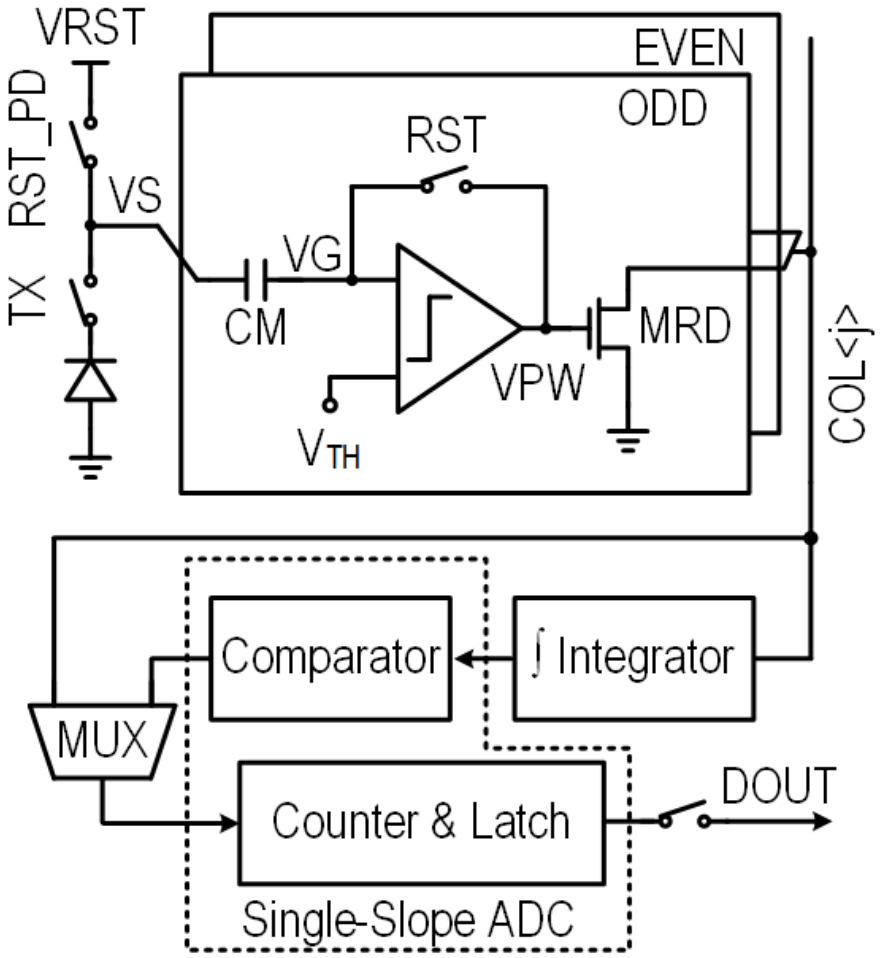
Proposed Ping-Pong PWM Pixel



- Ping-pong operation FD PWM(ODD & EVEN)
- $MCN_{O/E}$ offer fixed voltage level(GND) to $VG_{O/E}$

Chip Architecture

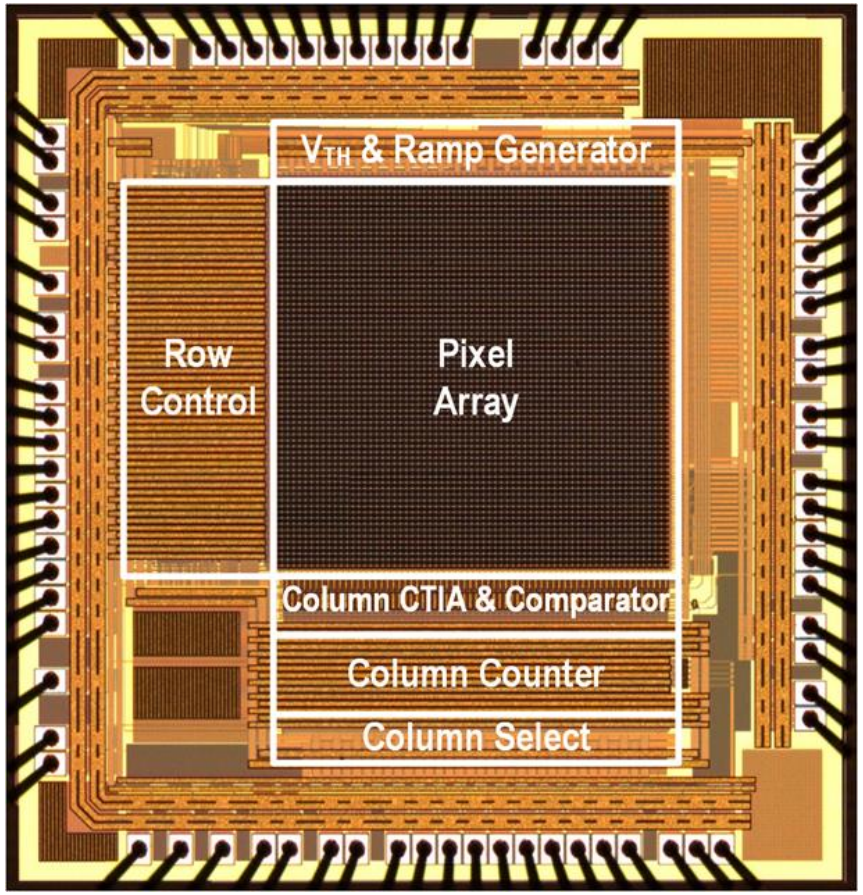




Chip Micrograph

- TSMC 0.18µm 1P6M standard technology
- Pixel pitch: 15µm
- Pixel array: 64×64
- Chip size:

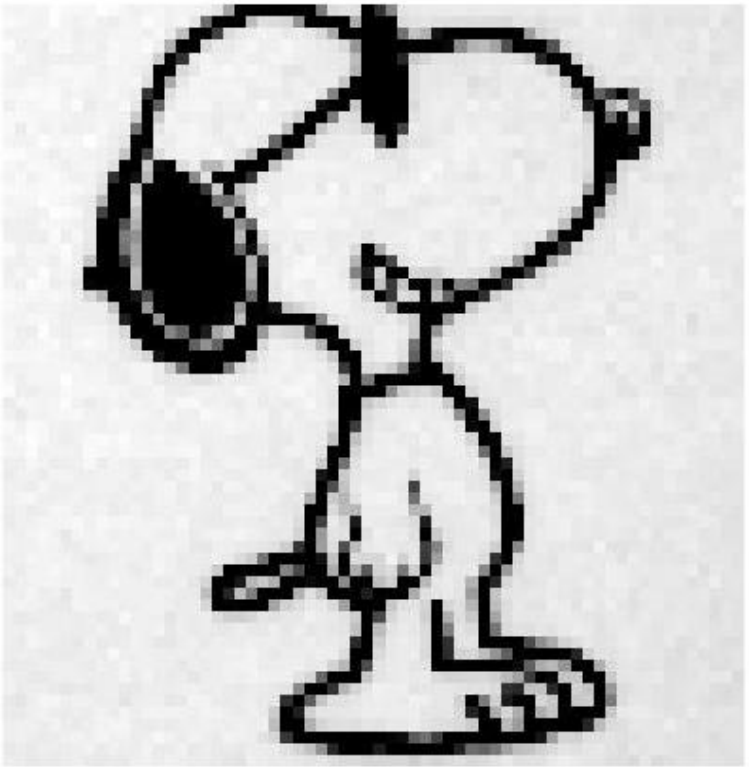
  2.0mm×2.1mm



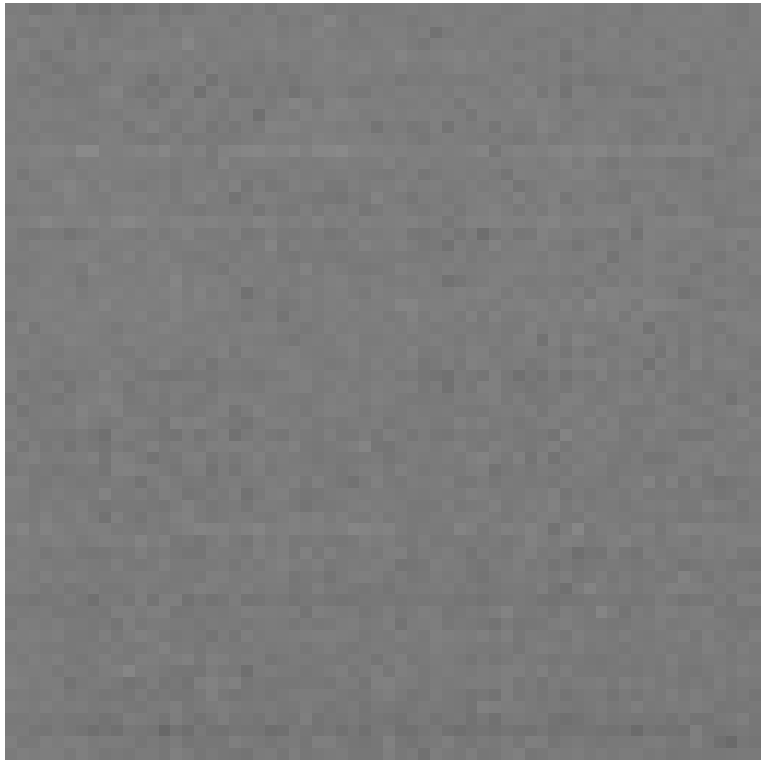
FD Multibit Mode

- FD mode capture frame rate: 510fps

Sliding

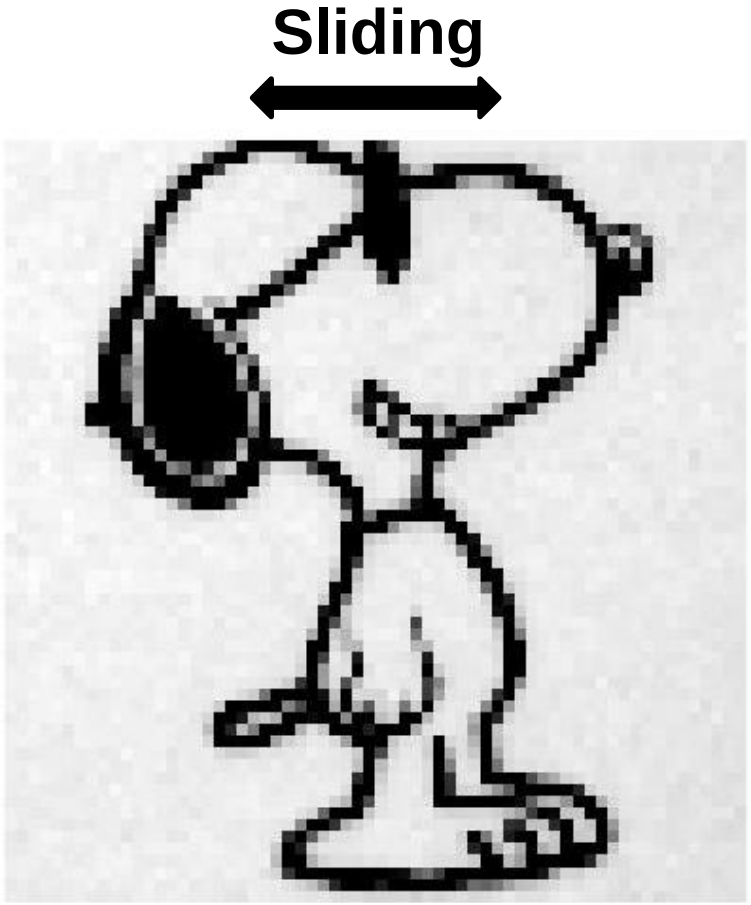


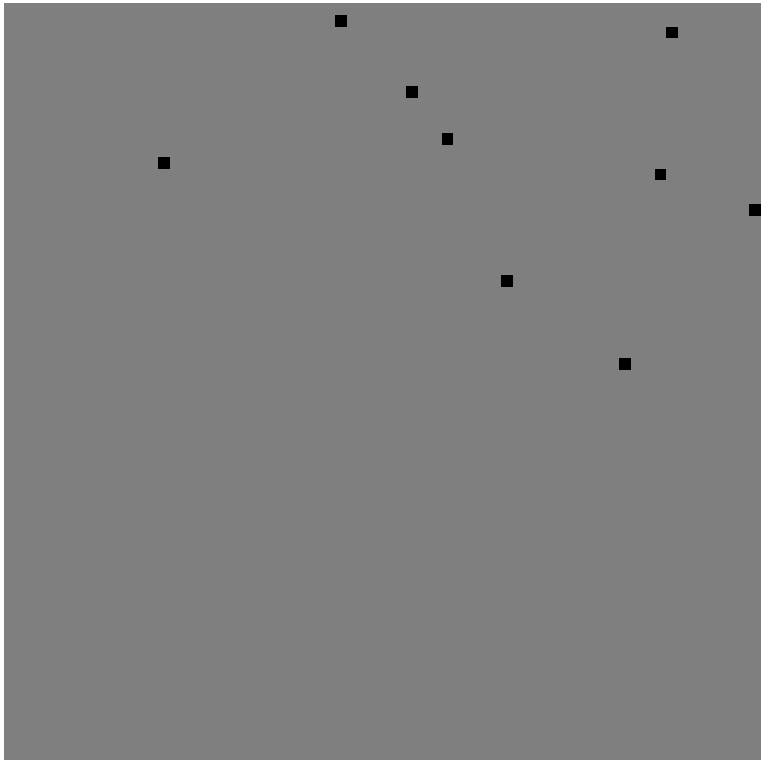
10fps



2-bit Event Mode

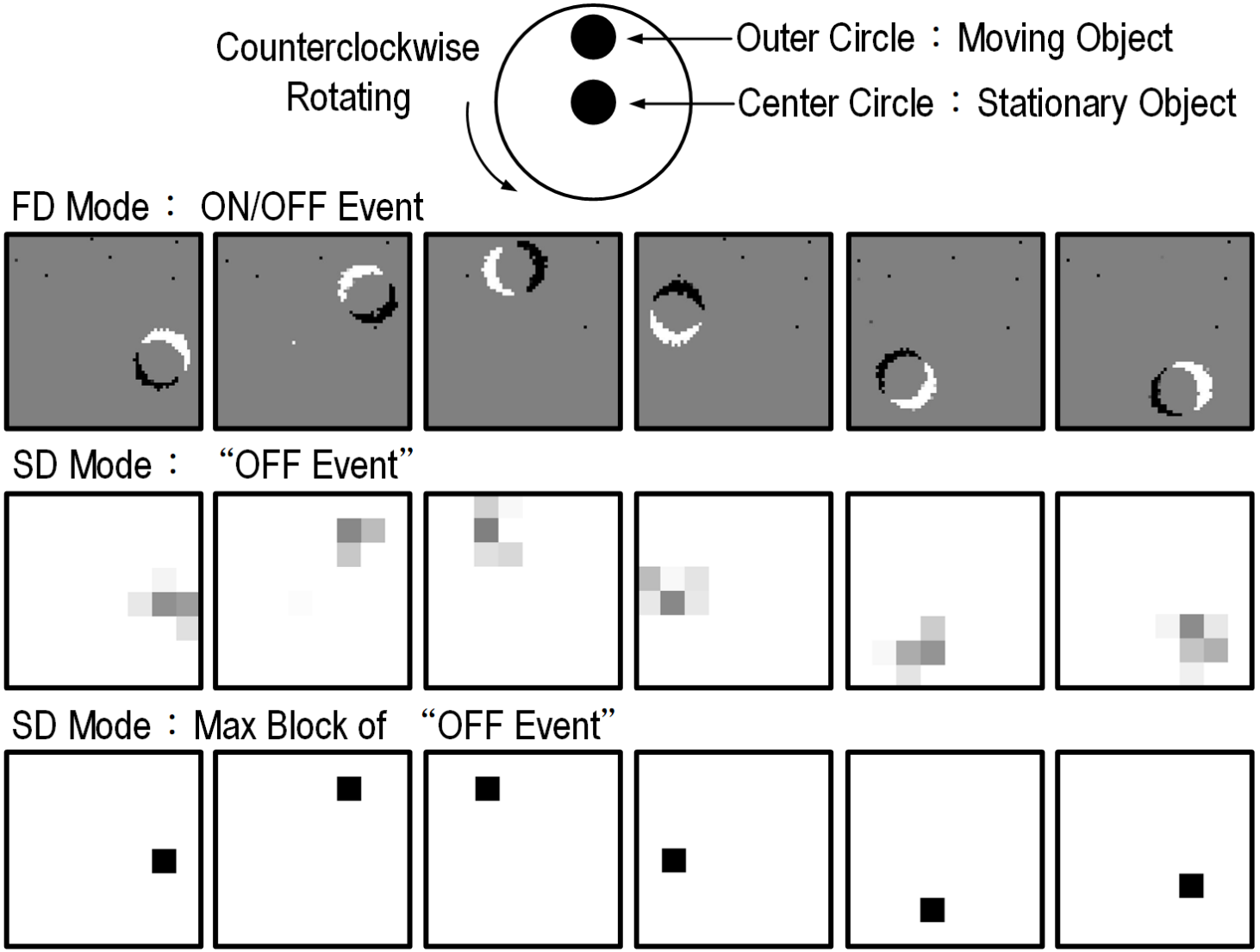
- Event mode capture frame rate: 510fps





95

Saliency Detection Mode



W5: Summary

- Ping-pong PWM pixel circuit realizing full-rate frame difference operation
- 8×8 sub-block level saliency detection implementation
- Multi-mode operation with high speed and low power consumption
  - IC mode: 71.2μW @ 360fps
  - FD mode: 74.4μW @ 510fps (64×64)
  - SD mode: 121.6μW @ 890fps (8×8)

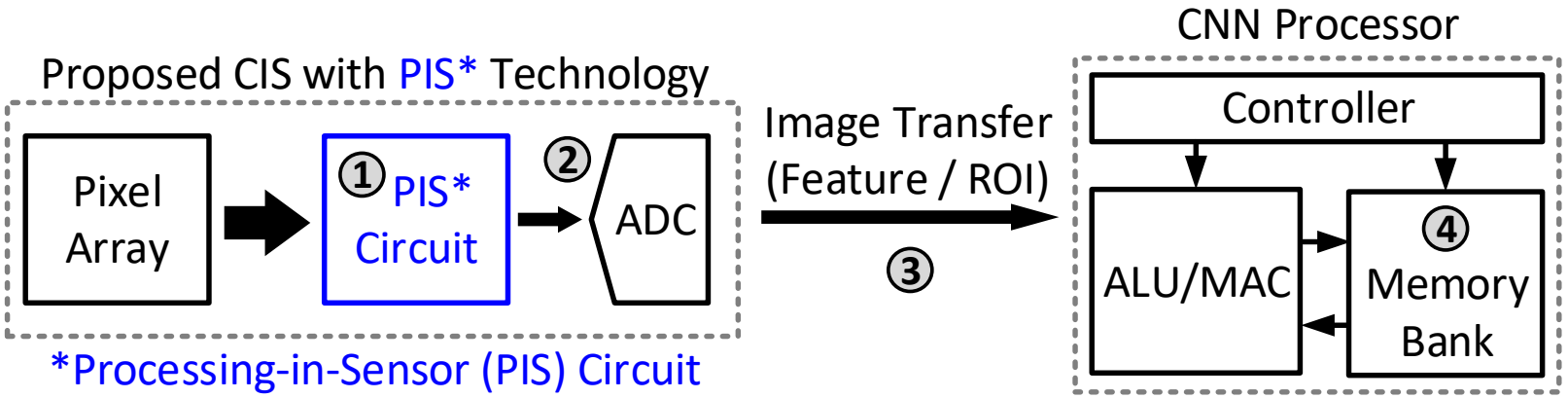
W6: Intelligent Vision Sensor with AI

- *Motivation*

- *Conventional CIS*
  - Shrink pixel size
  - Improve noise figure
  - Limited to human eyes
- *Intelligent CIS*
  - Spatial / temporal feature extraction
  - Object recognition / tracking
  - More possibility

Processing-in-Sensor

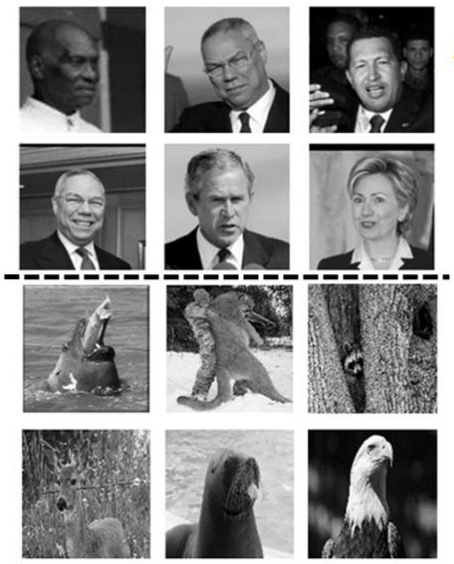
- CIS with PIS technique
  - PIS circuit for feature extraction
  - Transfer ROI / feature only
- Advantages
  - Keep meaningful information
  - Reduce ADC requirement
  - Relieve computing load
  - Relieve memory capacity



Better power, latency, bandwidth efficiency for AIoT Application ☺

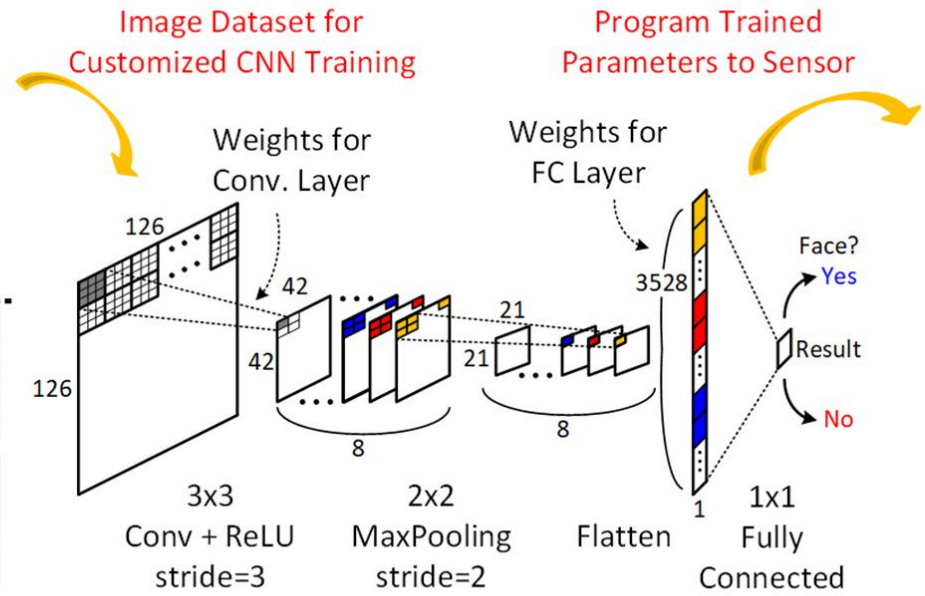
CIS + PIS + AI = Intelligent Vision

Image Dataset for Target Application

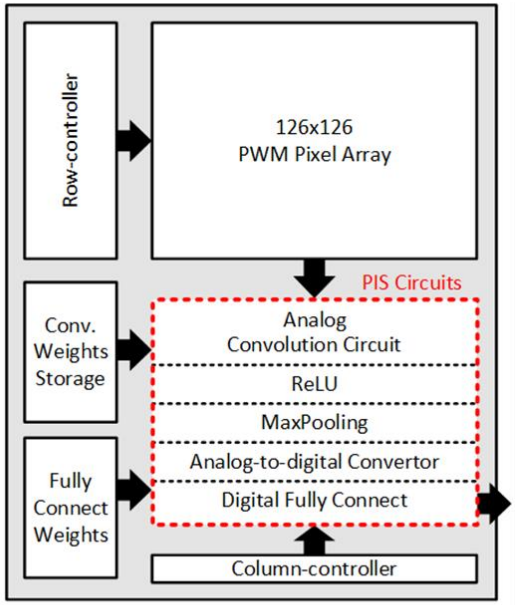


Ex. Human face or not

Customized CNN Model

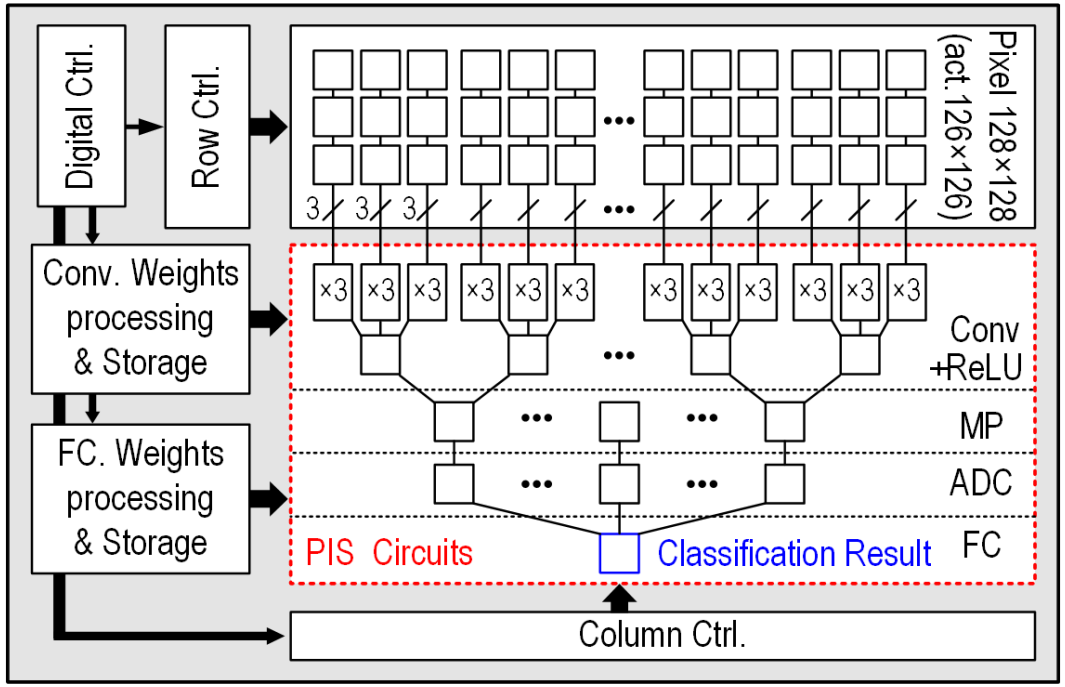


PIS-based CMOS Image Sensor

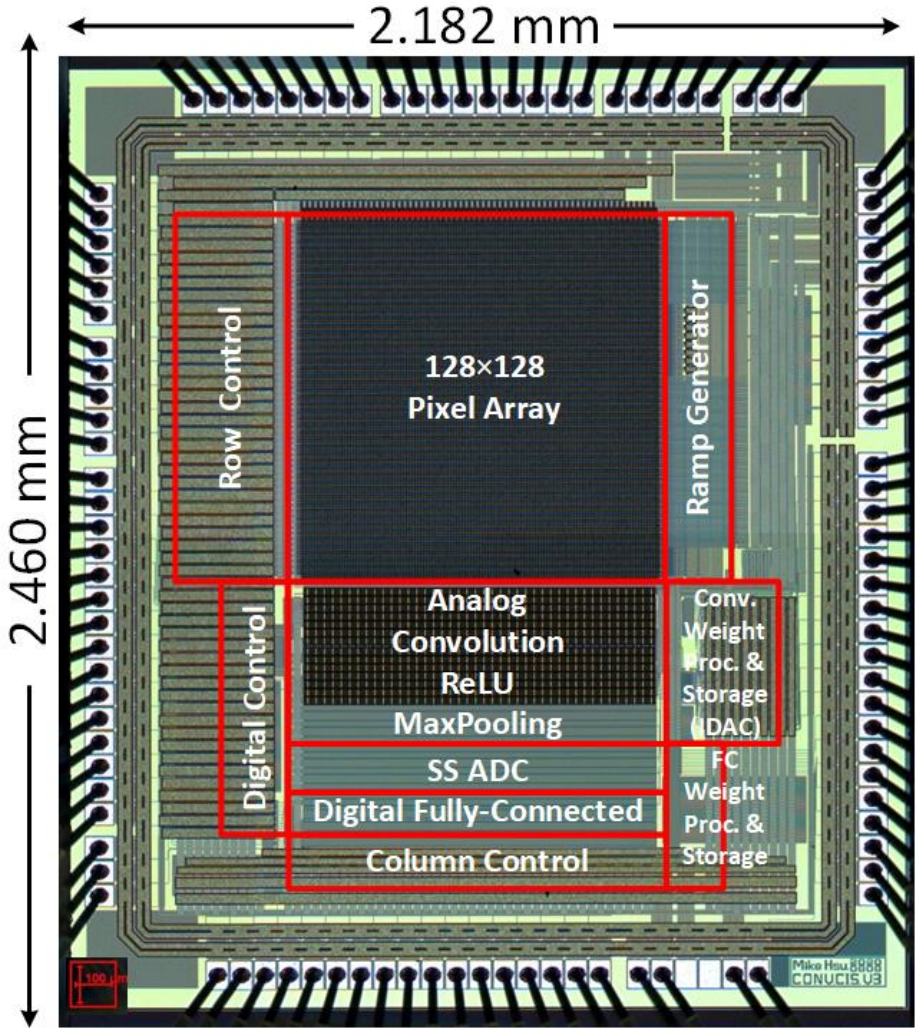


Chip Architecture

- 126x126 array
  - PWM Pixel
- PIS circuits
  - Convolution + ReLU
  - MaxPooling (MP)
  - ADC
  - Fully-connected (FC)
- Peripheral
  - Row/column control
  - Conv. weight storage
  - FC weight storage

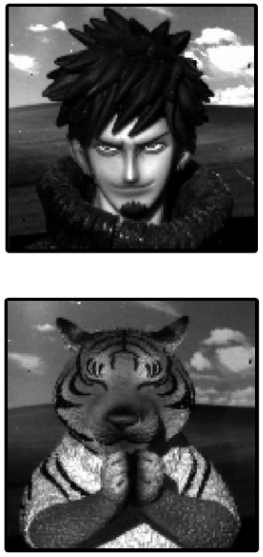


Chip Photo

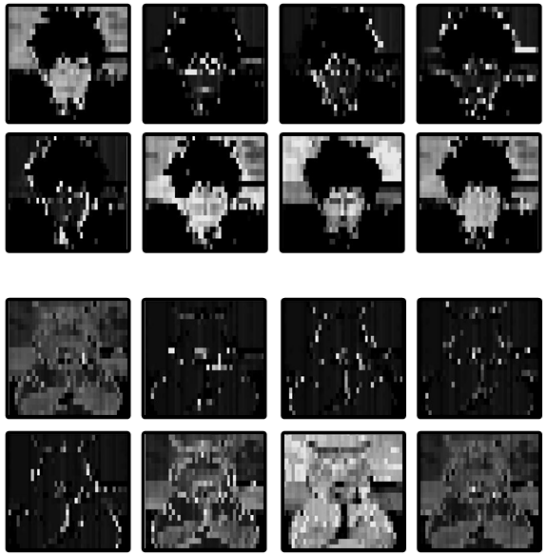

2.182 mm
2.460 mm
Row Control
128×128
Pixel Array
Ramp Generator
Digital Control
Analog
Convolution
ReLU
MaxPooling
SS ADC
Digital Fully-Connected
Column Control
Conv.
Weight
Proc. &
Storage
(DAC)
FC
Weight
Proc. &
Storage

Face-Detection Measurement

Raw Image
126×126

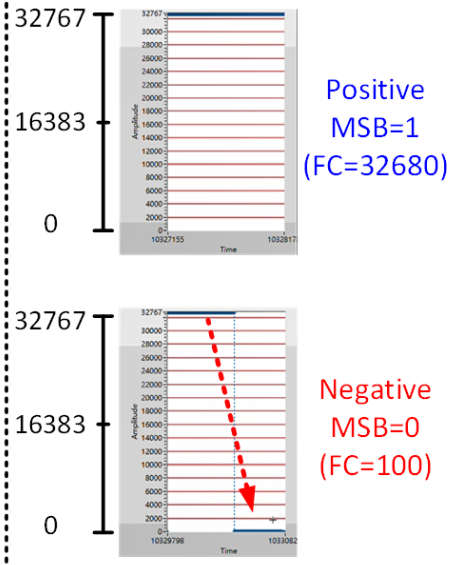


Feature Maps
21×21×8



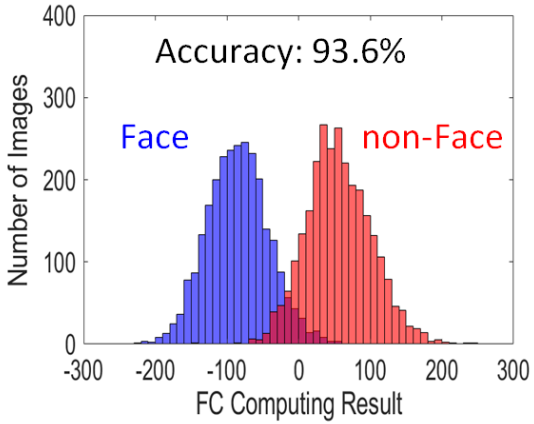
Detection Result

Global counter output

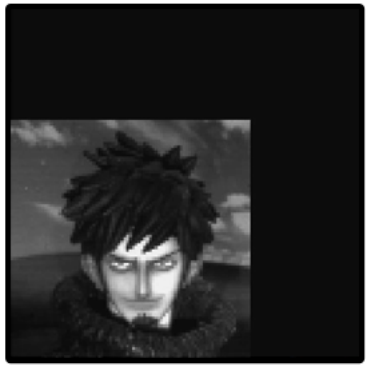
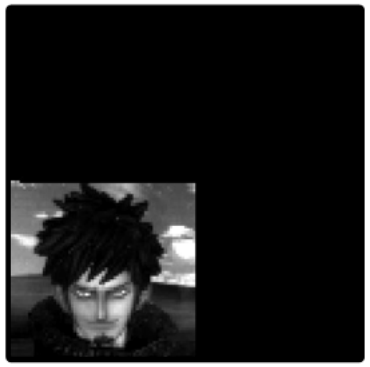


Statistical Results

Face Image: 2670
Non-Face Image: 2791



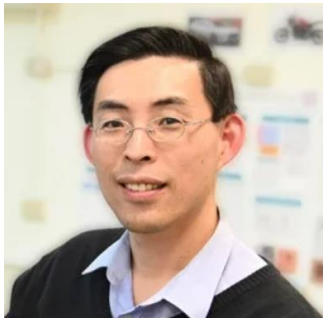
Face Detection with Different Size

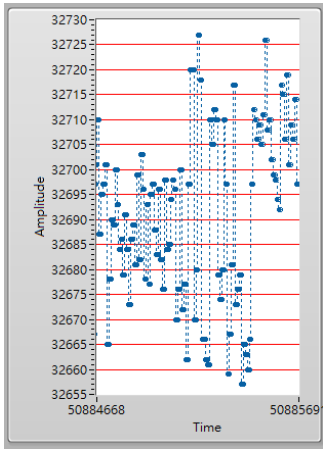
Captured Multiple-scale Image			
Detection Window	126×126	84×84	66×66
Number of FC Parameters	3528	1568	968
Meas. Accuracy (%)	93.6	91.6	90.1
Max. Frame Rate (fps)	250	535	867
Power (μW)	134.5	100.6	88.5
FoM (pJ/pix·frame)	33.8	26.6	23.4

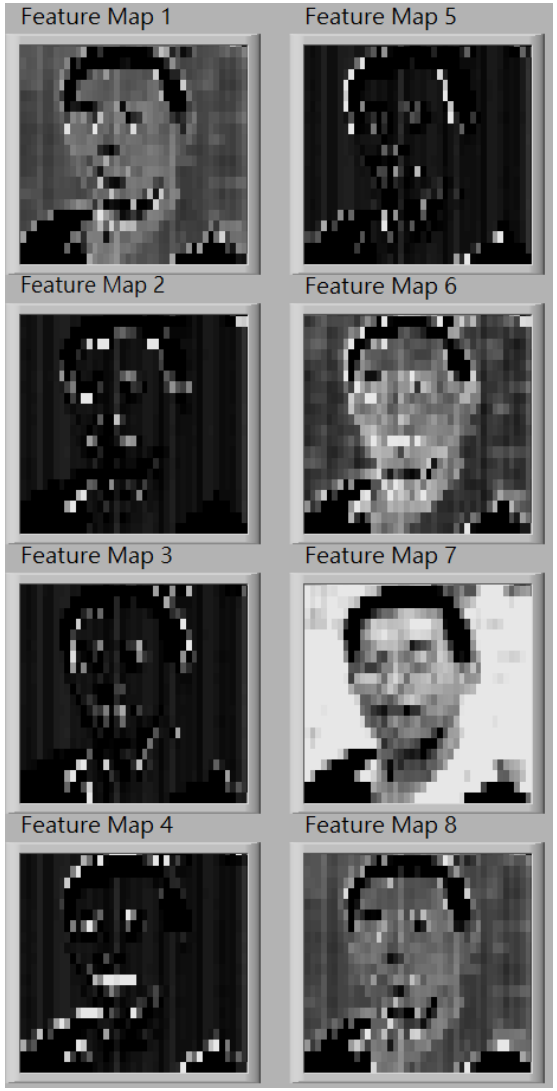
Reduced FC weighting

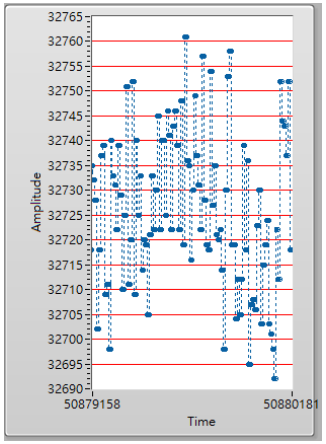
Keep accuracy > 90%

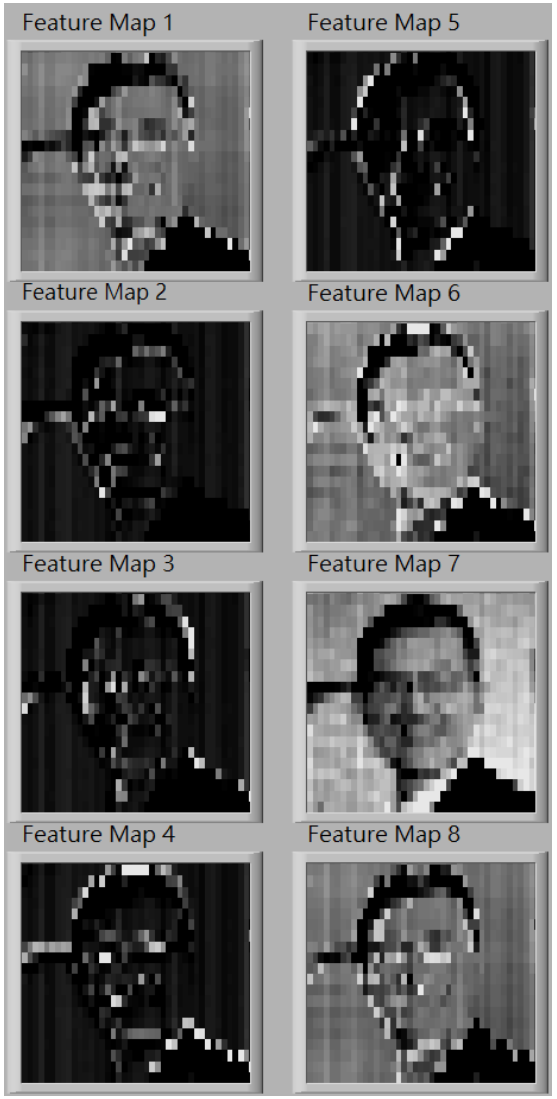
Successful FD





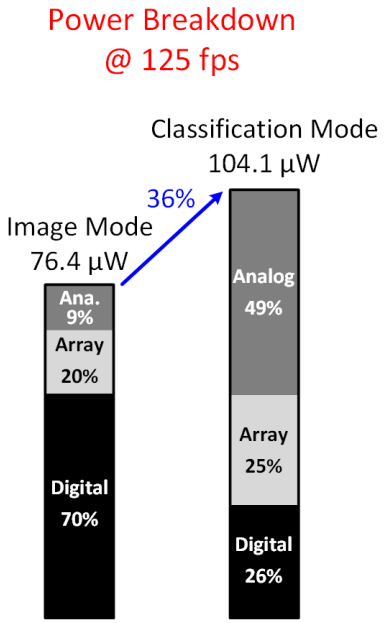






W6: Summary

- The 1st single 0.8V-operated intelligent vision sensor with PIS circuit for CNN model
  - Mixed-mode PIS circuits: 3×3 Conv. with ReLU, 2×2 MP and 1×1 FC
- Demonstrate a “human face detection” task
  - Achieve an accuracy above 90%
  - 2× frame rate, 12% of power and 14× better iFoM
- Low-power high-accuracy FD
  - 134.5µW @ 250fps



Conclusion

- CMOS Image Sensor Keeps to Dominate the Imaging Market
- New Market Share
  - Surveillance
  - Automotive
  - Compact camera
  - AR/VR
- New CIS Applications
  - Biomedical : X-ray, Multi-spectral, DNA Sequencing..
  - Industrial, Scientific, Computational Imaging, HID..
  - Intelligent Vision (CIS+AI)