CHAPTER 2

Device Modeling

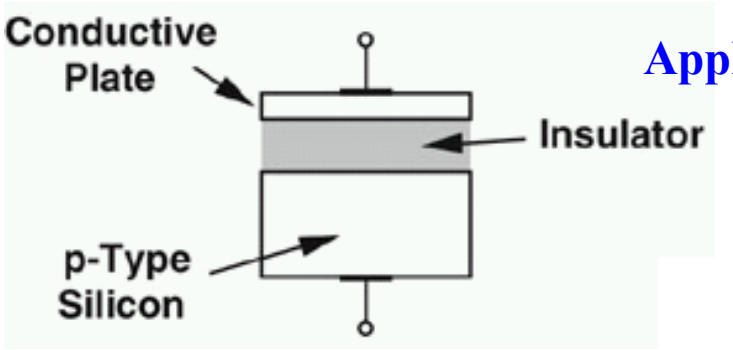
Acknowledgment

感謝 鄭桂忠老師 熱情贊助投影片!!

Syllabus

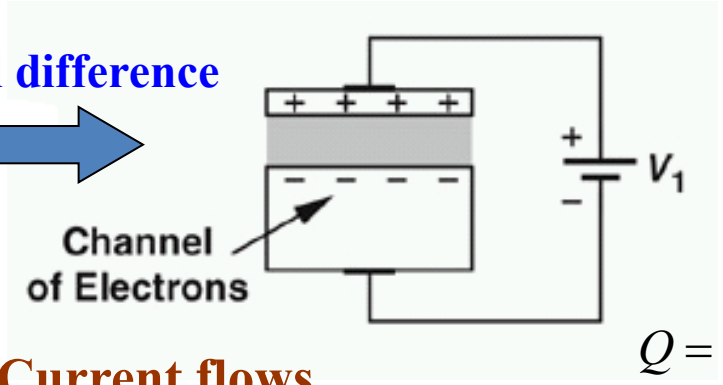
- Basic physics of MOS transistors and their equivalent circuit models (ch. 6)
- Elementary gain stages (ch. 7, ch. 9, and ch. 10)
- Operational amplifier basics (ch. 8)
- Frequency responses (ch. 11)
- Noise (ch.7, Design of analog CMOS ICs)
- Feedback, stability and compensation (ch. 12)
- Operational amplifiers (ch.9, Design of analog CMOS ICs)

Metal-Oxide-Semiconductor (MOS)



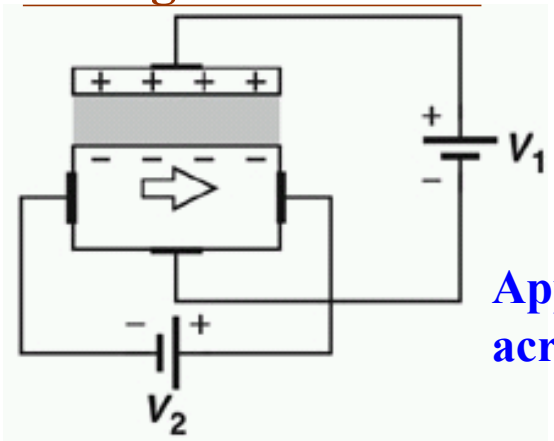
Apply a potential difference

A channel is formed



$Q = CV_1$

Current flows through the channel



Apply a voltage across the silicon

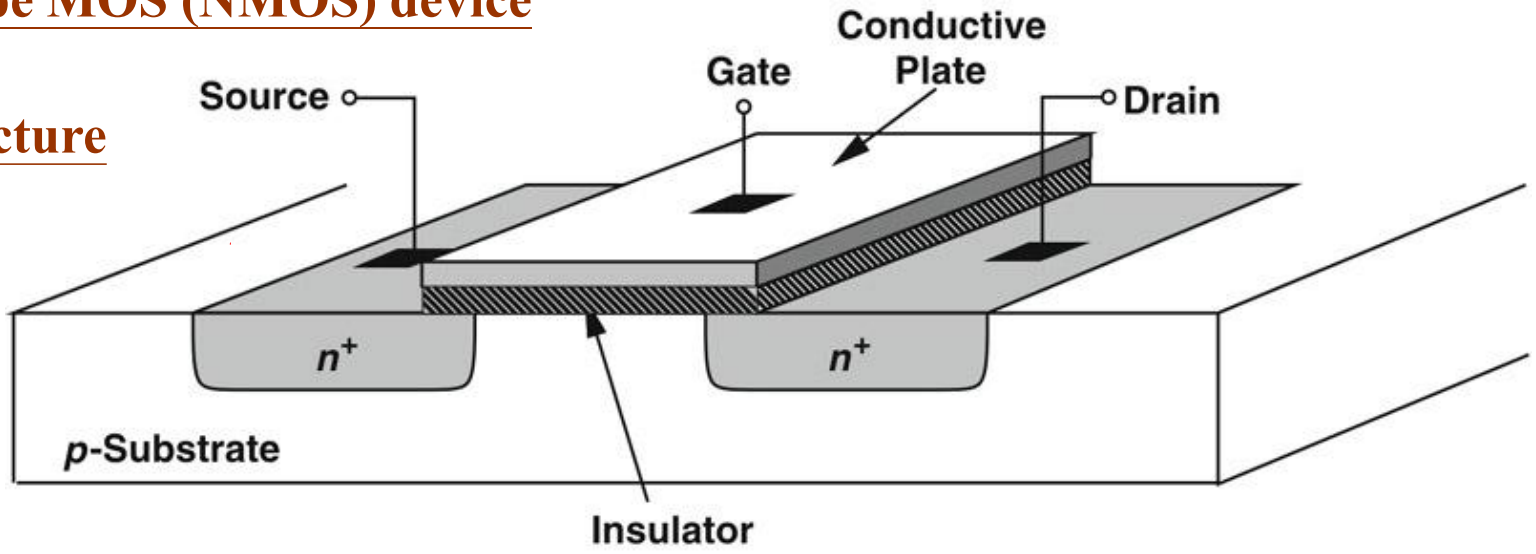
- V_1 controls the current by adjusting the resistivity of the channel
- Reducing the thickness of the dielectric layer for a strong control of Q (20A today)

A voltage-controlled current source

Structure and Symbol of MOSFET

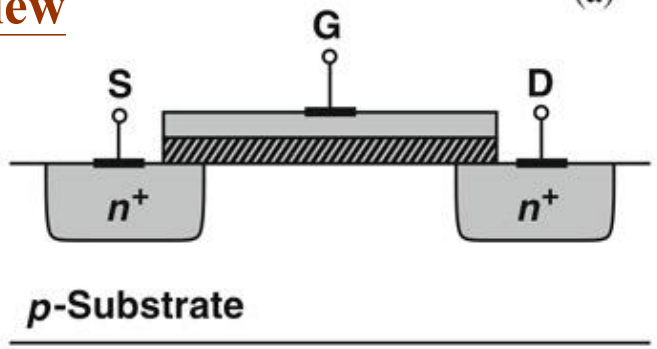
***n*-type MOS (NMOS) device**

Structure



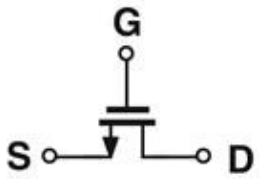
(a)

Side view



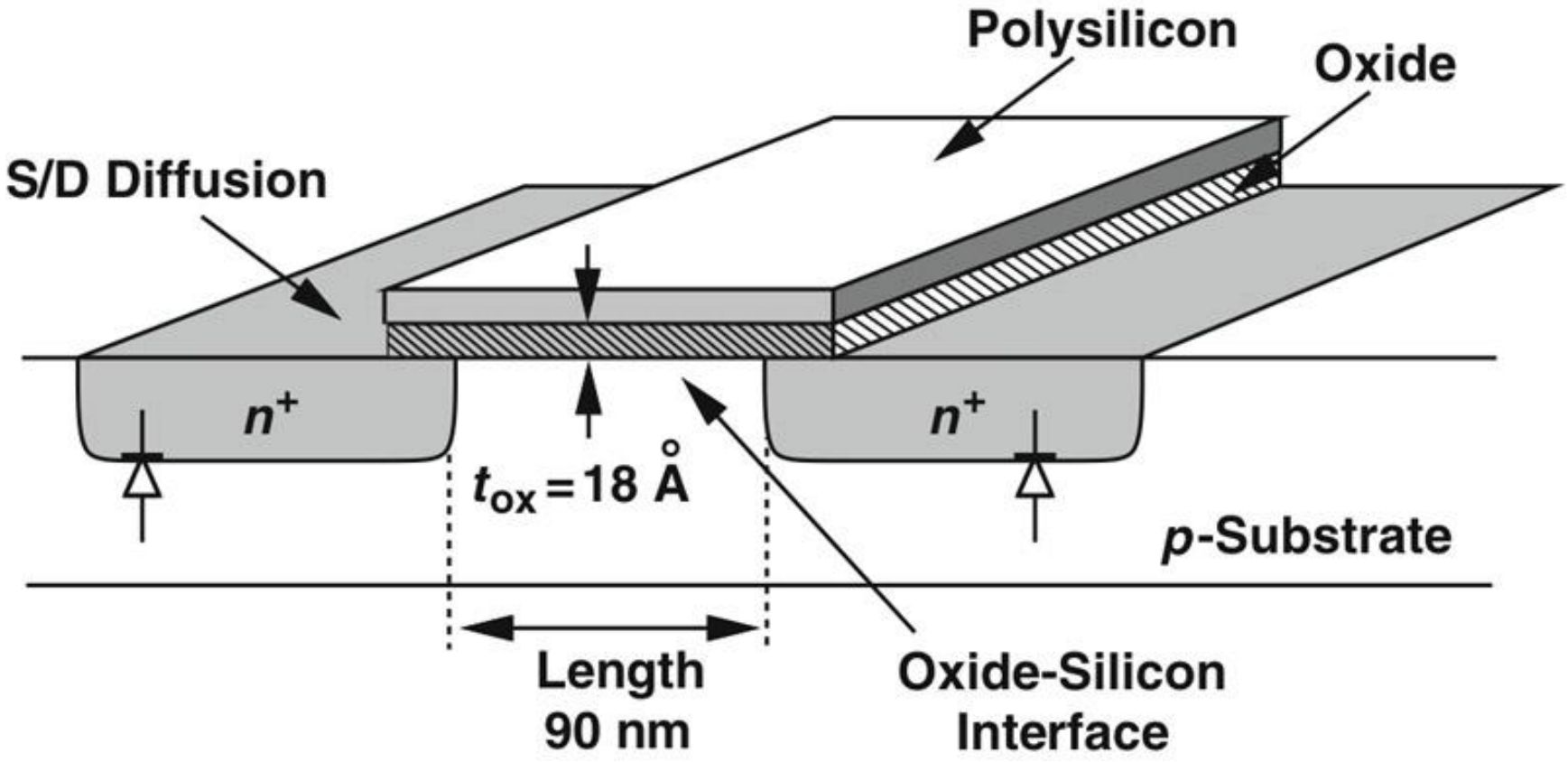
(b)

Symbol



(c)

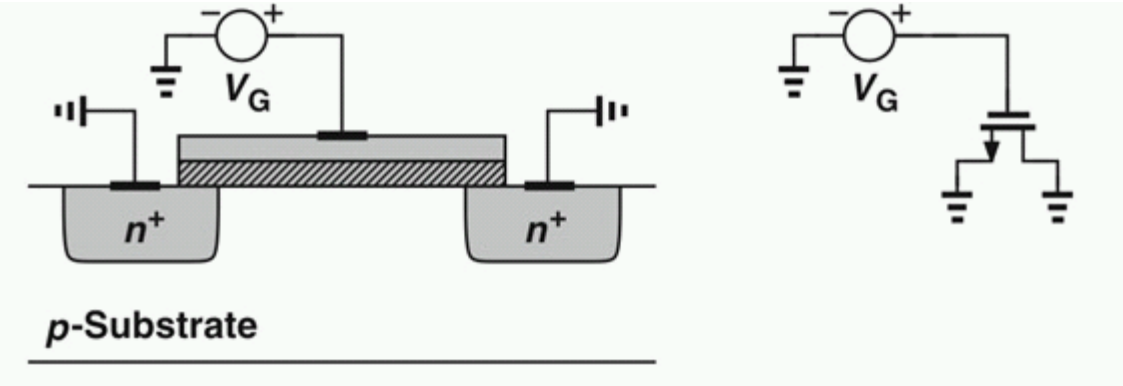
Typical Dimension of MOSFET



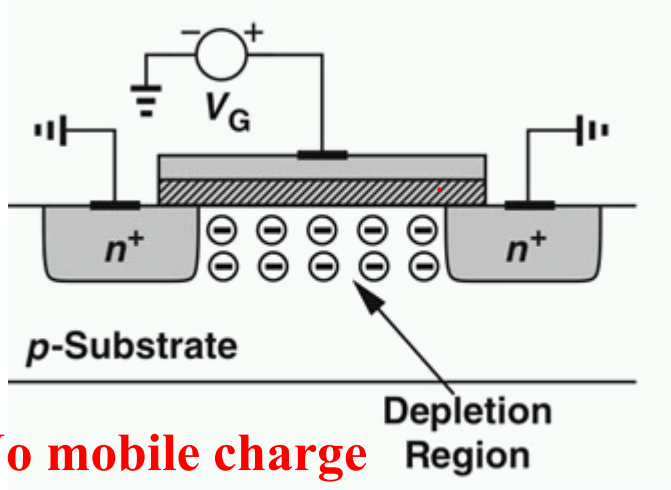
- The gate is formed by polysilicon, and the insulator by Silicon dioxide.

Operation of MOSFET

Formation of channel

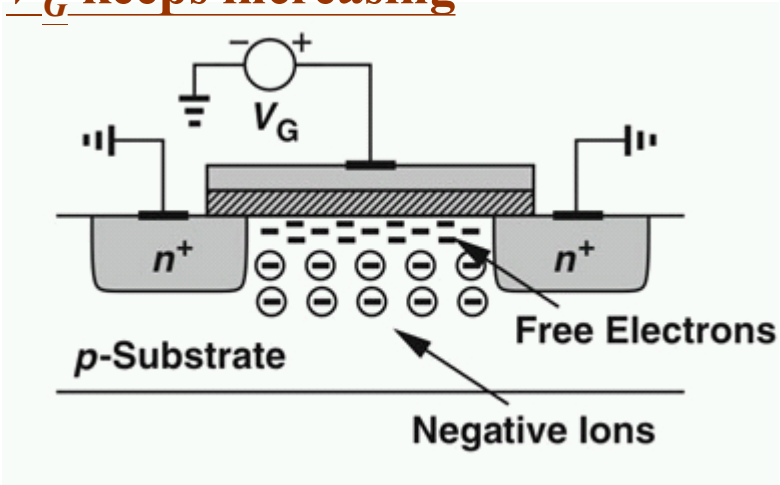


V_G increases from zero



No mobile charge – no current!! MOSFET is off

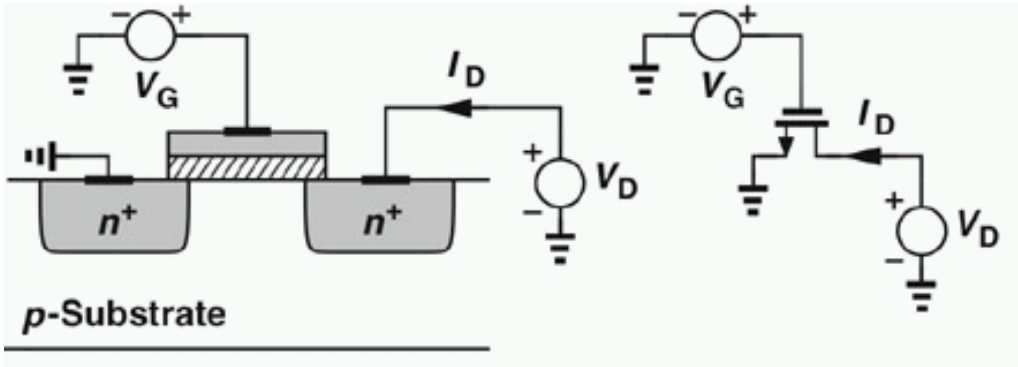
V_G keeps increasing



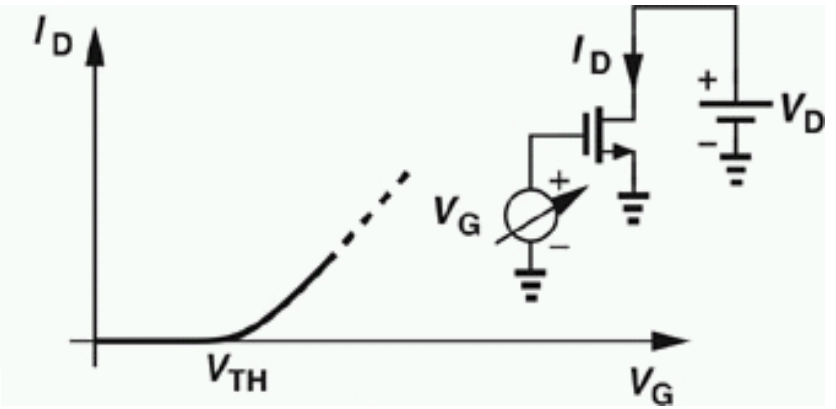
MOSFET is on!!

MOSFET Characteristics

Varying V_G or V_D while keeping the other one

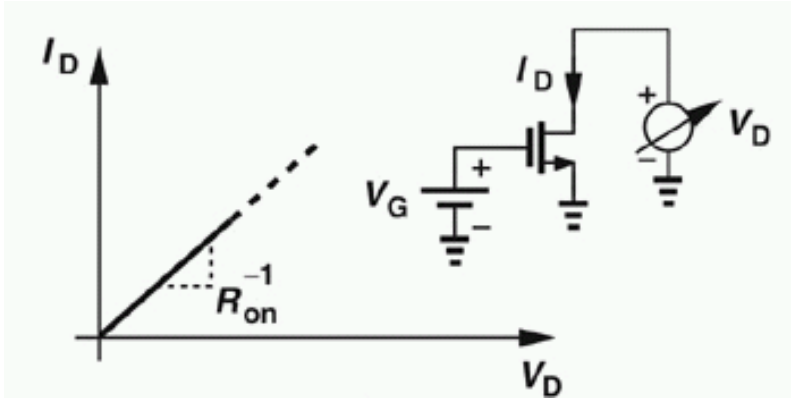


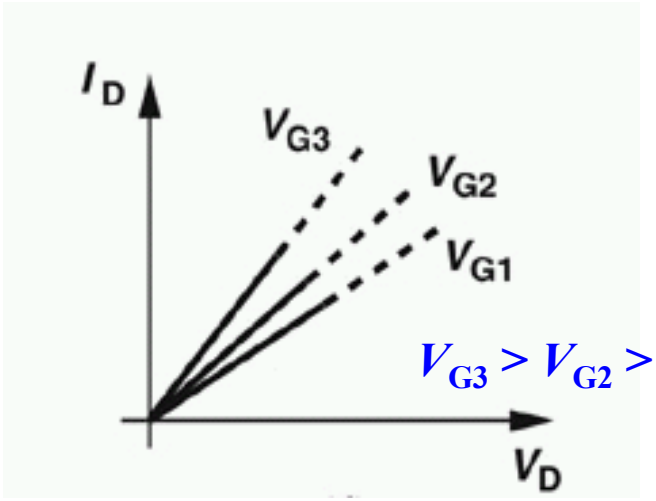
Varying V_G



Varying V_D

R_{on}: on-resistance
- Between source and drain

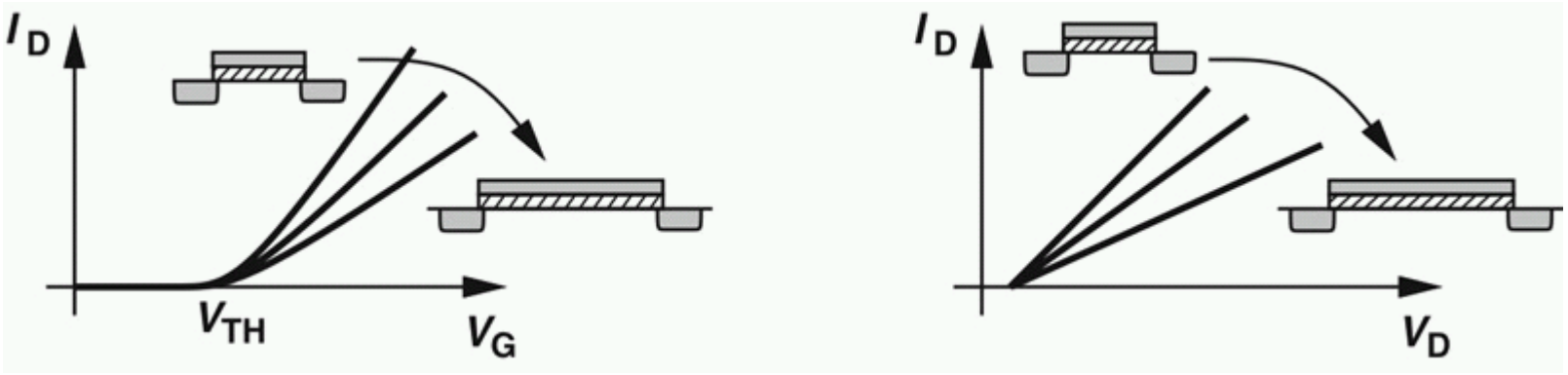




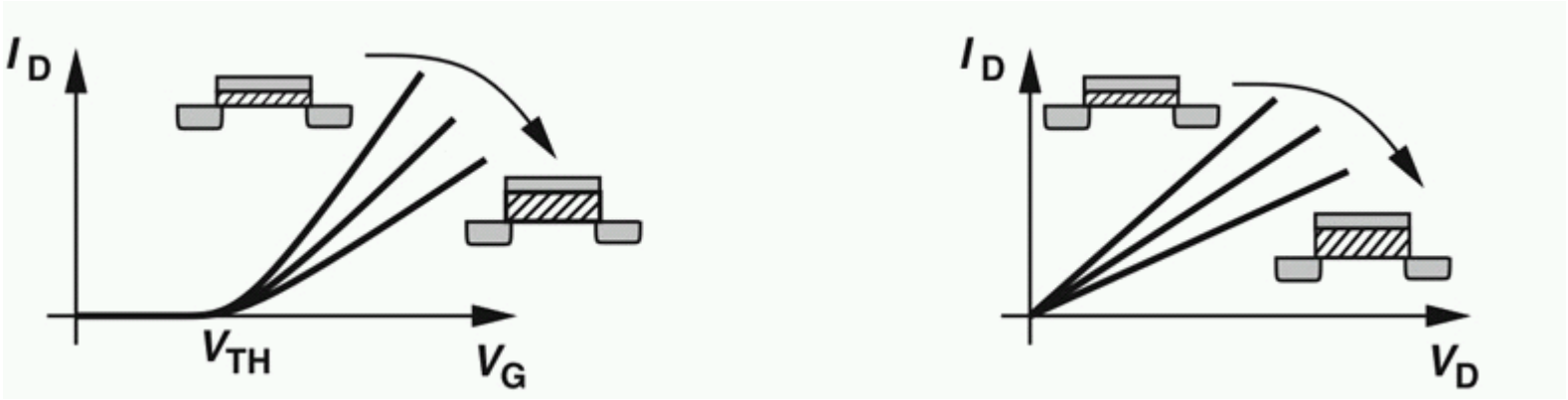
Current flows through drift or diffusion?

Dependence on L and t_{ox}

(a) Different channel lengths

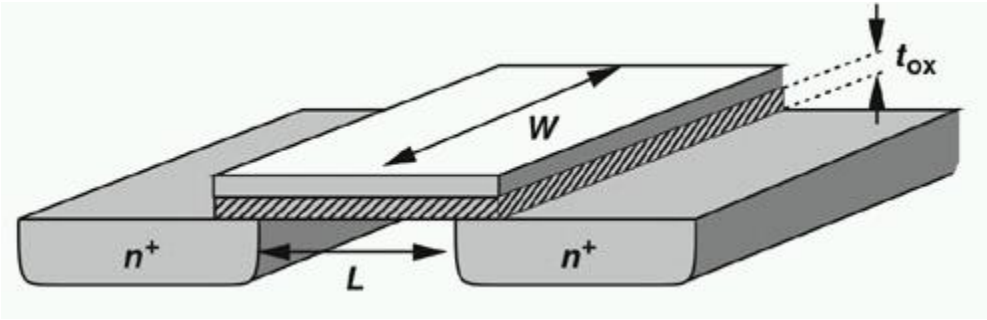


(b) Different oxide thickness

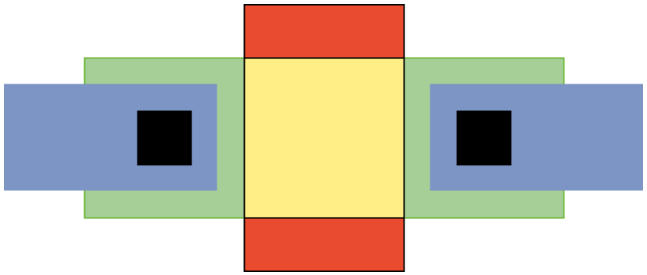


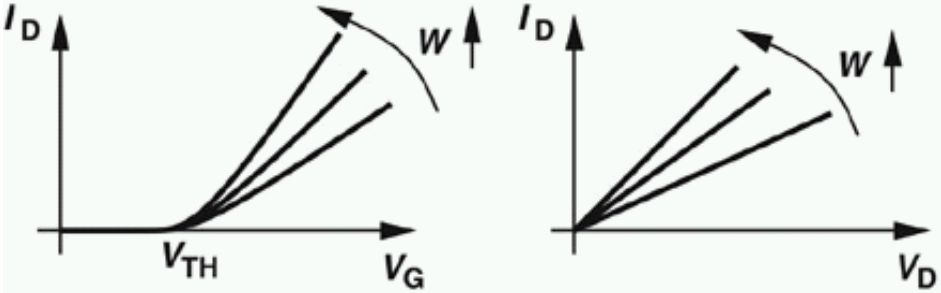
Dependence on Channel Width (*W*)

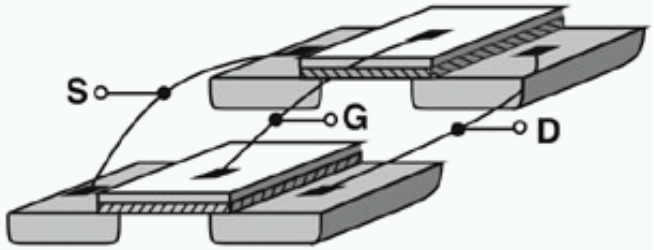
MOSFET structure



MOSFET circuit layout







Width (*W*) and length (*L*) can be controlled by designer, while t_{ox} cannot

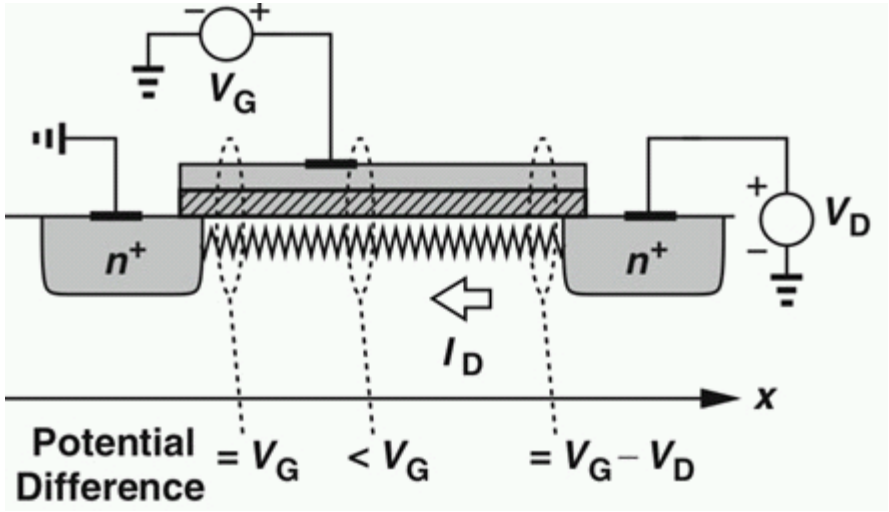
So, MOSEFT is a voltage-dependent resistor?

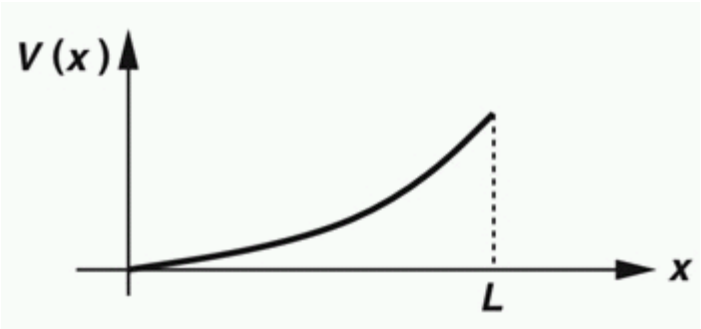
Channel Potential Variation

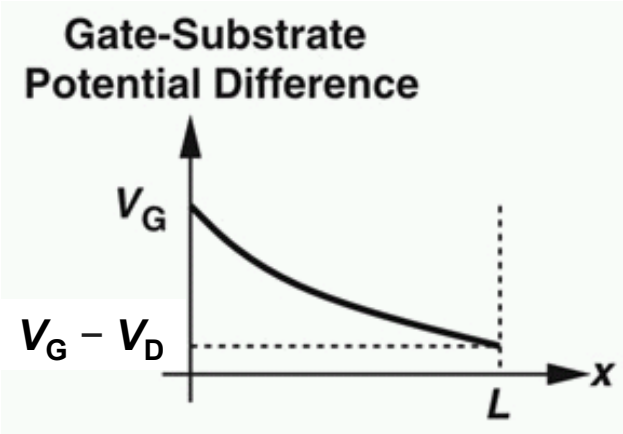
MOSFET transistor is actually a current source if V_D sufficiently positive

Two observations:

- To form a channel, the potential difference between the gate and the oxide-silicon interface must exceed V_{TH}.
- If the drain voltage remains higher than the source voltage, then the voltage at each point along the channel with respect to ground increases as we go from the source towards the drain

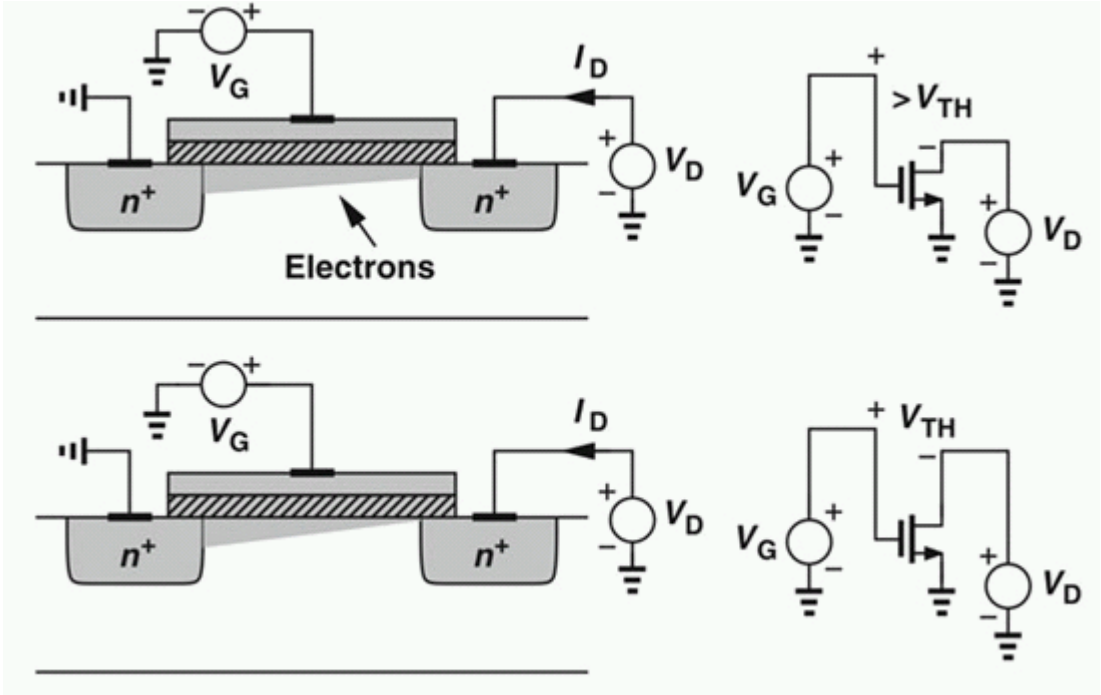






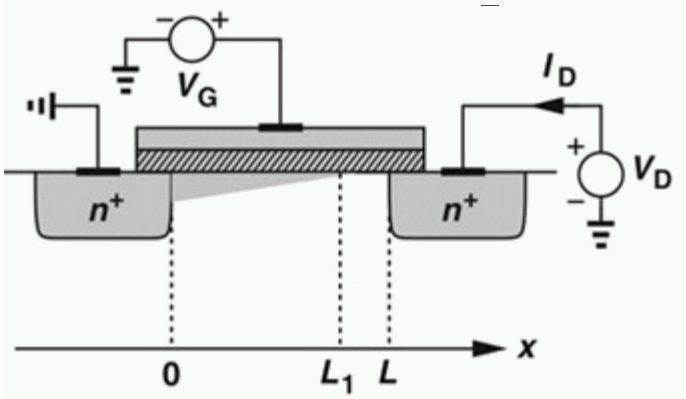
Channel Pinch-off

If the drain voltage is high enough to produce $V_G - V_D \le V_{TH}$, then the channel ceases to exist near the drain: channel is pinched off

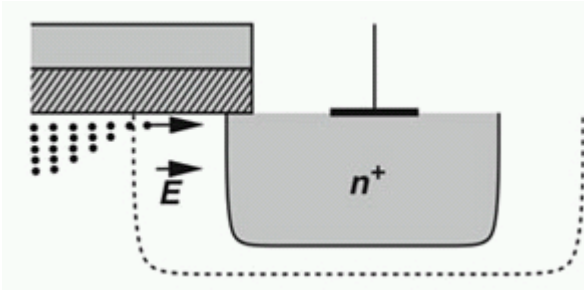


What if $V_D > V_G - V_{TH}$?

No channel between L_1 and L!



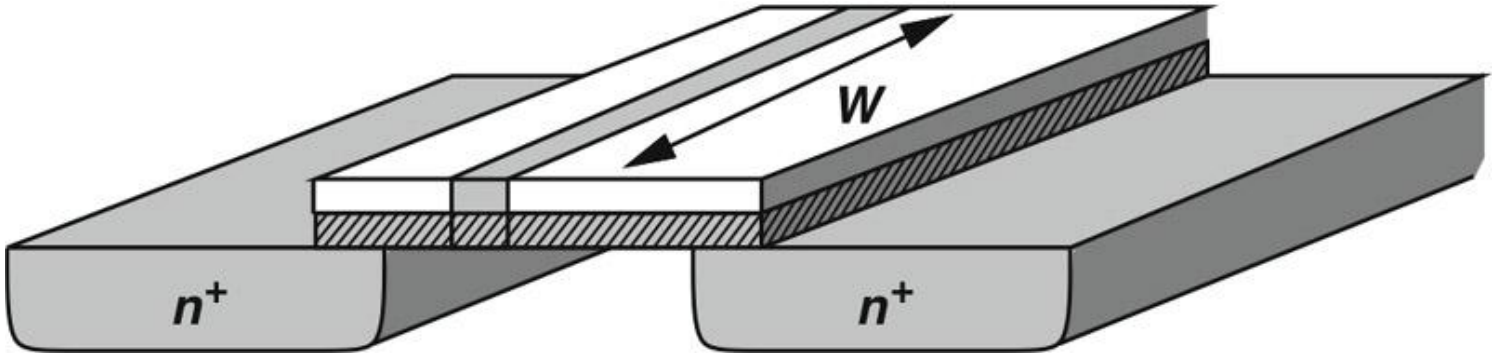
So it does not conduct current?



MOSFET acts as a constant current source

Channel Charge Density

Channel charge density: the channel charge per unit *length*



$Q = CV$

$C = WC_{ox}$

$V = V_{GS} - V_{TH}$

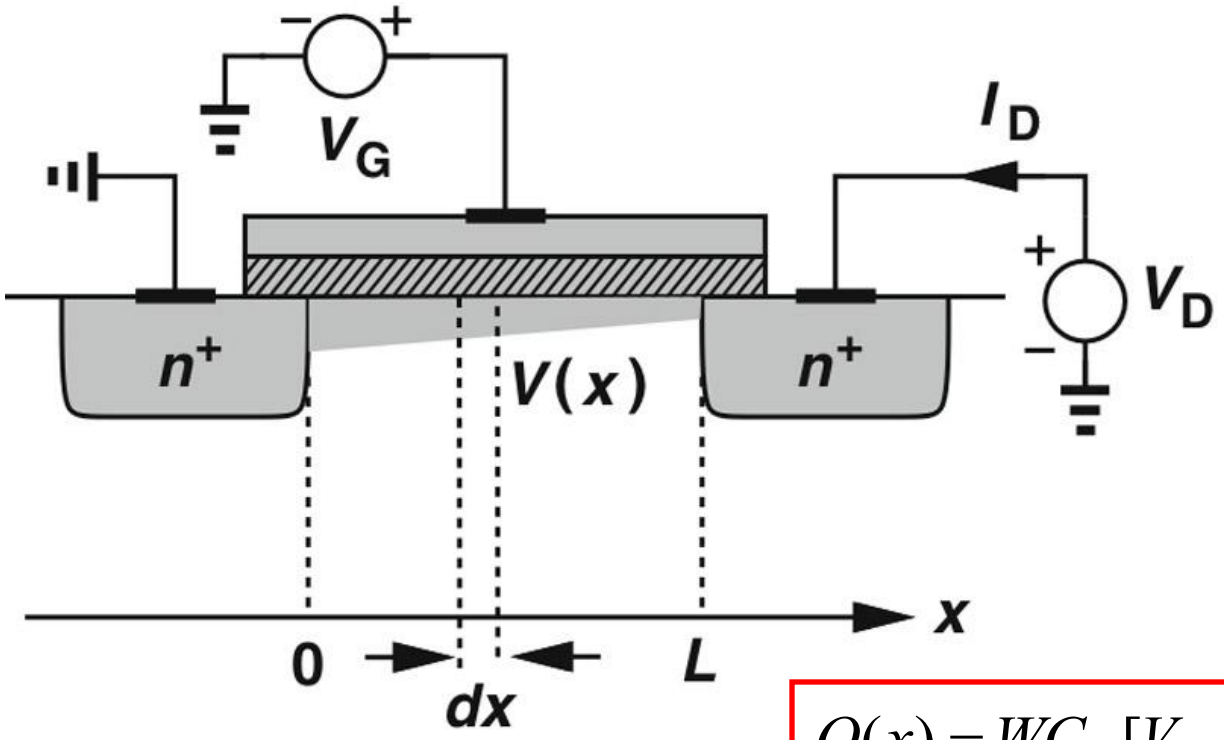
Q: charge density
C: gate capacitance per unit length
V: voltage difference between gate and channel
C_{ox}: gate capacitance per unit *area*

$$\Rightarrow \quad Q = WC_{ox}(V_{GS} - V_{TH}).$$

Channel voltage is not a constant!

- The channel charge density is equal to the gate capacitance times the gate voltage in excess of the threshold voltage.

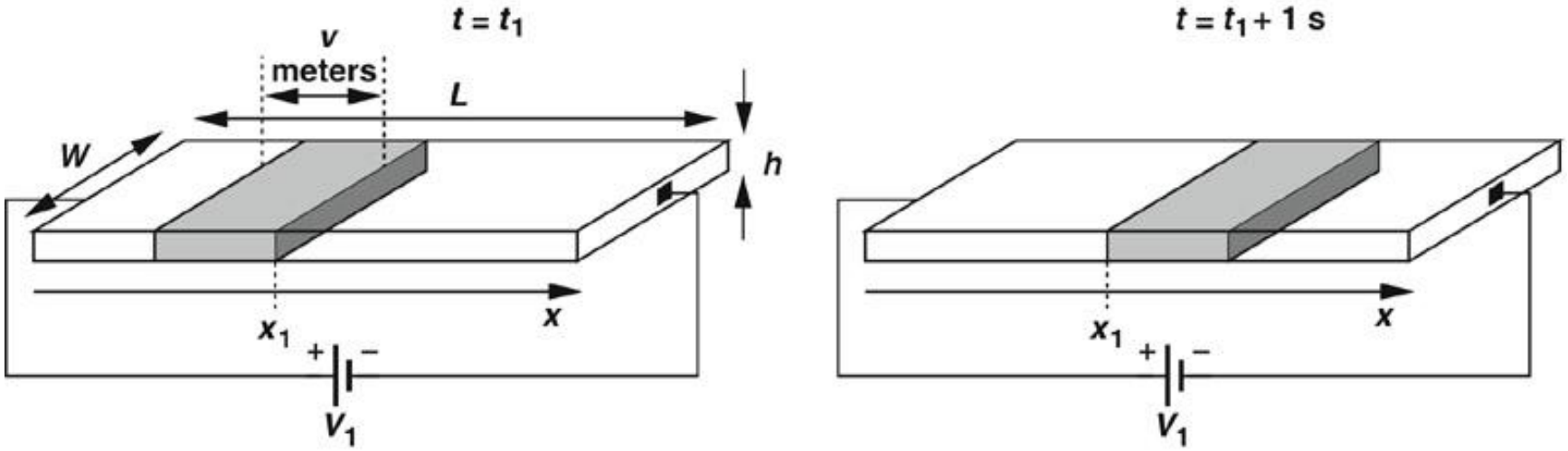
Charge Density along Channel



$$Q(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}],$$

- Let x be a point along the channel from source to drain, and V(x) its potential; the expression above gives the charge density (per unit length).

Charge Density and Current



$$I = Q \cdot v,$$

$$v = -\mu_n E, = +\mu_n \frac{dV}{dx},$$

Q: uniform charge density (per unit length)

I: current carried

- the total charge that passes through the cross section of the bar in one second

v: carriers move with a velocity of v m/s

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}.$$

$$\int_{x=0}^{x=L} I_D dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n C_{ox} W[V_{GS} - V(x) - V_{TH}]dV.$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2].$$

I_D vs. V_{DS}

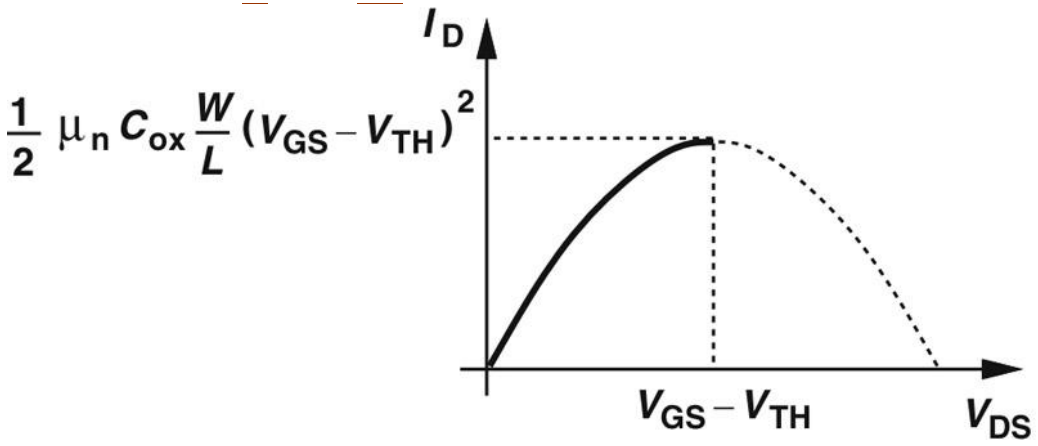
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2].$$

(1) Linear dependence of I_D upon μ_n, C_{ox}, W/L (aspect ratio)

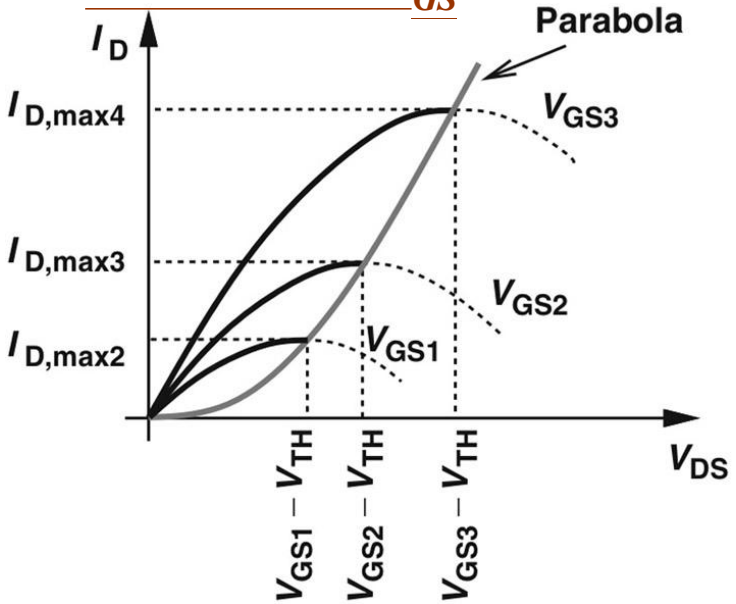
(2) For a constant V_{GS}, I_D varies *parabolically* with V_{DS}, reaching a maximum

$$I_{D,max} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \qquad V_{DS} = V_{GS}-V_{TH}$$

Parabolic $I_D - V_{DS}$ characteristic



$I_D - V_{DS}$ characteristics for different V_{GS}



I_D vs. V_{DS} (for small V_{DS})

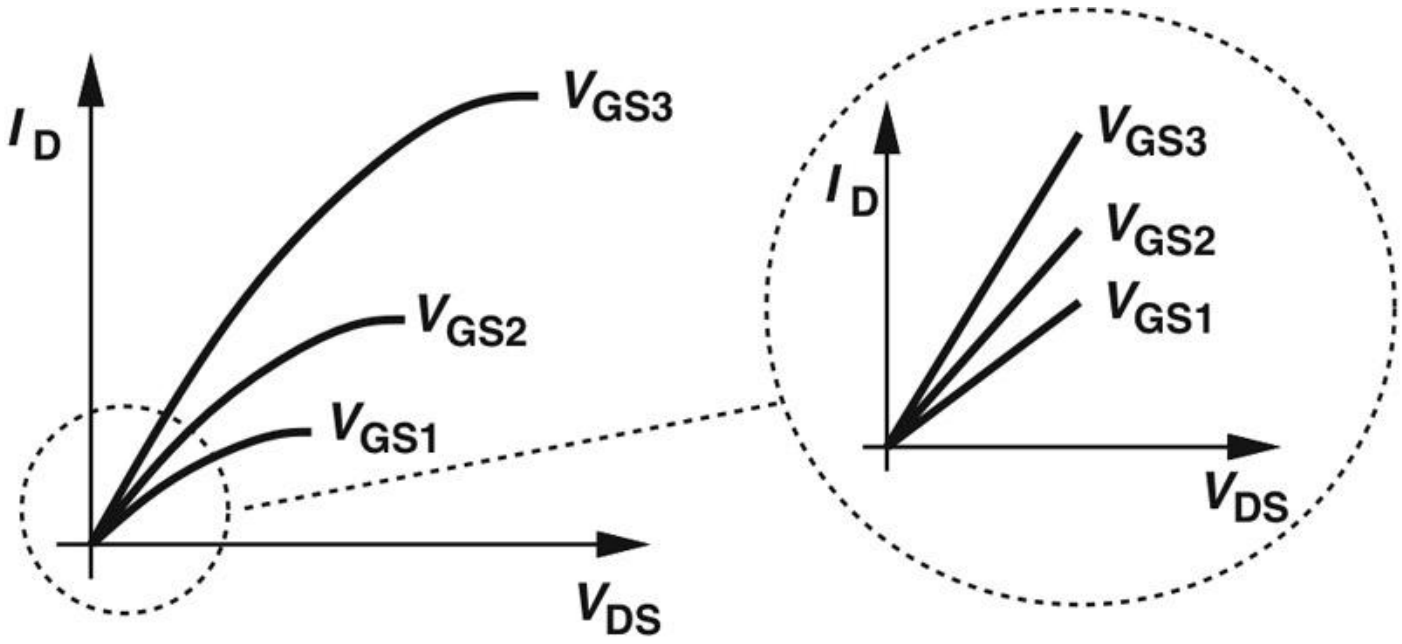
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2].$$

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}.$$

For $V_{DS} << 2(V_{GS}-V_{TH})$

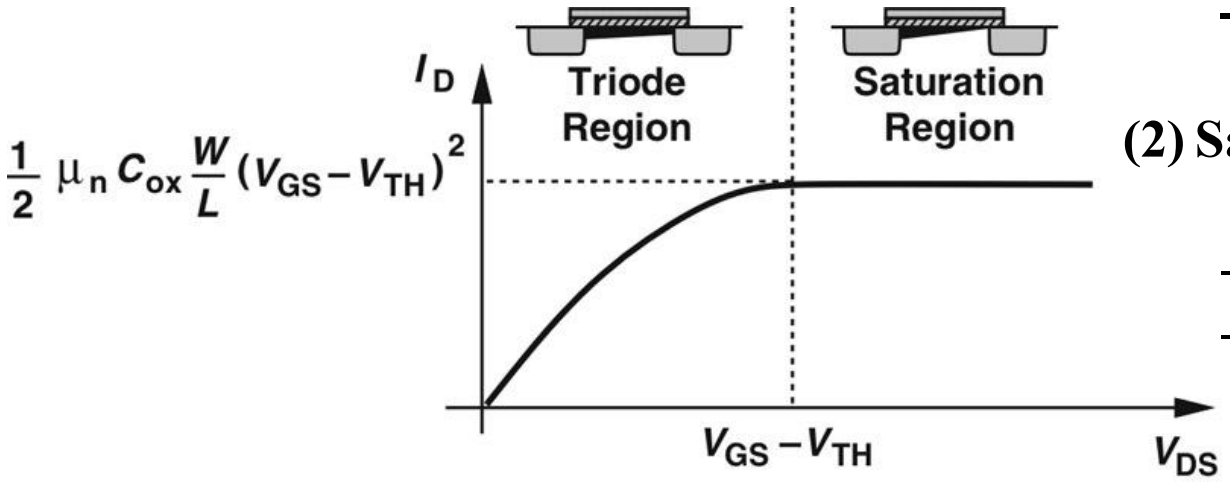
$$I_D \approx \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})V_{DS},$$

Can work as an electronic switch!



Triode and Saturation Regions

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2].$$



(1) Triode region (Linear region)

$$V_{DS} < V_{GS} - V_{TH}$$

- **Deep triode region**

$$V_{DS} << 2(V_{GS} - V_{TH})$$

(2) Saturation region

$$V_{DS} > V_{GS} - V_{TH}$$

- **Channel pinch-off**
- **What happens to $V_{DS}\uparrow$?**

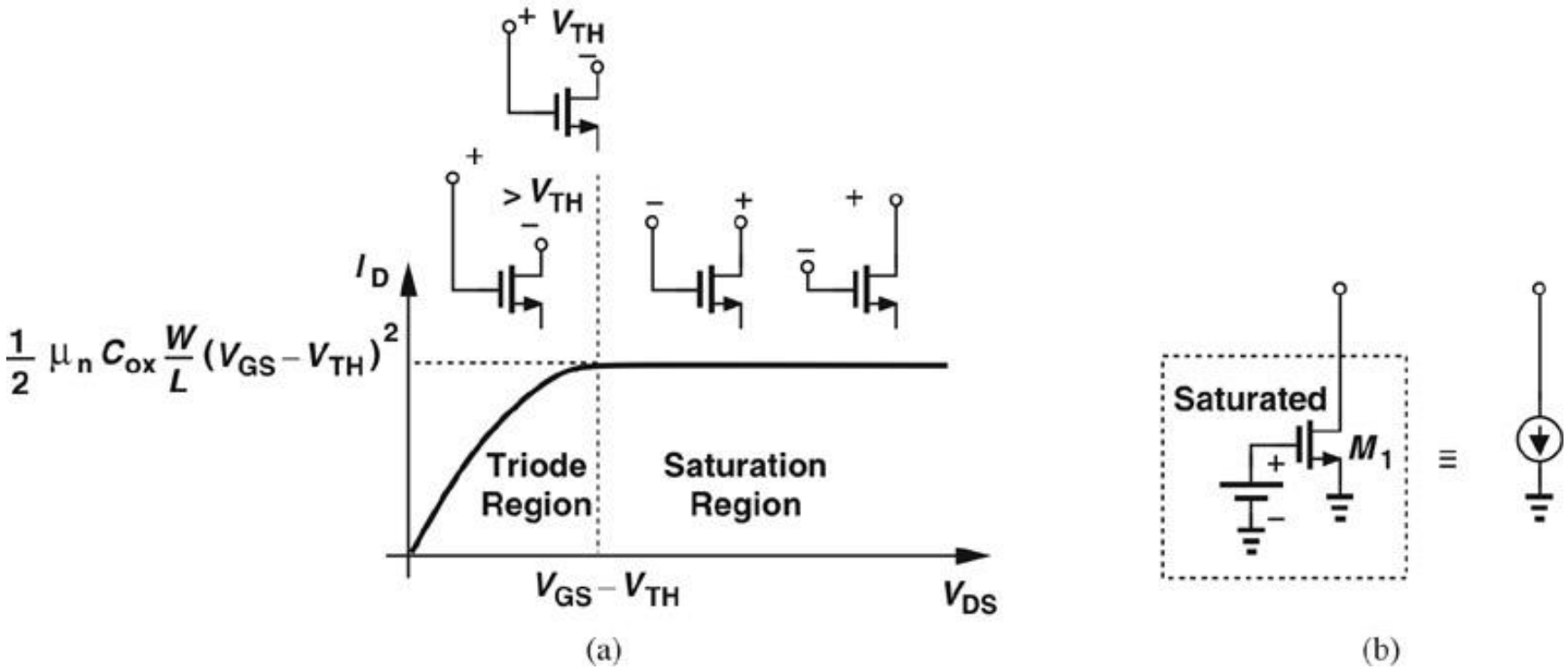
$$\int_{x=0}^{x=L_1} I_D dx = \int_{V(x)=0}^{V(x)=V_{GS}-V_{TH}} \mu_n C_{ox} W[V_{GS} - V(x) - V_{TH}]dV.$$

$$\Rightarrow \quad I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_1}(V_{GS}-V_{TH})^2, \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \quad assume \quad L_1 \approx L$$

$V_{GS} - V_{TH}$ **: overdrive voltage**

MOSFETS are "square-law" devices

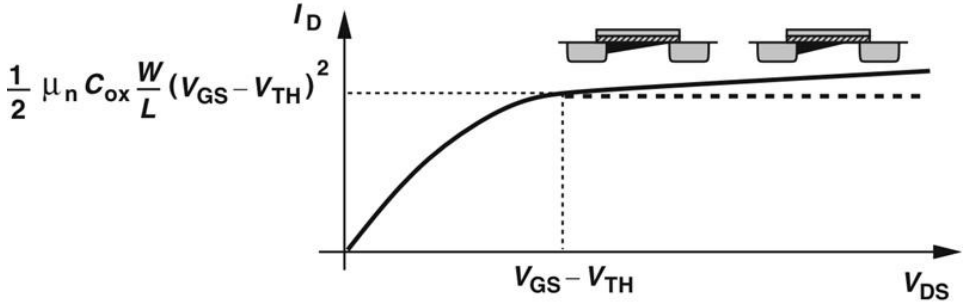
Voltage-Controlled Current Source



- **When the potential difference between gate and drain is greater than V_{TH}, the MOSFET is in triode region.**
- **When the potential difference between gate and drain becomes equal to or less than V_{TH}, the MOSFET enters saturation region.**

Channel Length Modulation

I_D increases as V_{DS} increases



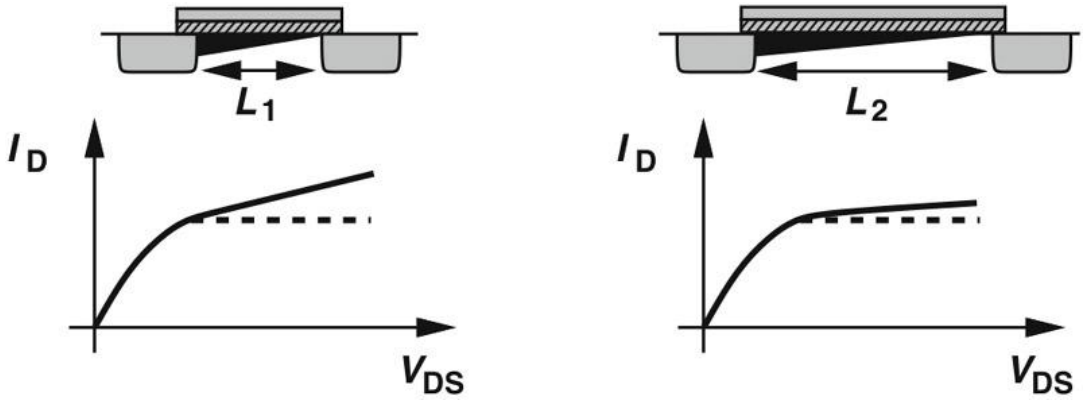
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_1}(V_{GS}-V_{TH})^2,$$

Assume L is constant

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}),$$

λ: channel length modulation coefficient

Different lengths



$\lambda \propto 1/L$

Designer has control!!

Transconductance

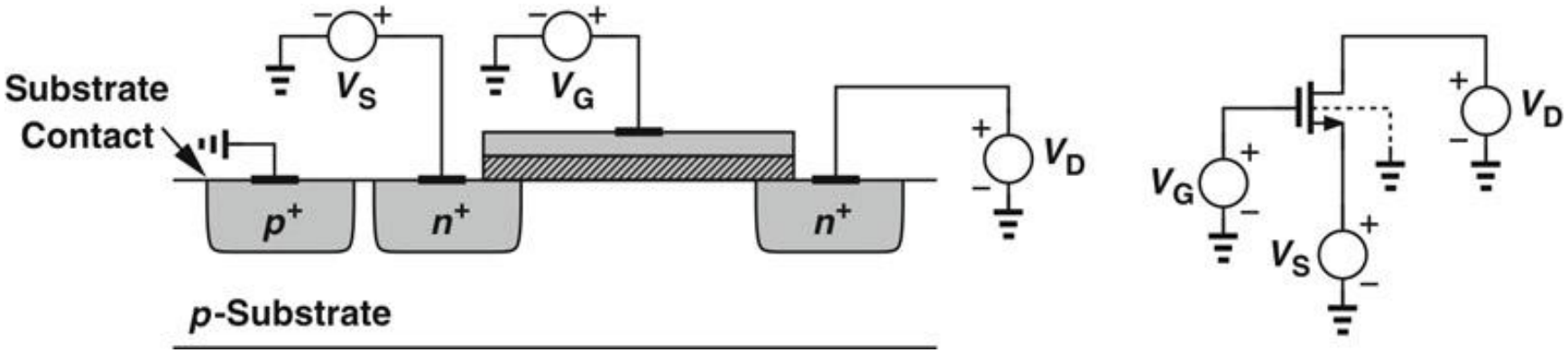
A measure of the "strength" of the device

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \qquad g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}), \qquad g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}. \qquad g_m = \frac{2I_D}{V_{GS} - V_{TH}},$$

$\frac{W}{L}$ Constant $V_{GS} - V_{TH}$ Variable	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant	$\frac{W}{L}$ Variable I_D Constant
$g_m \propto \sqrt{I_D}$ $g_m \propto V_{GS} - V_{TH}$	$g_m \propto I_D$ $g_m \propto \frac{W}{L}$	$g_m \propto \sqrt{\frac{W}{L}}$ $g_m \propto \frac{1}{V_{GS} - V_{TH}}$

Body Effect

We have assumed both source and substrate (bulk, body) are tied to ground

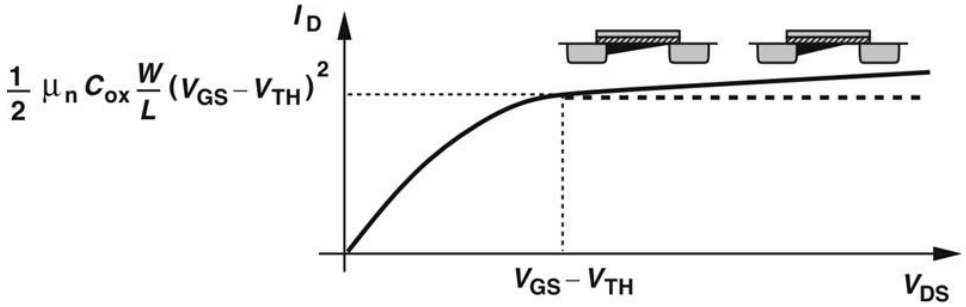


$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}),$$

V_{TH0} : threshold voltage with V_{SB} = 0
γand Φ_F : technology-dependent parameters

- **As the source potential departs from the bulk potential, the threshold voltage changes.**

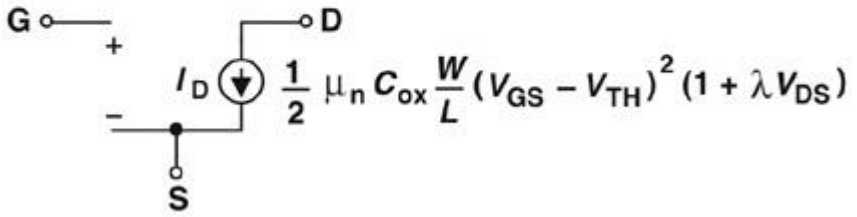
Large-Signal Model



Saturation region

$V_{GS} > V_{TH}$

$V_{DS} > V_{GS} - V_{TH}$



Triode region

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2].$$

Saturation region

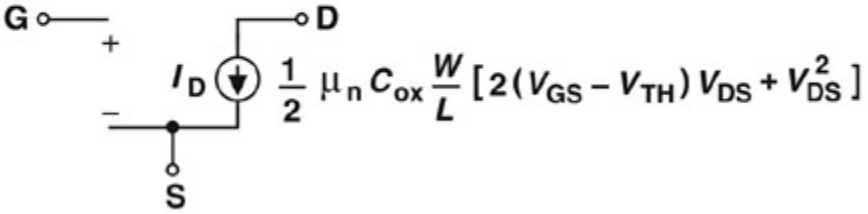
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}),$$

Gate remains an open circuit to represent the zero gate current

Triode region

$V_{GS} > V_{TH}$

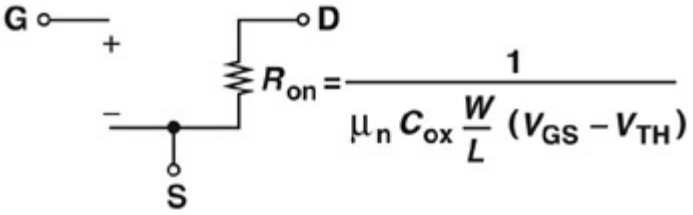
$V_{DS} < V_{GS} - V_{TH}$



Deep triode region

$V_{GS} > V_{TH}$

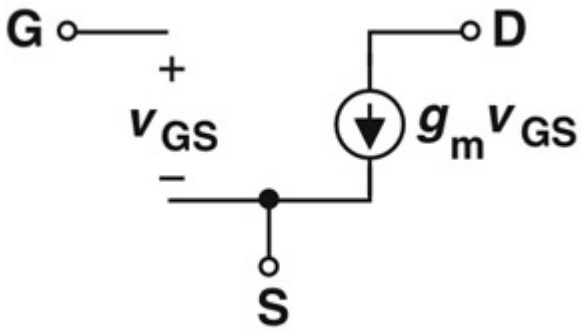
$V_{DS} << 2(V_{GS} - V_{TH})$



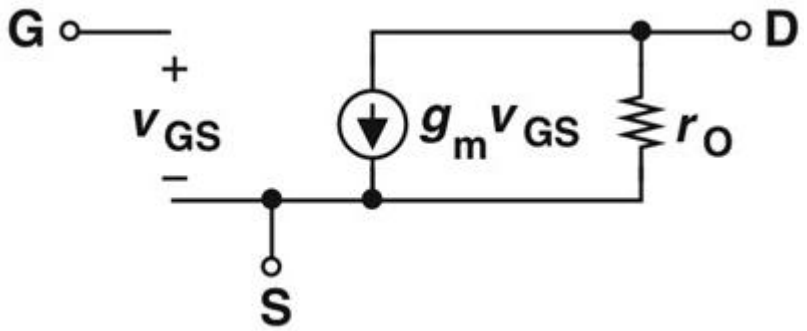
Small-Signal Model

Small-signal model in saturation region is of interest

Voltage-controlled current source



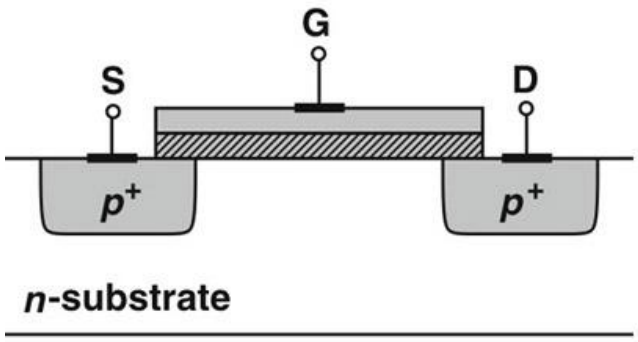
With channel-length modulation



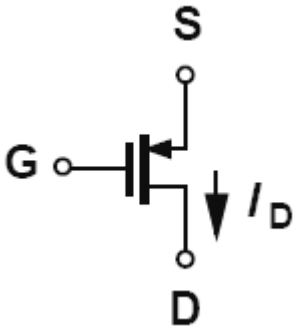
$$r_O = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \cdot \lambda}. \qquad r_O \approx \frac{1}{\lambda I_D}.$$

- **When the bias point is not perturbed significantly, small-signal model can be used to facilitate calculations.**

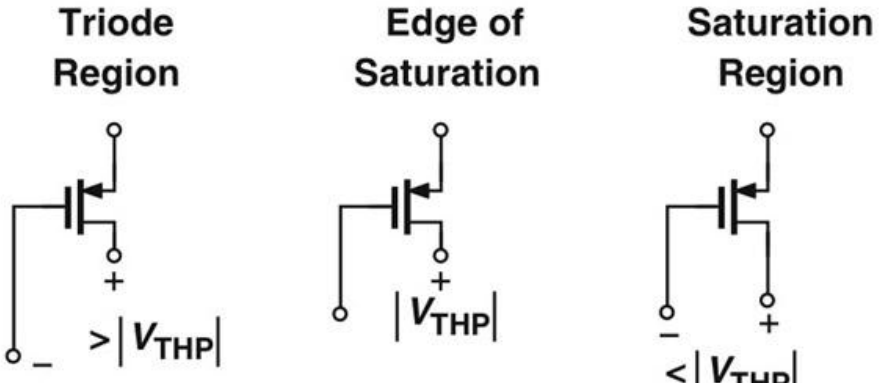
PMOS Transistor



(a)



(b)



(c)

Saturation region

$$I_{D,sat} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1-\lambda V_{DS}),$$

Triode region

$$I_{D,tri} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2].$$

Very confusing!!!

Saturation region

$$|I_{D,sat}| = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(|V_{GS}|-|V_{TH}|)^2(1+\lambda|V_{DS}|)$$

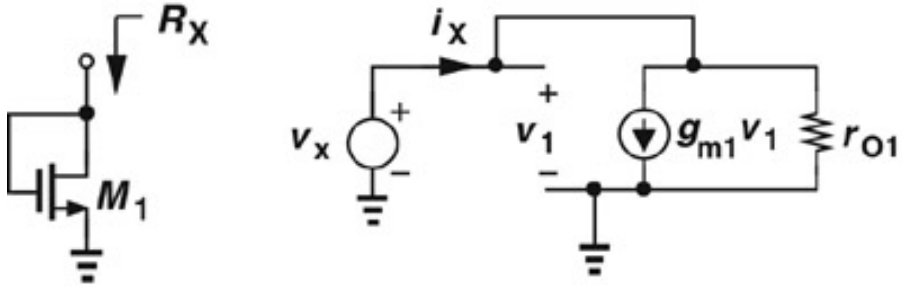
Triode region

$$|I_{D,tri}| = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(|V_{GS}|-|V_{TH}|)|V_{DS}|-V_{DS}^2].$$

Small-Signal Model

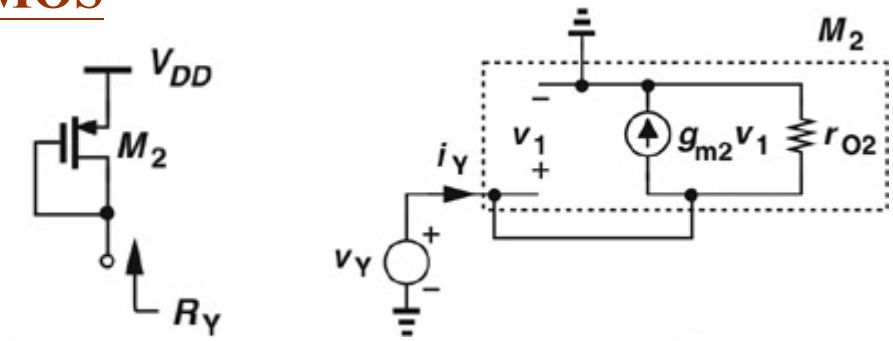
<Example 6.16> Determine the small-signal resistances R_X and R_Y. Assume $\lambda \neq 0$.

NMOS



$$R_X = \frac{v_X}{i_X} = (g_{m1}v_X + \frac{v_X}{rO1})\frac{1}{i_X} = \frac{1}{g_{m1}} \| r_{O1}.$$

PMOS



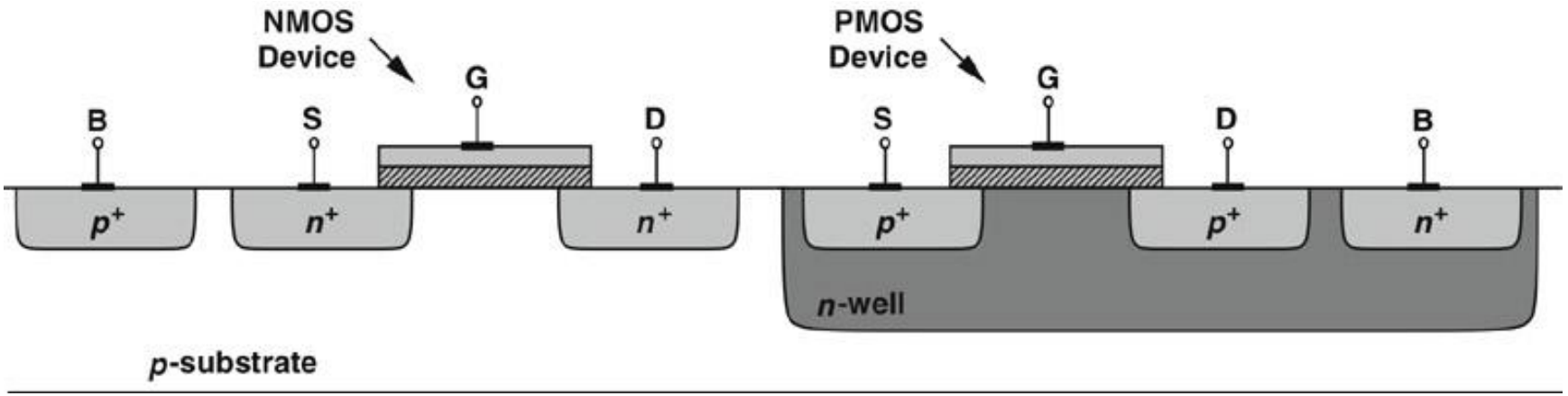
$$R_Y = \frac{v_Y}{i_Y} = (g_{m2}v_Y + \frac{v_Y}{rO1})\frac{1}{i_Y} = \frac{1}{g_{m2}} \| r_{O2}.$$

"Diode-connected" devices

The small-signal model of PMOS is identical to that of NMOS!

CMOS Technology

"Complementary MOS" (CMOS) technology



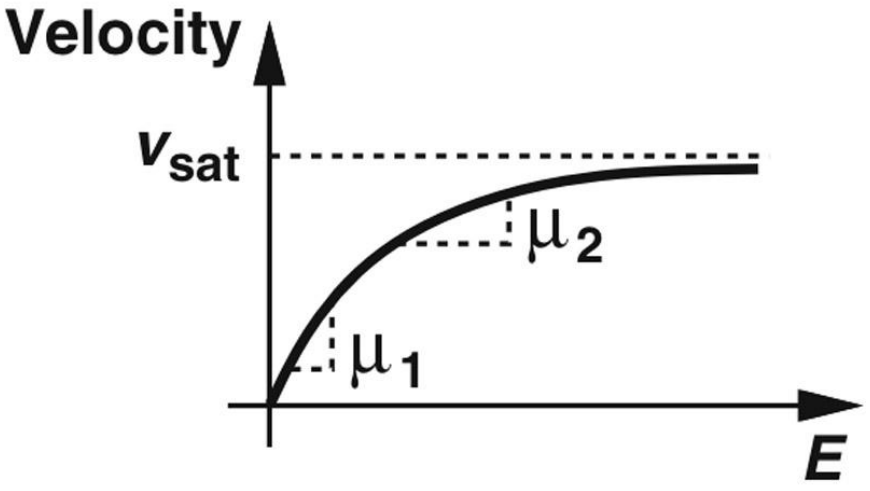
- **It possible to grow an n-well inside a p-substrate to create a technology where both NMOS and PMOS can coexist.**
- **It is known as CMOS, or "Complementary MOS".**

Short Channel Effect

- Small geometry effects arise because
  - The electric fields tend to increase because the supply voltage has not scaled proportionally.
  - The built in potential is neither scalable nor negligible.
  - The depth of S/D junctions cannot be reduced easily.
  - The mobility decreases as the substrate doping increases.
  - The subthreshold slope is not scalable.

Velocity Saturation

- **Carriers collide with the lattice frequently**
- **Time between collisions is short**
- **Not enough time to accelerate much**



$E \to \infty \qquad v \to v_{sat}$

For 0.1μm channel length, V_{DS} = 1V

$$I_D = v_{sat} \cdot Q$$
$$= v_{sat} \cdot WC_{ox}(V_{GS} - V_{TH}).$$

I_D has no dependence on L

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = v_{sat} WC_{ox},$$

g_m has no dependence on L and I_D

Mobility Degradation

- High vertical electrical field E_{ver} filed between the gate and the channel confines the charge carriers to a narrow region below the oxide-silicon interface, leading to more scattering and hence lower mobility.
- Small geometry devices experience significant mobility degradation.

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{GS}-V_{TH})}$$

  - μ_o denotes the low-field mobility and θ is a fitting parameter ~ $10^{-7}/t_{ox}$ (V^{-1}).
  - θ rises as t_{ox} drops.
  - If t_{ox} =*100 Å,* θ~ $1V^{-1}$, the mobility begins to fall considerably as the overdrive exceeds 100 mV.

$$I_D = \frac{1}{2}\frac{\mu_0 C_{ox}}{1+\theta(V_{GS}-V_{TH})}\frac{W}{L}(V_{GS}-V_{TH})^2$$

Assume $\theta(V_{GS}-V_{TH}) << 1$

$$I_D \approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\left[1-\theta(V_{GS}-V_{TH})\right](V_{GS}-V_{TH})^2 \approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\left[(V_{GS}-V_{TH})^2-\theta(V_{GS}-V_{TH})^3\right]$$

  - Lead to higher harmonics in the drain current.
  - The mobility degradation with the E_{ver} affects the device g_m as well.

Mobility Degradation

- High vertical electrical field E_{ver} filed between the gate and the channel confines the charge carriers to a narrow region below the oxide-silicon interface, leading to more scattering and hence lower mobility.
- $V_{GS} \uparrow \rightarrow \mu \downarrow$

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$$\mu_{eff} = \frac{\mu_0}{1 + \theta (V_{GS} - V_{TH})}$$

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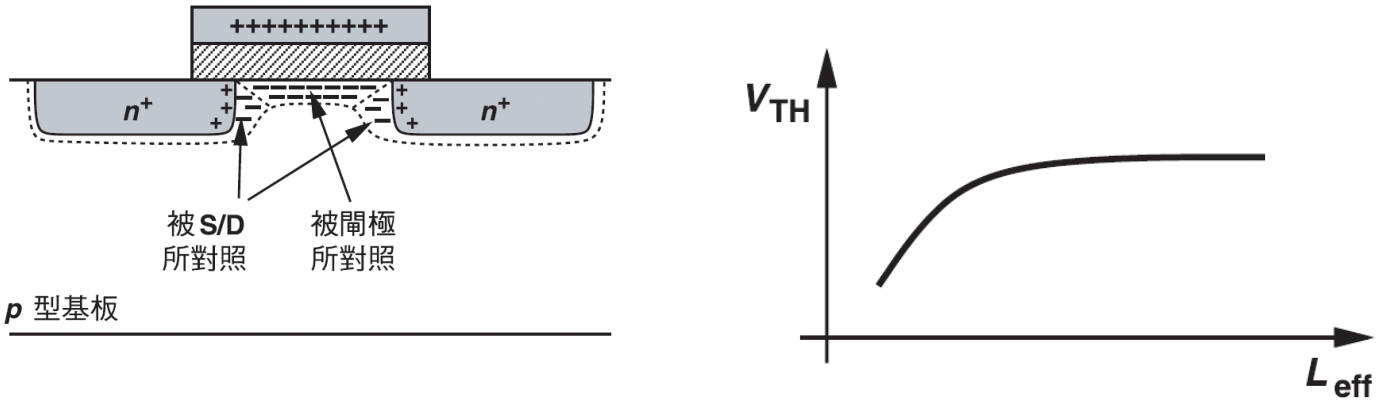
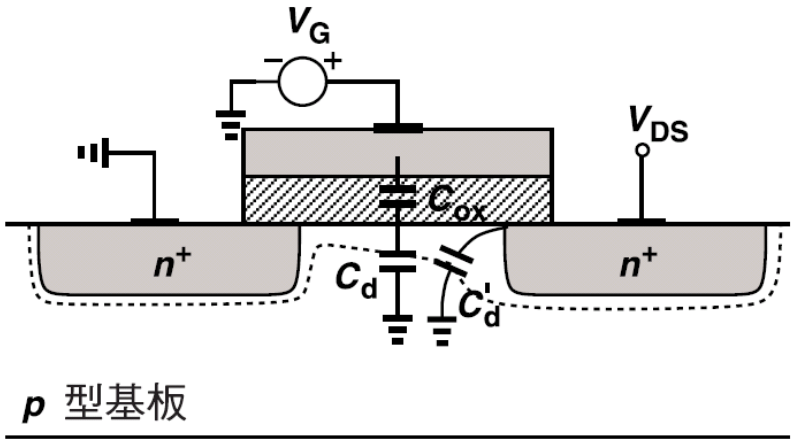
Threshold Voltage Variation

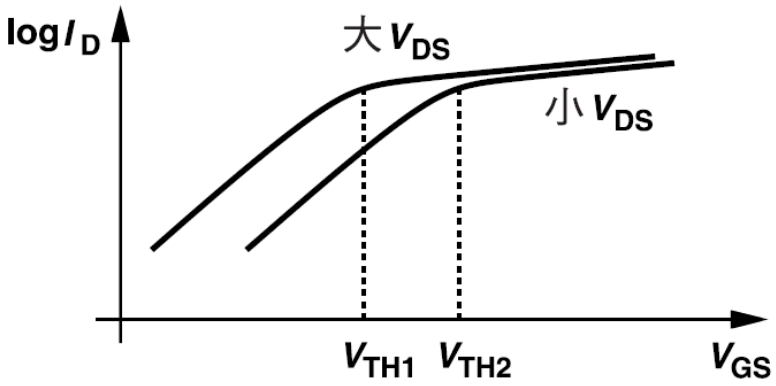


- Different lengths yield lower V_{TH} as L decreases.
  - The depletion regions associated with the source/drain is comparable to channel area.
  - Gate voltage required to create an inversion layer decreases.
  - Length variation also introduces additional variations in V_{TH}.
- If the length is increased for a higher output impedance, then the threshold voltage also increases by as much as 100 ~ 200 mV.

DIBL



(a)



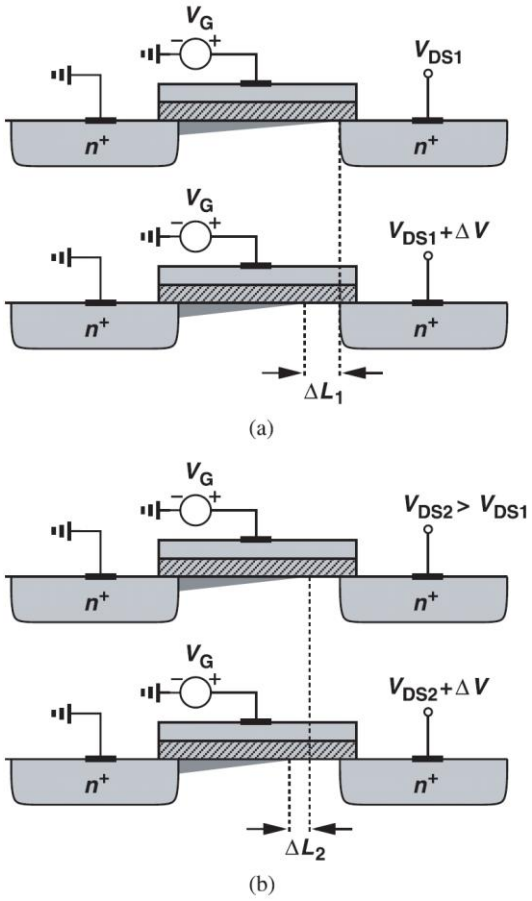
(b)

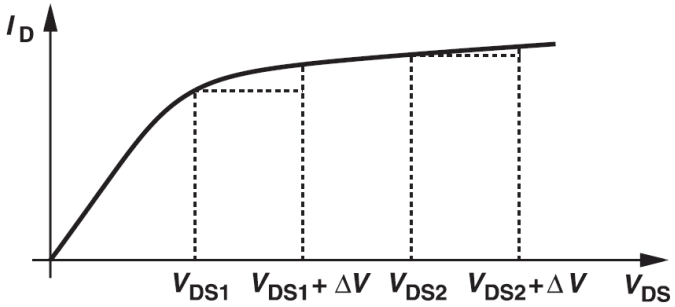
- DIBL: Drain Induced Barrier Lowering
  - In short channel devices, the ***drain voltage*** also makes the surface more positive by creating a two-dimensional field in the depletion region.
  - The drain introduces a capacitance C_d' that raises the surface potential in a manner similar to C_d .
  - The barrier to the flow charge and hence the threshold voltage are decreased.
  - The principal impact of DIBL on circuit design is the degraded output impedance. (p.2-67)

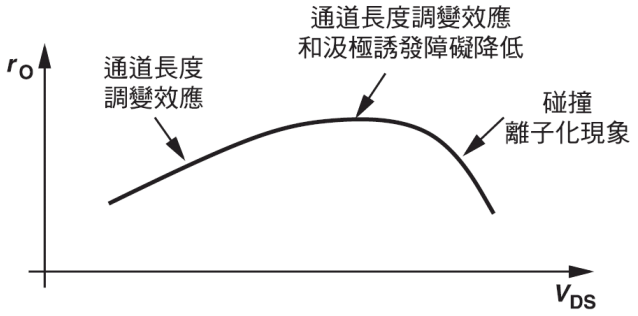
Hot Carrier Effect

- The instantaneous velocity and hence the kinetic energy of carriers continue to increase as they accelerate towards the drain.
- Hot carriers may hit the silicon atoms at high speeds, thereby creating impact ionization.
  - New electrons and holes are generated, with the electrons absorbed by the drain and the holes by the substrate.
  - A finite drain substrate current appears.
  - If the carriers acquire a very high energy, they may be injected into the gate oxide and even flow out the gate terminal, introducing the gate current.
  - Supply voltage scaling becomes inevitable.

r_o Variation with V_{DS}







- As V_{DS} increases and the pinch off point moves toward the source, the rate at which the depletion region around the drain becomes wider decreases, resulting in a higher incremental output impedance.
- The W_{dep} is a strong function of the voltage of small $V_{reverse}$ and becomes weak with large $V_{reverse}$.
- ***Impact ionization*** limits the maximum gain that can be obtained from cascode structures because it introduces a small-signal resistance from ***the drain to the substrate*** rather than ***to the source***.