Lecture 2: Micromachining Processes

Contents

- Deposition (Additive techniques)
- Pattern Transfer: Optical Lithography
- Etching (Subtractive techniques)
  - Bulk Micromachining and Surface Micromachining
  - Wet Etching and Dry Etching

References:
(1) G. Kovacs, Micromachined Transducers Sourcebook
(2) M. Madou, Fundamentals of Microfabrication
(3) J.W. Gardner et al., Microsensors MEMS and Smart Devices
(4) S.A. Campbell, The Science and Engineering of Microelectronic Fabrication
The Toolbox: Processes for Micromachining

- Some are inherited from IC fabrication (e.g., optical lithography), and some are unique for MEMS only (e.g., wet etching, wafer bonding, deep reactive ion etching (DRIE), etc)

### Deposition (additive)
- Sputtering
- Evaporation
- CVD/LPCVD/PECVD
- Epitaxy
- Oxidation
- Spin-on
- Electroplating
- Wafer bonding
- Doping

### Patterning
- Optical lithography

### Etching (subtractive)
- Wet etching
- Plasma (Dry) etching:
  - Chemical
  - RIE
  - DRIE
  - Lift-off*

---

Clean Room Classification

- U.S. Federal Standard 209b

[Image: Clean Room Classification diagram]

Courtesy of M. Madou
**Processing Chamber Pressure Ranges**

- **Rough vacuum**: 0.1 – 760 torr
- **Medium vacuum**: \(10^{-4} – 10^{-1}\) torr
- **High vacuum**: \(10^{-8} – 10^{-4}\) torr
- **Ultrahigh vacuum**: < \(10^{-8}\) torr

- Most of the processing equipments used in semiconductor fabrication operate in the rough or medium vacuum regime
- Pressure measurements:
  - > 1 mtorr, use Pirani gauge whose resistance change with thermal conductivity (and thus pressure) of the gas
  - < 1 mtorr, use ionization gauge
    - Principle: use an electron stream to ionize the gas in the gauge, and an electrical field to collect the ions (current)

---

**A Parallel-Plate Plasma Reactor**

- Many low-pressure processes such as etching, chemical vapor deposition, and sputtering involve the use of plasma
- A *plasma* is a partially ionized gas produced by the applied high voltage
  - Slow ions toward cathode and fast electrons toward anode
- Plasma is sustained by the generated secondary electrons (from collisions of ions and cathode), and their subsequent collisions with neutral atoms
Cont’d: Glow Discharge and Dark Spaces

- When a moderate energy electron collides with a neutral atom, the core level electron of the atom may be excited to a higher energy state, then immediately give off the energy in the form of light (glow discharge).
- Dark spaces don’t have glow discharge:
  - Crook’s dark space: just above cathode, since most electrons have low energies.
  - Very large electric field across this space to accelerate ions (sputtering can use this!)
  - Anode dark space: anode is a sink for electrons. Very low electron density just above the anode.
  - Faraday dark space: electrons are accelerated to high energies, leading to ionization. Very few moderate energy electrons exist for glow discharge.

Physical Vapor Deposition (PVD): Sputtering

- Developed by Langmuir in the 1920’s
- Physical bombardment of inert ions (e.g. Ar+) into target to “knock out” atoms.
  - Ions accelerated by E field of the Crook’s dark space, so the target material is placed as the cathode.
- DC plasma or radio-frequency plasma ($f = 13.56$ MHz)
  - RF is intended for dielectric materials.
- Almost any thin films: metal films (Al, Ti, Pt, etc.), amorphous Si, insulators (glass and piezoelectrical ceramics PZT, ZnO).
**An Ion Incident on the Surface of the Wafer**

- Very low energy ions ⇒ bounce off
- Energy less than about 10 eV ⇒ an ion may adsorb to the surface, giving its energy to phonons (heat)
- Energy above about 30 eV ⇒ eject atoms (sputter)
- Energy above about 10 keV ⇒ the ion penetrates into the material (ion implantation)

**Step Coverage for Sputtering**

- Dependent on temperature, pressure, and DC bias
- Better step coverage and better adhesion to the substrate than the evaporation technique
  - Because the energy level of sputtered atoms is about 100 times higher (higher surface mobility)
Deposition Rate: Sputter Yield

- Deposition rate depends on:
  - Ion flux to the target (Langmuir-child relation)
    \[ J_{\text{ion}} \propto \frac{1}{m_{\text{ion}}} \frac{V^{3/2}}{d^2} \]
  - The probability that a collision will eject a target atom
  - The transport of the ejected atoms across the plasma to the substrate
- Sputter yield \( S = \frac{\# \text{ of target atoms ejected}}{\# \text{ of incident ions}} \)
  - Sputtering must happen above a threshold ion energy

Sputtering of Aluminum

- Aluminum is the major metallization material used in integrated circuits (now gradually shift to Cu in sub-\(\mu\)m CMOS processes)
  - Low resistivity; less RC time delay
  - Good adhesion to the dielectric layer (SiO\(_2\))
- Issues of using Al in CMOS:
  - Silicon has certain solid solubility with respect to Al at around 400 °C (the Spiking phenomenon)
    - The cure: add about 1% silicon in Al
  - Electromigration: open circuit due to the movement of grain boundary
    - The cure: add some Cu in Al
The Spiking Phenomenon in CMOS

**Room temperature:**

```
SiO₂
```

```
Source  Gate  Drain
```

```
p-type substrate
```

**Above 400 °C: short circuit can happen**

```
SiO₂
```

```
Source  Gate  Drain
```

```
p-type substrate
```

---

**PVD: Evaporation**

- Evaporation is seldom used for IC fabrication because of its poor step coverage (especially when line-width becomes narrower)
- Local heating of target material to generate vapor, followed by condensation
  - Atoms travel in straight line due to low pressure
- Techniques
  - Resistive Heating
  - Electron Beam
    - Accelerated electrons strikes and melt materials
    - Better film quality
    - X-rays produced during strikes (crystal and electronics damages)
Refactory metals (Ta, W, Mo, and Ti) have very high melting temperatures and therefore have low vapor pressures.

Source: S.A. Campbell

---

**Evaporation Film Thickness**

- Line of sight deposition – POOR STEP COVERAGE
  - Need to rotate substrate to achieve uniform thickness

Without substrate rotation

With substrate rotation
Deposition: Chemical Vapor Deposition (CVD)

- Can produce high-quality metal and dielectric films for IC fabrication (better step coverage than sputtering)
  - Single crystal films: silicon, GaAs
    - the process has its own name called Epitaxy
  - Polycrystalline film: polysilicon, tungsten, titanium, copper
  - Amorphous films: silicon oxides and nitrides, low-k dielectrics
- Chemical reaction: better crystallinity and stoichiometry than sputtering
- Types:
  - CVD (APCVD): Atmosphere Pressure, 500 – 800 °C
  - LPCVD: Low Pressure, 500 – 800 °C
    - Pyrolytic reaction: thermal breakdown of gases
  - PECVD: Plasma Enhanced deposition rate, ~ 300 °C
    - Compatible with IC metallization

CVD Principles

(a) Diffusion of reaction gas to the substrate surface
(b) Absorption to the substrate
(c) Chemical reaction (film deposition) with energy provided through the substrate
(d) Desorption of by-products into the boundary-layer
(e) Pump out
Transfer Mechanisms in CVD for Chemical Reactions

- Heat (energy) transfer:
  - Conduction: use a susceptor in contact with the wafer
  - Convection
  - Radiation
- Momentum transfer:
  - Laminar flow: preferred, for better film quality
  - Turbulent flow
- Mass transfer:
  - Diffusion through the boundary layer
- The slowest of the above three mechanisms limits the reaction rate

Laminar or Turbulent Flow?

- We can use Reynolds number (non-dimensional) to determine:
  \[ R_e = \frac{dpv}{\mu} \]
  - \( d \): diameter of the flow path, \( p \): density, \( v \): velocity, \( \mu \): viscosity
  - \( R_e < 2100 \Rightarrow \) Laminar flow, and turbulent flow otherwise
- Molecular flow: the mean free path of particles is larger than the chamber size, therefore less collisions and slower reaction rate
  - Not preferred for use in CVD
**Limits of the Reaction Rate**

- (a) Surface-reaction limited
- (b) Diffusion- or mass-transfer limited

» In general (not always true), (a) occurs at low temperatures, and (b) at high temperatures

![Diagram showing surface-reaction limited and mass-transfer limited](image)

**Growth Rate vs. Temperature**

- Deposition rate (log scale)
- Mass-Transport Limited regime
- Reaction Rate Limited Regime

![Graph showing growth rate vs. temperature](image)
The Issue of Nucleation (長晶) in CVD

- (a) Homogeneous (or gas phase) nucleation: reaction occurs above the substrate and particles gradually accumulate on the surface
  - Would like to avoid in CVD; Bad morphology
- (b) Heterogeneous nucleation: reaction has to consider the surface (e.g., wetting)
  - Preferred!! Better film quality

(A) Homogeneous (B) Heterogeneous

APCVD, LPCVD, and PECVD

- APCVD: reaction occurs around 1 atm; high collision frequency
  - High reaction rate
  - Homogeneous reaction
- LPCVD: low pressure; less collisions
  - Slower reaction rate than APCVD
  - Excellent film quality
- PECVD: in addition to the three transfer mechanisms, a separate plasma is produced to enhance reaction rate, and lower the required reaction temperature
  - Negatively impact the stoichiometry
  - The good: The ion bombardment from plasma can be used to tune down the internal film stress
LPCVD Furnace Tube

CVD Silicon Dioxide

- Most popular dielectric film, can be grown *in situ* (e.g., thermally grown gate oxide) or deposited
- Types of Reactions:
  - Silane + O₂ (LPCVD): SiH₄ + O₂ → SiO₂ + 2H₂
  - Tetraethoxysilane (TEOS) decomposition (LPCVD):
    Si(OH)₂ → SiO₂ + 4C₂H₄ + 2H₂O
    - Excellent uniformity and step coverage
  - PECVD: SiH₄ + 2 N₂O → SiO₂ + 2N₂ + 2H₂
**Oxide Color Chart**

- Interference causes colorization of light reflected from thin films; color is dependent on film thickness
  - A handy solution; eliminate the use of an ellipsometer

<table>
<thead>
<tr>
<th>$t_{ox}$ (um)</th>
<th>color</th>
<th>$t_{ox}$ (um)</th>
<th>color</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.05</td>
<td>tan</td>
<td>0.54</td>
<td>yellow green</td>
</tr>
<tr>
<td>0.12</td>
<td>royal blue</td>
<td>0.60</td>
<td>pink</td>
</tr>
<tr>
<td>0.20</td>
<td>light gold</td>
<td>0.80</td>
<td>orange</td>
</tr>
<tr>
<td>0.25</td>
<td>orange</td>
<td>0.89</td>
<td>blue</td>
</tr>
<tr>
<td>0.31</td>
<td>blue</td>
<td>1.00</td>
<td>pink</td>
</tr>
<tr>
<td>0.34</td>
<td>green</td>
<td>1.10</td>
<td>green</td>
</tr>
<tr>
<td>0.39</td>
<td>yellow</td>
<td>1.19</td>
<td>red violet</td>
</tr>
<tr>
<td>0.47</td>
<td>violet</td>
<td>1.28</td>
<td>yellow</td>
</tr>
<tr>
<td>0.49</td>
<td>blue</td>
<td>1.40</td>
<td>orange</td>
</tr>
<tr>
<td>0.52</td>
<td>green</td>
<td>1.50</td>
<td>blue</td>
</tr>
</tbody>
</table>

**CVD Polysilicon**

- Polysilicon is one of the most popular MEMS structural material; For IC, it can be MOSFET gate material, high-value resistor, and conductor (with silicide film)
- Can be deposited using pyrolytic reaction: $\text{SiH}_4(g) \rightarrow \text{Si}(s) + 2\text{H}_2(g)$
- LPCVD polysilicon (600 – 700 °C) exhibits a crystalline grain structure. PECVD polysilicon is completely amorphous
- Requires annealing @900 °C or above to reduce stress (~50 MPa) for MEMS applications
Annealing (回火)

- Use high temperature to re-arrange the crystal structure and reduce the defect density
  - Also for film stress control
  - For IC, annealing is required after ion implantation
- Rapid Thermal Annealing (RTA): can increase and decrease the temperature very rapidly
  - You may use it when long-time annealing would affect existing devices

- Defect types:
  - (a) Vacancy
  - (b) Self-interstitial
  - (c) Dislocation
  - (d) Substitutional impurity

Thermal Oxidation of Silicon

- Highest-quality SiO₂ (e.g., 10 nm gate oxide) is obtained by oxidizing Si in dry O₂
  - Reaction: Si + O₂ → SiO₂
  - The Oxide is stoichiometric, has high density, and is pinhole free
- Wet oxidation is used to make thicker oxides (up to ~1.5 um)
  - Quality not as good as obtained by dry oxidation
  - Film thickness characterized by Deal-Grove model
  - Reaction: Si + H₂O → SiO₂ + H₂
- 46% of grown oxide is below original Si surface
- Short times: reaction-rate limited; linear rate
- Long times: diffusion limited; parabolic rate

\[
\text{Silicon wafer} \rightarrow \rightarrow \rightarrow \rightarrow \rightarrow \rightarrow \rightarrow
\]
\[
\text{After oxidation}
\]
\[
0.54 t_{ox}
\]
**Thermal Oxides**

- For IC (e.g., CMOS), the electronic quality of the Si/SiO₂ interface is closely related to the interface trap states, oxide surface charges, bulk oxide charges and mobile charges.
  - These issues are not as important in MEMS
    - Used most often as the structural layer, the sacrificial layer, or a dielectric layer

---

**Deal-Grove Model**

- The final oxide thickness \( x_f \) is given by:

\[
x_f = 0.5 A_{DG} \left[ \sqrt{1 + \frac{4 B_{DG}}{A_{DG}} (t + \tau_{DG})} - 1 \right]
\]

\[
\tau_{DG} = \frac{x_i^2}{B_{DG}} + \frac{x_i}{\left( \frac{B_{DG}}{A_{DG}} \right)}
\]

- Deal-Grove rate constants for dry oxidation

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>( A_{DG} ) (um)</th>
<th>( B_{DG} ) (um/hr)</th>
<th>( \tau_{DG} ) (hr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>920</td>
<td>0.235</td>
<td>0.0049</td>
<td>1.4</td>
</tr>
<tr>
<td>1000</td>
<td>0.165</td>
<td>0.0117</td>
<td>0.37</td>
</tr>
<tr>
<td>1100</td>
<td>0.090</td>
<td>0.0270</td>
<td>0.067</td>
</tr>
</tbody>
</table>
Properties of Thermal SiO₂

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistivity @25°C (Ω cm)</td>
<td>3 - 5 × 10¹⁵</td>
</tr>
<tr>
<td>Density (g/cm³)</td>
<td>2.24-2.27 (dry); 2.18-2.20 (wet)</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>3.9</td>
</tr>
<tr>
<td>Dielectric strength (V/cm)</td>
<td>2 × 10⁶(dry); 3 × 10⁶(wet)</td>
</tr>
<tr>
<td>Energy gap (eV)</td>
<td>9</td>
</tr>
<tr>
<td>Etch rate in buffered HF (Å/min)</td>
<td>1000</td>
</tr>
<tr>
<td>Refractive index</td>
<td>1.46</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm°C)</td>
<td>0.014</td>
</tr>
<tr>
<td>Specific heat (J/g°C)</td>
<td>1.0</td>
</tr>
<tr>
<td>Thermal expansion coefficient (°C⁻¹)</td>
<td>5 × 10⁻⁷</td>
</tr>
</tbody>
</table>

Spin-on Deposition

- “Spin” and “spread”
- Material types
  - Dielectric insulators
    - spin-on glass (SOG) : interlayer dielectric for IC
  - Organic materials
    - Photoresist (PR)
    - Polyimides
    - SU-8 (very thick photoresist, ~ 100 um)
    - Organic polymer

Liquid solution

wafer
**Deposition by Electroplating**

- Metal ions in solution deposit on conductive surface at negative potential.
- DC or pulsed electroplating; the latter has better corner coverage.

Reactions:
\[ \text{Ni}^{2+} + 2e^- \rightarrow \text{Ni} \text{ (cathode)} \]
\[ 2\text{Cl}^- \rightarrow \text{Cl}_2 + 2e^- \text{ (anode)} \]

---

**“Black” Metal Films**

- Electroplating using high current density creates uneven crystallites due to the large reactant concentration gradient.
- The tallest crystallites are favored to continue plating.
- The deposited film is porous and optically black.
- Since it is porous, the effective area increases which is beneficial for:
  - Infrared absorber in infrared detector.
  - “Platinum-black” microelectrodes to record bioelectric signals.
  - etc.
Electroless Metal Deposition

- No need to apply voltages; your familiar chemistry in senior high school
- For example, when surface of less noble metal (e.g. Zn) is immersed in copper sulphate:
  \[ \text{Zn} + \text{Cu}^{2+} \rightarrow \text{Cu} + \text{Zn}^{2+} \]
- Can be used in the IC fabrication (Cu metallization) as shown from step (a) to (e)

Wafer Bonding
- Silicon Fusion Bonding
- Anodic Bonding
- Eutectic Bonding
**Silicon Fusion Bonding**

- Can achieve direct Si-to-Si wafer bonding or with an intermediate oxide layer
  - Silicon-on-insulator (SOI) wafer can be made
- Require hydrated surfaces (immersed in an ammonium hydroxide solution)
- Bonded by van der Waals forces
- Annealed at 800 to 1000 °C to strengthen the bonds
  - Reaction: Si-O-H $\cdots$ H-O-Si $\rightarrow$ Si-O-Si + H₂O

**Silicon-On-Insulator (SOI) Technology**

- Developed by IBM; SOI can promote the performance by 30% than conventional CMOS
  - Because the reduction of capacitances
- SOI wafer can also be made using ion implantation, the so-called “SIMOX” process (Separation by Ion Implantation of Oxygen)
**Anodic Bonding**

- Anodic Bonding joins together a silicon wafer and sodium-containing glass substrate by electrostatic force
  - Thermal energy is often applied simultaneously
  - High voltages, depending on the thickness of the glass layer

![Diagram of anodic bonding](image)

**Eutectic Bonding**

- Occurs at the temperature lower than the melting points of bonded materials
  - Au and Si eutectic bonding is commonly used (@ 363 °C)
- Disadvantages:
  - Difficult to obtain complete bonding over large areas
  - Native oxide can prevent bonding to take place
**Cont’d: an Example**

Source: M. Madou, Fundamentals of microfabrication

---

**Doping**

- Elements having one valence electron, more or less, than Si (+4) are used as substitutional donors (n-type) or acceptors (p-type)
  - Boron (+3), phosphorous (+5), arsenic (+5)
  - The conducting carriers are electrons and holes for n and p types, respectively
Doping

- Two main doping techniques:
  - Diffusion
  - Ion implantation: offers the advantage of being able to place ions at any depths, independent of the thermodynamics of diffusion

Ion Implantation for Making SOI Wafers

  - Increase circuit speed and radiation hardness
  - 150 to 300 keV O⁺ at doses about $2 \times 10^{18} \text{ cm}^{-2}$
Pattern Transfer: Photolithography

- Create masks for patterning the underlying layer

1. (1) PR
2. (2) PR
3. (3) PR
4. (4) PR
5. (5) PR
Photolithography

- The major cost in IC fabrication
- Three major sequential steps:
  - Coating (光阻覆蓋): application of photoresist (PR: 光阻, a photosensitive material)
  - Exposure (曝光): to transfer mask image onto the resist
  - Development (顯影): Immersion in an aqueous developer solution to dissolve exposed resist and render desired image
- Light source:
  - Deep UV: $\lambda = 150$ to $300$ nm
  - Near UV: g-line $\lambda = 436$ nm; i-line $\lambda = 365$ nm

Resist Spinner and On-line Thickness Monitor

- Resist thickness is deduced from the interference profile of reflected light

**Wafer Cleaning**

- Wet etching is generally used
  - RCA1 (removes organic dirt): 1 part of NH$_3$ (25% aqueous solution) + 5 parts deionized (DI) water; heat up to boiling and add 1 part H$_2$O$_2$. Immerse the wafer for 10 min.
  - RCA2 (removes metal ions): 1 part HCl + 6 part DI water; heat up to boiling and add 1 part H$_2$O$_2$. Immerse the wafer for 10 min.

---

**Typical Process Flow of Photolithography**

1. Dehydration bake (去水烘烤) — To remove water particles from the wafer
2. Priming (塗底) — To coat (spin or vapor) HDMS (Hexamethyldisilazane) on wafer to promote PR adhesion
3. Resist application (上光阻) — Spin-coat PR, whose thickness is inversely proportional to spin speed $\sqrt{\omega}$
Cont’d

Drive off most of the solvent in the PR, thus further promote its adhesion to the wafer. Establish the exposure characteristics; time and temperature are both critical:
(1) Too short or too low: then more solvent in PR would affect the resolution of the exposure
(2) Too long or too high: can lead to resist dissolution of unexposed regions in the developer

To transfer photo mask (光罩) image onto PR
Exposure systems: (1) Contact (2) Proximity (3) Projection

Cont’d

Re-arrange the PR; an optional step

Developer reacts with exposed regions and produces desired PR patterns

(1) Further enhance the PR adhesion to the wafer
(2) Enhance the PR selectivity for etching
(3) Enhance the PR resistance for ion implantation
**Photoresist (PR)**

- It contains three components:
  - Resin
  - Photoactive compound (PAC): acts as an inhibitor to slow dissolution rate of the PR in the developer before exposure, and a sensitizing agent to increase the dissolution rate after exposure
  - Solvent: control the viscosity of mixed resin and PAC

- Sensitivity and resolution
  - The former refers to the amount of light energy (mJ/cm²) necessary to create the required chemical changes
  - The latter refers to the smallest features that can be reproduced in a photoresist

---

**Photo-Chemical Reactions: a Positive PR Example**

**Exposure:**

\[
\begin{align*}
\text{Exposure:} & \quad \text{O} & \quad \text{N}_2 & \quad + & \quad \text{light} & \quad \rightarrow \quad & \\
\text{N} & \quad \text{R} & \quad \text{O} & \quad + & \quad \text{N}_2 & \quad & \\
\end{align*}
\]

**Adding water:**

\[
\begin{align*}
\text{Ketene} & \quad + & \quad \text{H}_2\text{O} & \quad \rightarrow & \quad & \text{carboxylic acid} & \quad + & \quad \text{N}_2 & \\
\text{R} & \quad \text{O} & \quad & \text{C} & \quad & \text{C-OH} & \quad & \text{C-OK} & \quad \text{R} & \quad \text{O} & \quad \text{N}_2 & \quad \text{C-OH} & \quad \text{C-OK} & \quad \text{R} & \quad \text{O} & \quad \text{N}_2 & \quad \text{C-OH} & \quad \text{C-OK} & \quad & \\
\end{align*}
\]

**Soaked in KOH developer:**

\[
\begin{align*}
\text{carboxylic acid} & \quad + & \quad \text{KOH} & \quad \rightarrow & \quad & \\
\text{H}_2\text{O} & \quad & \text{R} & \quad \text{O} & \quad \text{C-OK} & \quad & \text{R} & \quad \text{O} & \quad \text{C-OK} & \quad & \\
\end{align*}
\]
**Positive and Negative Photoresists**

<table>
<thead>
<tr>
<th>Positive PR (mostly used)</th>
<th>Negative PR (not used for less than 2 µm features)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cr</td>
<td>Mask</td>
</tr>
<tr>
<td></td>
<td>Photoresist</td>
</tr>
<tr>
<td></td>
<td>Thin film</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Light-Field and Dark-Field Masks**

- **Drawn patterns**: Designer’s layout
- **Chromium**
- **Quartz or glass**

**Light field**

**Dark field**
Contact/Proximity Photolithography

- Masks are susceptible to damage and contamination during alignment

Resolution (R) in Contact and Proximity Lithography

- R is affected by optical diffraction; defined as \( 2b_{\text{min}} \)
  - For proximity printing: \( z \) is PR thickness
  \[
  2b_{\text{min}} = 3\sqrt{\frac{\lambda}{\pi}}(s + 1/2)z
  \]
  - For contact printing (\( s = 0 \)): resolution is better

Source: M. Madou
**Projection Photolithography**

- Mask patterns are imaged onto wafers with reduction (5:1 or 10:1)
- Step and repeat for complete wafer exposure
- No mask degradation
- Large mask patterns are easier to make reliably

![Canon Stepper](image)

**Linewidth Control for Projection Photolithography**

- Small optical-wavelength light source increases the resolution (R) of lens
  \[ R = K_1 \frac{\lambda}{NA} \] (NA = numerical aperture = n \cdot \sin \theta_{\text{max}})
- Large depth of focus (DOF) allows the latent image to remain in focus through the depth of the resist layer
  \[ \text{DOF} = K_2 \frac{\lambda}{(NA)^2} \]
- For example, with i-line (365 nm), NA = 0.5, K_1 = 0.65, and K_2 = 1
  \[ R = 0.47 \mu m \text{ and } \text{DOF} = 1.46 \mu m \]
Surface Reflections and Standing Waves

- The reflected and penetrated lights in the PR form the standing waves that would affect the absorbed light energy, and therefore the controlled linewidth.
- Solutions:
  - Avoid the topology and planarize the layers (the better idea!)
  - Use of an antireflective polymer between the PR and metal

Planarization

- Especially important for sub-mm IC processes with thin metal lines and narrow gaps.
- Techniques:
  - Chemomechanical Polishing (CMP)
  - Etch back planarization: use PR to smooth the surface, then etch PR and oxide (similar etch rates) in a plasma (as shown)
Types of Lithography

- The difference between using a mask and direct-write? (speed)
- Minimum linewidth?
- The cost?

Source: M. Madou

Determine Linewidth

- Optical microscope
- Scanning Electron Microscopy (SEM)
  » Has larger magnification than microscope; the material must be metal or have a metal coating before scanning
- Alpha step
- Optical profiler
  » Based on optical interference
SEM

Primary electrons → Detector

Secondary electrons

Alpha Step

Gives you a quick idea of the film thickness in the clean room

Scanning stylus
**Optical Profiler**

- Very convenient
- Vertical resolution can down to Angstroms

---

**Translational Misalignment**

- Design rules are required to make working devices
- Misalignment limits your minimum feature size

---

Perfect alignment

Unacceptable misalignment
Etching

Etch

- Based on the size of removed material:
  - Bulk micromachining: the substrate is partially or completely etched
  - Surface micromachining: structures are made by a sequence of deposition and patterning of thin films (usually < 10 um), followed by removing the sacrificial material for structural release
- Based on the etching reactant:
  - Wet etching (chemical solution)
  - Dry etching (e.g. plasma)
**Selectivity**

- Ratio of etch rates: \( S = \frac{R_{\text{etch}}}{R_{\text{mask}}} \)
- High selectivity (\( S \gg 1 \))

**Low selectivity**

**Aspect Ratio**

- High-aspect ratio
  - Trench
  - Post
- Low-aspect ratio (< 1:1)
  - Recess
  - Mesa
Bulk Silicon Micromachining

- Dates back to a piezo-resistive silicon pressure sensor (Tufte et al., Honeywell, 1962)
- Structures made by etching substrate material (usually silicon or glass wafer)
- Membranes for pressure sensors, microphones
- Nozzles for ink-jet printing, drug delivery
- Cantilevers for thermomechanical sensing
- Cavities for microfluidic chambers

Isotropy of Bulk Silicon Micromachining

- Isotropic etch
  » No direction dependence

- Anisotropic etch
  » Etch rate and profile changes with wafer or crystal orientation
### Examples of Bulk Micromachining

- Trenches, STS
- Micro-turbine, Tohoku U.
- Suspended beam, Tohoku U.
- Fuel atomiser, CWRU

**Spring, Klassen et al., 1995**

### Surface Micromachining

- Illustration of one-layer polysilicon surface micromachining
- Surface micromachining is more commonly used in IC fabrication than bulk micromachining
  - Key issues: intrinsic stress, step coverage, etc

**ENE 5400 Microelectromechanical Systems, Spring 2004**
Cont’d

- Many processes; common one used produces polysilicon microstructures
- Starts with deposition of insulating layers and sacrificial material

![Phosphosilicate Glass (PSG), 2 um thick](image1)

Insulating layers (Si₃N₄/SiO₂) ~ 1000 Å

Cont’d

- Selected regions of sacrificial material are patterned and removed (etched)
- Regions serve as anchor areas for succeeding structural material deposition

![“Anchor” cut](image2)
Cont’d

- Deposition of structural material

Phosphorous-doped polysilicon; 2 um thick

Cont’d

- Structural material is patterned and etched to create desired microstructures
- Underlying sacrificial layer is exposed
Cont’d

- Buffered hydrofluoric (HF) acid etches sacrificial material, releasing microstructure

Examples of Surface Micromachining

Gear (Sandia Lab)
3D mirror (Sandia Lab)
Micro-resonator
Optical mirror switch (Lucent)
Micro-mirrors for projection display (Texas Instrument)
Material Removal

- Wet etching
- Etch-stop
- Dry etching
  - Chemical etching
  - Ion milling
  - Plasma etching
  - Reactive-ion etching
- Lift off

Wet Etching

- Etching mechanism:
  1. Reactant transport from etchant solution to surface
  2. Surface reaction
  3. Transport of etch products from surface into solution
- Reaction rate limits:
  - Mass transport is diffusion limited $\Rightarrow$ etch rate increased by agitation
  - Surface reaction is rate limited $\Rightarrow$ etch rate increased by increasing temperature
### Anisotropic Silicon Etch

<table>
<thead>
<tr>
<th>Etchant</th>
<th>Temperature (°C)</th>
<th>Etch rate (µm/hr)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Si (100)</td>
</tr>
<tr>
<td>KOH:H₂O</td>
<td>80</td>
<td>84</td>
</tr>
<tr>
<td>KOH</td>
<td>75</td>
<td>25-42</td>
</tr>
<tr>
<td>EDP</td>
<td>110</td>
<td>51</td>
</tr>
<tr>
<td>NH₄OH</td>
<td>75</td>
<td>24</td>
</tr>
</tbody>
</table>

- EDP = EthyleneDiamine Pyrochatechol
- Note that (111) plane is etched much slower

### Silicon

- Diamond lattice crystal structure
- Each atom has 4 neighboring atoms forming a tetragonal shape
- The ‘unit cell’ is the smallest repeating cell
- ‘a’ is the lattice constant = 5.43 Å for Si

---

EN 5400 微機電系統設計, Spring 2004 87 ©施克成, 清華大學電機系
**High Selectivity of (111) Plane over (100)**

- Here is one reason: the number of dangling bonds is less for (111)

  2 dangling bonds on a (100) plane

  ![Diagram of dangling bonds](image)

  1 dangling bond on a (111) plane

**V-Shaped Grooves in a (100) Si Wafer**

![Image of V-shaped grooves](image)
**Etch Stop Techniques**

- As wet etching processes are also fundamentally charge-transport phenomena, the etch rate can be dependent on dopant type, dopant concentration, applied voltage bias
- Types:
  - Electrochemical etch stop
  - Dopant selective (e.g., with a heavily boron doped layer)
  - Dielectric Etch Stop
    - The silicon etching stops on a dielectric layer (e.g., silicon nitride) to produce a dielectric diaphragm

**Electrochemical Etch Stop**

- To achieve uniform thickness control for bulk silicon wet etching, if the n⁺ layer thickness is known
- Leakage current of reverse-biased diode affects the etching selectivity
- Wet etch stops on a passivated n-type epitaxial layer
Cont’d

- SiO₂ is formed when the passivation potential (PP) is reached (PP of n-Si is lower than PP of p-Si, so operation voltage is chosen in between)

Dopant-Selective Etch Stop

- P⁺ Etch Stop with a heavily boron doped layer (diffusion or ion implantation); produces stressed membrane due to the changed lattice constant
Dry Etching

- Chemical Etching
  - Chemical reaction
- Plasma-Assisted Etching
  - Ion beam milling: physical impingement
  - Plasma etching: energetic chemical reaction
  - Reactive-ion etching (RIE): physically assisted chemical reaction
  - Deep RIE

Chemical Etch
**Dry XeF₂ Chemical Etching**

- Gas phase etch without plasma
- Vapor phase XeF₂ (Xenon difluoride) etch of Si at room temperature:
  \[ 2\text{XeF}_2 + \text{Si} \rightarrow 2\text{Xe} + 2\text{SiF}_4 \]
- Isotropic
- Excellent selectivity over photoresist, oxide, aluminum, and nitride
- Can make CMOS-integrated MEMS devices with aluminum as mask to undercut silicon
- Ideal for dry release of surface micromachined devices if polysilicon (or silicon) is the sacrificial material

---

**Ion Beam Milling**

- Physical impingement; no etching selectivity
- Triode set-up
- Heated filament emits electrons which are accelerated to create Ar⁺
- Ar ions are then accelerated and neutralized (by electrons emitted from another filament) toward the substrate for etching
- Heavy ions promote yield!

---

*Courtesy of M. Madou*
**Ion Milling Example**

1. Al
2. (3) Ion mill
3. Note that there is almost no etching selectivity
4. (4) Use oxygen plasma to remove remaining PR

---

**Plasma Etching**

- Disassociated gas radicals in the plasma are responsible for etching
- Wafer on grounded electrode
- Reacted material is pumped out of the chamber
- \( \text{O}_2 \text{ plasma + photoresist} \rightarrow \text{CO}_2 + \text{H}_2 \text{O} \) (called “Ashing”)
- 0.1 to 10 torr operating pressure
**Reactive-Ion Etch**

- Good directionality is achieved by operating at low pressure ($10^{-3}$ to $10^{-1}$ torr) to generate relatively higher energy ions perpendicular to wafer (physical + chemical)
- Creates polymeric species by chemical cross-linking
- Fluorocarbon etching of silicon: gas phase products formed

---

**Silicon Reactive Ion Etch**

- Fluorine free radicals are responsible for Si etch with SF$_6$ plasma
  - Dissociation reactions, for example:
    $$ e^- + SF_6 \rightarrow SF_5^- + F + e^- $$
  - Ionization reactions, for example:
    $$ e^- + SF_6 \rightarrow SF_5^+ + F + 2e^- $$
  - Attachment reactions, for example:
    $$ e^- + SF_6 \rightarrow SF_5^- + F $$
**Produced Polymer during RIE**

- Polymer is hard to etch (must use more oxygen plasma to remove)

![Image of polymer on sidewall]

Etch SiO$_2$ with CHF$_3$ plasma

---

**Deep Reactive Ion Etch**

- Inspired from polymer produced in RIE
- Patent 4455017, 4784720 by Robert Bosch GmbH, of Stuttgart, Germany
- Rapid cycling between ETCH and PASSIVATION and high-density plasma to achieve very high aspect ratio microstructures
  - ETCH: SF$_6$ + O$_2$ plasma
  - PASSIVATION: C$_4$H$_8$ to produce a fluorocarbon polymer for sidewall protection
- Sidewall scalloping: less than 50 nm roughness can be achieved
**Wet versus Dry Etching**

- **Wet Etching**
  - Excellent selectivity
  - Etching isotropic or can stop at crystal planes
  - Inexpensive
  - Fast
  - Poor dimension control
  - Hard to make repeatable
  - Surface tension upon removal of sacrificial material can cause sticking

- **Dry Etching**
  - Can etch directionally
  - Expensive equipment
  - Relatively slow
  - Excellent dimension control
  - Repeatable
  - No rinsing or drying steps

---

**Lift Off**

- Used with metals that are difficult to etch with plasmas
- Typically photoresist is soaked in chlorobenzene to form an overhanging "lip" to form discontinuous metal layer

![Diagram of Lift Off process]

- wafer with photoresist
- deposition of metal
- strip PR in acetone and lift off metal
Spindt-Tip Made by Lift-Off Process

A modified lift-off process to create sharp tips for data storage and field-emission devices

1. Double-layer mask with undercut
2. Metal evaporation
3. A sharp tip formed at closure
4. After lift-off