Lecture 2: Micromachining Processes

- Deposition (Additive techniques)
- Pattern Transfer: Optical Lithography
- Etching (Subtractive techniques)
  - Bulk and Surface Micromachining
  - Dry and Wet Etching

The Toolbox: Processes for Micromachining

- Some are inherited from IC fabrication (e.g., optical lithography), and some are unique for MEMS only (e.g., wet etching, wafer bonding, deep reactive ion etching (DRIE), etc)

Deposition (additive)
- Sputtering
- Evaporation
- CVD/LPCVD/PECVD
- Epitaxy
- Oxidation
- Spin-on
- Plating

Patterning
- Optical lithography

Etching (subtractive)
- Wet etching
- Plasma (dry) etching:
  - Chemical
  - RIE
  - DRIE
  - Lift-off*
**Physical Vapor Deposition (PVD): Sputtering**

- Physical bombardment of inert ions (Ar, He) into target to “knock out” atoms
  - Ions accelerated by E field of the dark space
- DC plasma or Radio-Frequency plasma (f = 13.56 MHz)
- Almost any thin films: metal films (Al, Ti, Pt, etc.), amorphous Si, insulators (glass and piezoelectrical ceramics PZT, ZnO)
- Equal # of electrons and ions ⇒ plasma potential is constant, and always most positive

![Diagram of Physical Vapor Deposition (PVD): Sputtering](image)

**Sputter Step Coverage**

- Dependent on temperature, pressure, and DC bias
- Better step coverage and better adhesion to the substrate than Evaporation

![Diagram of Sputter Step Coverage](image)
**Understand Film Stresses**

- **Tensile Stress** (concave bending)
- **Compressive Stress** (convex bending)

- Stresses can be extracted from measured radius of curvature (Stoney's equation)
- Undesirable mechanical features
  - Compressive stress results in “BUCKLING” for clamped-clamped mechanical structures
  - Stress gradient results in structural CURLING

---

**PVD: Evaporation**

- Local heating of target material to generate vapor, followed by condensation
- For deposition of nearly any material, including refractory metals
- **Techniques**
  - Resistive Heating
    - Needs good vacuum (10^{-7} to 10^{-6} Torr) to avoid contamination
  - Electron Beam
    - Accelerated electrons strikes and melt materials
    - Better film quality
    - X-rays produced during strikes (crystal and electronics damages)
**Evaporation Film Thickness**

- Line of sight deposition – POOR STEP COVERAGE
  - Need to rotate substrate to achieve uniform thickness

**Deposition: Chemical Vapor Deposition (CVD)**

- Produces high-quality metal and dielectric films for IC fabrication
  - Polycrystalline film: Polysilicon, tungsten, titanium, copper
  - Amorphous films: silicon oxides and nitrides, low-k dielectrics
  - Chemical reaction
    - Requires heat and mass transfer modeling
  - Relative HIGH temp. (> 300 °C)
- Types
  - CVD (APCVD): Atmosphere Pressure, 500 – 800 °C
  - LPCVD: Low Pressure, 500 – 800 °C
    - Pyrolytic reaction: thermal breakdown of gases
  - PECVD: Plasma Enhanced deposition rate, ~ 300 °C
    - Compatible with IC metallization
- Requires post-deposition anneals to “densify” the CVD films to remove voids
**LPCVD Furnace Tube**

- Wafers
- Heating coils
- Pump
- Gas inlets
- Boat

---

**CVD Silicon Dioxide**

- Most commonly used dielectric film, can be grown in situ (e.g., thermally grown gate oxide) or deposited

**Types**
- Phosphorus-doped SiO2 (PSG): good passivation layer
- Boron-doped SiO2 (BSG)
- BPSG (Low-Temp. Oxide, LTO): excellent reflow property at low temperature for planarization

**Reactions**
- Silane + O₂: SiH₄ + O₂ → SiO₂ + 2H₂
- Tetraethoxysilane (TEOS) decomposition: Si(OC₂H₅)₄ → SiO₂ + by-products
  - Excellent uniformity and step coverage (@650 – 750 °C)
- SiCl₂H₂ + 2N₂O → SiO₂ + 2N₂ + 2 HCl
  - Less used. Excellent uniformity and step coverage (@~900 °C)
Oxide Color Chart

- Interference causes colorization of light reflected from thin films; color is dependent on film thickness

<table>
<thead>
<tr>
<th>$t_{ox}$ (um)</th>
<th>color</th>
<th>$t_{ox}$ (um)</th>
<th>color</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.05</td>
<td>tan</td>
<td>0.54</td>
<td>yellow green</td>
</tr>
<tr>
<td>0.12</td>
<td>royal blue</td>
<td>0.60</td>
<td>pink</td>
</tr>
<tr>
<td>0.20</td>
<td>light gold</td>
<td>0.80</td>
<td>orange</td>
</tr>
<tr>
<td>0.25</td>
<td>orange</td>
<td>0.89</td>
<td>blue</td>
</tr>
<tr>
<td>0.31</td>
<td>blue</td>
<td>1.00</td>
<td>pink</td>
</tr>
<tr>
<td>0.34</td>
<td>green</td>
<td>1.10</td>
<td>green</td>
</tr>
<tr>
<td>0.39</td>
<td>yellow</td>
<td>1.19</td>
<td>red violet</td>
</tr>
<tr>
<td>0.47</td>
<td>violet</td>
<td>1.28</td>
<td>yellow</td>
</tr>
<tr>
<td>0.49</td>
<td>blue</td>
<td>1.40</td>
<td>orange</td>
</tr>
<tr>
<td>0.52</td>
<td>green</td>
<td>1.50</td>
<td>blue</td>
</tr>
</tbody>
</table>

CVD Polysilicon

- Polysilicon is a popular MEMS structural material, MOSFET gate material, high-value resistor, and conductor (with silicide film)
- Pyrolytic reaction: $\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2$
- LPCVD polysilicon (600 – 700 °C) exhibits a crystalline grain structure. PECVD polysilicon is completely amorphous
- Requires annealing @900 °C or above to reduce stress (~50 MPa) for MEMS application
Deposition by Plating

- Metal ions in solution deposit on conductive surface at negative potential

![Deposition by Plating Diagram]

Thermal Oxidation of Silicon

- Highest-quality SiO₂ (e.g., 10 nm gate oxide) is obtained by oxidizing Si in dry O₂
  - Reaction: Si + O₂ → SiO₂
- Wet oxidation is used to make thicker oxides (up to ~1.5 um)
  - Film thickness characterized by Deal-Grove model
  - Reaction: Si + H₂O → SiO₂ + H₂
- 46% of grown oxide is below original Si surface
- Short times: reaction-rate limited; linear rate
- Long times: diffusion limited; parabolic rate

![Thermal Oxidation of Silicon Diagram]
**Deal-Grove Model**

- The final oxide thickness $x_f$ is given by:

$$x_f = 0.5A_{DG} \left[ \sqrt{1 + \frac{4B_{DG}}{A_{DG}} (t + \tau_{DG})} - 1 \right]$$

$$\tau_{DG} = \frac{x_i^2}{B_{DG}} + \frac{x_i}{(B_{DG}/A_{DG})}$$

- Deal-Grove rate constants for dry oxidation

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>$A_{DG}$ (um)</th>
<th>$B_{DG}$ (um/hr)</th>
<th>$\tau_{DG}$ (hr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>920</td>
<td>0.235</td>
<td>0.0049</td>
<td>1.4</td>
</tr>
<tr>
<td>1000</td>
<td>0.165</td>
<td>0.0117</td>
<td>0.37</td>
</tr>
<tr>
<td>1100</td>
<td>0.090</td>
<td>0.0270</td>
<td>0.067</td>
</tr>
</tbody>
</table>

**Spin-on Deposition**

- “Spin” and “spread”
- Material types
  - Dielectric insulators
    - spin-on glass (SOG) : interlayer dielectric for IC
  - Organic materials
    - Photoresist (PR)
    - Polyimides
    - SU-8 (special thick PR, ~ 100 um)
    - Organic polymer
**Wafer Bonding**

- **Silicon Fusion Bonding** achieves direct Si-to-Si wafer bonding or with an intermediate oxide layer; hydrated surfaces annealed at 800 to 1000 °C.

- **Anodic Bonding** joins together a silicon wafer and sodium-containing glass substrate by electrostatic force.

**Pattern Transfer: Lithography**

- **Three major sequential steps:**
  - Application of photoresist (photosensitive material) by spin coating
  - Optical exposure to print mask image onto the resist
  - Immersion in an aqueous developer solution to dissolve exposed resist and render desired image

- **Light source**
  - Deep UV: \( \lambda = 150 \) to 300 nm
  - Near UV: g-line \( \lambda = 436 \) nm; i-line \( \lambda = 365 \) nm
**Positive and Negative Photoresists**

Positive PR

- Exposed regions ARE soluble
- (1) UV exposition
- (2) After development and postbake
- (3) After etching
- (4) After removing PR

Negative PR

**Light-Field and Dark-Field Masks**

Drawn patterns

Designer’s layout

Chromium

Quartz or glass

Light field

Dark field
Contact/Proximity Photolithography

Mask with opaque patterns
UV light
Contact, or close proximity
Photoresist
SiO₂
Substrate

- Mask susceptible to damage and contamination during alignment

Contact aligner

Projection Photolithography

- Mask patterns imaged onto wafers with reduction (5:1 or 10:1)
- Step and repeat pattern
- No mask degradation
- Large mask patterns are easier to make reliably
**Misregistration**

- Translational Misalignment
- Rotational Misalignment
- Mask or wafer expansion
- Etch shift and bloat

**Example: Translational Misalignment**

- Design rules are required to make working devices

![Diagram showing perfect alignment and unacceptable misalignment after two masks.](image-url)
**Bulk Silicon Micromachining**

- Dates back to a piezo-resistive silicon pressure sensor (Tufte et al., Honeywell, 1962)
- Structures made by etching substrate material (usually Si or glass wafer)
- Membranes for pressure sensors, microphones
- Nozzles for ink-jet printing, drug delivery
- Cantilevers for thermomechanical sensing
- Cavities for microfluidic chambers

---

**Isotropy of Bulk Silicon Micromachining**

- Isotropic etch
  - No etch dependence

- Anisotropic etch
  - Etch rate and profile changes with wafer or crystal orientation
**Selectivity**

- **Ratio of etch rates**: \( S = \frac{R_{etch}}{R_{mask}} \)
- **High selectivity** (\( S \gg 1 \))

![High selectivity diagram](image)

- **Low selectivity**

![Low selectivity diagram](image)

**Aspect Ratio**

- **High-aspect ratio**

![High-aspect ratio](image)

- **Low-aspect ratio** (<1:1)

![Low-aspect ratio](image)
**Bulk Micromachining**

- Trenches, STS
- Fuel atomiser, CWRU
- Suspended beam, Tohoku U.
- Micro-turbine, Tohoku U.

**Surface Micromachining**

- Structures are made by a sequence of deposition and patterning of thin films (usually < 10 um), followed by removing the SACRIFICIAL material for structural release
  - More commonly used in IC fabrication than bulk micromachining
  - Key issues: deposition temperature, intrinsic stress, step coverage, etc

**AA' cross-section**

- Sacrificial material removed
Surface Micromachining

- Many processes; common one used produces polysilicon microstructures
- Starts with deposition of insulating layers and sacrificial material

Phosphosilicate Glass (PSG), 2 um thick

Insulating layers (Si$_3$N$_4$/SiO$_2$) ~ 1000 Å

Surface Micromachining

- Selected regions of sacrificial material are patterned and removed (etched)
- Regions serve as anchor areas for succeeding structural material deposition

“Anchor” cut
Surface Micromachining

- Deposition of structural material

Phosphorous-doped polysilicon; 2 um thick

Surface Micromachining

- Structural material is patterned and etched to create desired microstructures
- Underlying sacrificial layer is exposed
Surface Micromachining

- Buffered hydrofluoric (HF) acid etches sacrificial material, releasing microstructure

- Released cantilever beam

Surface Micromachining

- Gear (Sandia Lab)
- 3D mirror (Sandia Lab)
- Micro-mirrors for projection display (Texas Instrument)
- Optical mirror switch (Lucent)
Material Removal

- Wet chemical etching
- Dry etching
  - Chemical etching
  - Ion milling
  - Plasma etching
  - Reactive-ion etching
- Lift off

Wet etching

- Etching mechanism
  - Reactant transport from etchant solution to surface
  - Surface reaction
  - Transport of etch products from surface into solution
- Reaction rate limits:
  - Mass transport is diffusion limited ⇒ etch rate increased by agitation
  - Surface reaction is rate limited ⇒ etch rate increased by increasing temperature
**Etch Stop**

- To achieve uniform and controlled depths for bulk silicon wet etching
- Electrochemical technique: wet etch stops on a passivated n-type epitaxial layer when exposed

![Diagram of Etch Stop](image)

**Other Etch Stop Techniques**

- **Dielectric Etch Stop**
  - The Si etching stops on a dielectric layer (e.g., silicon nitride) to produce a dielectric diaphragm
- **P+ Etch Stop with a heavily boron doped layer**
  - Selectivity not as high as for passivating oxides
  - Residual stress due to doped layer
  - Not likely to diffuse piezo-resistors into heavily-doped p+ silicon
**Dry Etching**

- Chemical Etching
  » Chemical reaction

- Plasma-Assisted Etching
  » Ion milling: physical sputtering
  » Plasma etching: energetic chemical reaction
  » Reactive-ion etching (RIE): physically assisted chemical reaction
  » Deep RIE

---

**Dry XeF₂ Chemical Etching**

- Vapor phase XeF₂ (Xenon difluoride) etch of Si:
  » \(2 \text{XeF}_2 + \text{Si} \rightarrow 2\text{Xe} + \text{SiF}_4\)

- Isotropic
- Excellent selectivity over photoresist, oxide, aluminum, and nitride
- Can make CMOS-integrated MEMS devices with aluminum as mask to undercut silicon
- Ideal for dry release of surface micromachined devices if polysilicon is the sacrificial material
Plasma Etching

- Disassociated gas radicals in the plasma are responsible for etching
- Wafer on grounded electrode
- Reacted material is pumped out of the chamber
- $O_2$ plasma + photoresist $\rightarrow CO_2 + H_2O$ (called “Ashing”)
- 0.1 to 10 torr operating pressure

Plasma Etch Chemistry

- Silicon
  - $CF_4 + O_2, SF_6 + O_2, CCl_4$ (for polysilicon)
- Silicon dioxide
  - $CF_4 + H_2, CHF_3$
- Silicon nitride
  - $CF_4 + O_2, CHF_3, SF_6$
- Aluminum
  - $BCl_3, CCl_4$
- Organics
  - $O_2, O_2 + CF_4, O_2 + SF_6$
### Reactive-Ion Etch

- Good directionality is achieved by operating at low pressure (10⁻³ to 10⁻¹ torr) to generate relatively higher energy ions perpendicular to wafer
- Creates polymeric species by chemical cross-linking
- Wafer on powered electrode
- Fluorocarbon etching of Si: gas phase products formed

### Unwanted Etched Feature: Stringer

- Can be removed by planarization of uneven topography using
  - Chemomechanical Polishing (CMP)
  - Resist Etchback
  - Planarization with Polymers (e.g., polyimides, SU-8)

- Conformal deposition over step
- Directional plasma etch
- CMP-planarized surface
Deep Reactive Ion Etch

- Inspired from polymer produced in RIE
- Patent 4455017, 4784720 by Robert Bosch GmbH, of Stuttgart, Germany
- Rapid cycling between ETCH and PASSIVATION and high-density plasma to achieve very high aspect ratio microstructures
  - ETCH: SF₆ + O₂ plasma
  - PASSIVATION: C₃H₈ to produce a fluorocarbon polymer for sidewall protection
- Sidewall scalloping: less than 50 nm roughness can be achieved

Wet versus Dry Etching

- Wet Etching
  - Excellent selectivity
  - Etching isotropic or can stop at crystal planes
  - Inexpensive
  - Fast
  - Poor dimension control
  - Hard to make repeatable
  - Surface tension upon removal of sacrificial material can cause sticking
- Dry Etching
  - Can etch directionally
  - Expensive equipment
  - Relatively slow
  - Excellent dimension control
  - Repeatable
  - No rinsing or drying steps
**Comparison of Silicon Etchants***

<table>
<thead>
<tr>
<th></th>
<th>HNA (HF + HNO₃ + acetic acid)</th>
<th>Alkali-OH</th>
<th>EDP (ethylene diamine pyrochatechol)</th>
<th>TMAH (tetramethylammonium hydroxide)</th>
<th>XeF₂</th>
<th>SF₆ plasma</th>
<th>DRIE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type</strong></td>
<td>Wet</td>
<td>Wet</td>
<td>Wet</td>
<td>Wet</td>
<td>Dry</td>
<td>Dry</td>
<td>Dry</td>
</tr>
<tr>
<td><strong>Anisotropic</strong></td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Varies</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Si etch rate</strong></td>
<td>1 to 3</td>
<td>1 to 2</td>
<td>1 to 30</td>
<td>- 1</td>
<td>1 to 3</td>
<td>Varies</td>
<td>&gt; 1</td>
</tr>
<tr>
<td>(µm/min)</td>
<td>(nm/min)</td>
<td>(nm/min)</td>
<td>(nm/min)</td>
<td>(nm/min)</td>
<td>(nm/min)</td>
<td>(nm/min)</td>
<td>(nm/min)</td>
</tr>
<tr>
<td><strong>Oxide mask</strong></td>
<td>10 to 30</td>
<td>1 to 10</td>
<td>1 to 80</td>
<td>- 1</td>
<td>Low</td>
<td>Low</td>
<td>low</td>
</tr>
<tr>
<td><strong>P⁺⁺ etch stop?</strong></td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>CMOS compatible?</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Si roughness</strong></td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Varies</td>
<td>High</td>
<td>Varies</td>
<td>low</td>
</tr>
</tbody>
</table>

*William and Muller, "Etch rate for micromachining processes", J. MEMS, 1996

---

**Lift Off**

- Used with metals that are difficult to etch with plasmas
- Typically photoresist is soaked in chlorobenzene to form an overhanging “lip” to form discontinuous metal layer

```
wafer with photoresist

strip PR in acetone and lift off metal
```

---

*ENEE 5400 微機電系統設計  49  ©東向成, 清華大學電機系*
**Spindt Process**

- A modified lift-off process to create sharp tips for data storage and field-emission display

1. double-layer mask with undercut
2. metal evaporation
3. a sharp tip formed at closure
4. after lift-off