Cell-Based IC Design Flow
Sequential Divider

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Divider Algorithm

- Two integers A and B
- \( A = B \times Q + R \)
  - A: dividend
  - B: divisor
  - Q: quotient
  - R: remainder

```c
R <= A;
Q <= 0;
while (R >= B) {
    R = R - B;
    Q++;
}
```

Diagram:

- States: S0, S1, S2
- Transitions:
  - S0 \(\Rightarrow\) S1: In_valid
  - S1 \(\Rightarrow\) S2: R >= B
module divider(clk, reset, A, B, in_valid, Q, R, out_valid);
parameter BITWIDTH = 10;
parameter S0 = 2'b00;
parameter S1 = 2'b11;
parameter S2 = 2'b10;
input [BITWIDTH-1:0] A, B;
input in_valid, clk, reset;
output [BITWIDTH-1:0] Q, R;
output [2:0] c_state;
reg [BITWIDTH-1:0] Q, R;
reg [2:0] n_state;
reg [BITWIDTH-1:0] n_Q, n_R;
reg out_valid;
always@(posedge clk or posedge reset) begin
    if(reset) begin
        c_state <= 0;
        Q <= 0;
        R <= 0;
    end
    else begin
        c_state <= n_state;
        Q <= n_Q;
        R <= n_R;
    end
always@(R or Q or c_state or in_valid) begin
    case(c_state)
        S0: begin
            if(in_valid) begin
                n_state = S1;
                n_R = A;
                n_Q = 0;
                out_valid = 0;
            end
            else begin
                n_state = S0;
                n_R = 0;
                n_Q = 0;
                out_valid = 0;
            end
        end
        S1: begin
            if(R == B) begin
                n_state = S1;
                n_R = R - B;
                n_Q = Q + 1;
                out_valid = 0;
            end
            else begin
                n_state = S2;
                n_R = R;
                n_Q = Q;
                out_valid = 0;
            end
        end
        S2: begin
            n_state = S0;
            n_R = R;
            n_Q = Q;
            out_valid = 1;
        end
    endcase
end
endmodule
Logic Synthesis (Synopsys)

Gate Count = 1k
Critical Delay = 1.67ns
Power = 42nW
Output signal have gate delay
Auto Place & Route (Apollo)

Critical Delay = 2.55ns

Connect Wire
Output signal have gate delay and wire delay
DRC & LVS

DRC: Design rule check
LVS: Layout versus schematic

DRC Error Summary

<table>
<thead>
<tr>
<th>Error Type</th>
<th>Num</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly Width</td>
<td>0</td>
<td>poly minimum width = 0.24</td>
</tr>
<tr>
<td>Poly Spacing</td>
<td>0</td>
<td>poly minimum spacing = 0.4</td>
</tr>
<tr>
<td>Poly Overlap</td>
<td>0</td>
<td>poly &amp; blockage overlap</td>
</tr>
<tr>
<td>Poly Notch</td>
<td>0</td>
<td>poly notch (0.4)</td>
</tr>
<tr>
<td>Cont Width</td>
<td>0</td>
<td>polyCont minimum width = 0.3</td>
</tr>
<tr>
<td>Cont Spacing</td>
<td>0</td>
<td>polyCont minimum spacing = 0.3</td>
</tr>
<tr>
<td>Met1 Width</td>
<td>0</td>
<td>metall minimum width = 0.32</td>
</tr>
<tr>
<td>Met1 Spacing</td>
<td>0</td>
<td>metall minimum spacing = 0.32</td>
</tr>
<tr>
<td>Met1 Thir&amp;Fat</td>
<td>0</td>
<td>metall minimum spacing [0.32 and 10] = 0.6</td>
</tr>
<tr>
<td>Met1 Fat&amp;Fat</td>
<td>0</td>
<td>metall minimum spacing [10 and 10] = 0.6</td>
</tr>
<tr>
<td>Met1 Overlap</td>
<td>0</td>
<td>metall &amp; blockage overlap</td>
</tr>
<tr>
<td>Met1 Notch</td>
<td>0</td>
<td>metall notch (0.32)</td>
</tr>
<tr>
<td>Met1 PatNotch</td>
<td>0</td>
<td>metall Pat[10] notch (0.5)</td>
</tr>
<tr>
<td>Via1 Width</td>
<td>0</td>
<td>via1 minimum width = 0.35</td>
</tr>
<tr>
<td>Via1 Spacing</td>
<td>0</td>
<td>via1 minimum spacing = 0.35</td>
</tr>
<tr>
<td>Via1&amp;Via1BLk Sp</td>
<td>0</td>
<td>via1 &amp; via1Blockage minimum spacing = 0.35</td>
</tr>
</tbody>
</table>

LVS Error Summary

<table>
<thead>
<tr>
<th>Error Type</th>
<th>Num</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floating Port</td>
<td>0</td>
<td>Floating ports have been detected by LVS.</td>
</tr>
<tr>
<td>Floating Net</td>
<td>0</td>
<td>Floating Nets have been detected by LVS.</td>
</tr>
<tr>
<td>SHORT</td>
<td>0</td>
<td>SHORTS have been detected by LVS.</td>
</tr>
<tr>
<td>OPEN</td>
<td>0</td>
<td>OPENS have been detected by LVS.</td>
</tr>
<tr>
<td>Electric Equivalent</td>
<td>0</td>
<td>Electrical-Equivalent Errors have been detected by LVS.</td>
</tr>
<tr>
<td>MustJoin</td>
<td>0</td>
<td>MustJoin Errors have been detected by LVS.</td>
</tr>
<tr>
<td>Min Area</td>
<td>0</td>
<td>Minimum Area Errors have been detected by LVS.</td>
</tr>
</tbody>
</table>